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METHODS AND APPARATUS FOR RESISTANCE VARIABLE MATERIAL CELLS

Background of the Invention

Field of the Invention

The present invention is generally related to memory technology. In particular, the present invention relates to memory devices formed using chalcogenide glasses.

Description of the Related Art

Computers and other digital systems use memory to store programs and data. A common form of memory is random access memory (RAM). Many memory devices, such as dynamic random access memory (DRAM) devices and static random access memory (SRAM) devices are volatile memories. A volatile memory loses its data when power is removed. In addition, certain volatile memories such as DRAM devices require periodic refresh cycles to retain their data even when power is continuously supplied.

In contrast to the potential loss of data encountered in volatile memory devices, nonvolatile memory devices retain data when power is removed. Examples of nonvolatile memory devices include read only memory (ROM), programmable read only memory (PROM), erasable programmable read only memory (EPROM), electrically erasable programmable read only memory (EEPROM), and the like.

U.S. Patent No. 6,084,796 to Kozicki, et al., entitled "Programmable metallization cell structure and method of making same," discloses another type of nonvolatile memory device known as a programmable conductor memory cell or a programmable metallization cell (PMC). Such memory cells can be integrated into a memory device, which is known as a programmable conductor random access memory (PCRAM). Additional applications for a programmable metallization cell include use as a programmable resistance and a programmable capacitance.

One conventional technique for producing the programmable conductor memory cell applies silver (Ag) photodoping to a chalcogenide glass, such as germanium selenide ($Ge_xSe_{(1-x)}$). As reported by Mitkova, et al, in "Dual Chemical Role of Ag as an Additive in Chalcogenide Glasses," *Physical Review Letters*, Vol. 83, no. 19 (Nov. 8, 1999), pp. 3848-3851, silver (Ag) can only be photodoped into glasses of specific stoichiometries that form silver selenide and a new glass stoichiometry backbone. Further, glasses that can be photodoped with silver (Ag) are "floppy" and switch relatively slowly as compared to a rigid glass. Boolchand, et al., in *Onset of Rigidity in Steps in Chalcogenide Glass*, Properties and Applications of Amorphous Materials, pp. 97-132, (2001), observes a floppy to rigid transition in $Ge_xSe_{(1-x)}$ glasses that occurs when $x = 0.23$, where x corresponds to the germanium molar concentration.

In addition, Mitkova, et al., found that glasses that fall within the stoichiometry range defined by region II of Figure 1 of the Mitkova reference do not form silver selenide when doped with silver (Ag). For example, a rigid glass, such as germanium selenide ($Ge_{40}Se_{60}$) will not form

silver selenide when photodoped with silver (Ag) and, as a result, does not function as a memory switch.

The presence of silver selenide in a GexSe1-x glass photodoped with silver (Ag) allows the glass to be used as a memory switch. Glasses used for silver (Ag) incorporation via photodoping are floppy and switch more slowly electrically, and with worse memory retention, than glasses that are rigid. Preferred rigid glasses, e.g., $Ge_{40}Se_{60}$, do not form silver selenide when photodoped with silver (Ag). However, the relatively fast switching times and relatively good memory retention occur in a system which incorporates silver selenide and a rigid glass such as $Ge_{40}Se_{60}$. What is needed is a technique to form this type of memory cell.

Summary of the Invention

Embodiments of the invention overcome the disadvantages of the prior art. Embodiments of the invention include processes that advantageously allow the production of resistance variable material memory cells at relatively high rates and with relatively high yields. The resistance variable memory cells further advantageously feature improvements in switching speed, improvements in switching consistency, and improvements in data retention and operational temperature ranges relative to conventional programmable conductor memory cells.

Advantageously, embodiments of the present invention can be fabricated with relatively wide ranges for the thicknesses of silver chalcogenide and glass layers. Thus, memory cells can be fabricated without the relatively precise control of silver (Ag) and glass thicknesses that are necessary in a conventional photodoping process to maintain an appropriate amount of silver (Ag) in the glass without inducing crystallization in the memory cell. In addition, embodiments of the present invention can advantageously form memory cells on rigid glasses, such as $Ge_{40}Se_{60}$, which would normally incorporate silver (Ag) into the glass backbone making it unavailable for memory switching. These glasses have an additional advantage of having higher glass transition temperatures.

In one embodiment, silver (Ag) is not added directly to germanium selenide ($Ge_xSe_{(1-x)}$). Thus, adherence of a layer of silver (Ag) to a layer of germanium selenide ($Ge_xSe_{(1-x)}$) is advantageously not a concern.

One embodiment according to the present invention includes a memory cell with a layer of a silver chalcogenide and a layer of a chalcogenide glass, such as germanium selenide ($Ge_xSe_{(1-x)}$). The layers of silver chalcogenide and chalcogenide glass are formed between two electrodes, which are also formed. The electrodes can be formed from materials such as tungsten (W), tungsten nitride (WN), titanium (Ti), and the like. The silver chalcogenide can correspond to a variety of materials, such as silver selenide, silver sulfide, silver telluride, and silver oxide. The chalcogenide glass can correspond to a variety of materials, such as germanium selenide ($Ge_xSe_{(1-x)}$), germanium sulfide ($Ge_xS_{(1-x)}$) and arsenic selenide (As_xSe_y).

Another embodiment according to the present invention includes a memory cell with a layer of silver (Ag), a layer of chalcogenide glass, such as germanium selenide ($Ge_xSe_{(1-x)}$), and a layer of silver selenide disposed between two electrodes. In one embodiment, the layers are arranged such that the chalcogenide glass is disposed between the layer of silver (Ag) and the layer of silver selenide. The chalcogenide glass can be selected from a variety of glasses such as $Ge_{40}Se_{60}$ and $Ge_{25}Se_{75}$. In one embodiment, the silver selenide is slightly poor in silver (Ag) and the presence of silver (Ag) in the silver (Ag) layer allows the memory cell to function as intended.

Another embodiment according to the present invention includes a memory cell with co-deposited silver selenide and germanium selenide ($Ge_xSe_{(1-x)}$). The memory cell can correspond to non-volatile memories or to volatile memories.

One embodiment according to the present invention is a process of fabricating a memory. The process forms an active layer on a bottom electrode. The process forms the active layer, which includes a silver chalcogenide, such as silver selenide, and a selenium-including glass, such as germanium selenide, substantially in the absence of an ultraviolet (UV) photodoping step. The process also forms a top electrode layer such that a voltage applied between the top electrode layer and the bottom electrode layer creates a conductive pathway between the two electrodes, or disrupts a conductive pathway that had connected the two electrodes.

Another embodiment according to the present invention includes a physical vapor deposition (PVD) process of fabricating an active layer in a memory cell. The PVD process fabricates the active layer by co-depositing silver chalcogenide, such as silver selenide, and a chalcogenide glass, such as germanium selenide ($Ge_xSe_{(1-x)}$), on a bottom electrode at substantially the same time. The process forms a top electrode layer on the active layer such that a voltage or difference in electric potential applied between the top electrode layer and the bottom electrode can form or disrupt a conductive pathway within the active layer.

Another embodiment according to the present invention includes a deposition process to form an active layer in a substrate assembly by forming a layer of a chalcogenide glass and forming a layer of silver selenide. The layers are disposed between a top electrode layer and a bottom electrode layer. In one embodiment, the chalcogenide glass is germanium selenide ($Ge_xSe_{(1-x)}$), and there are no other sources of silver (Ag) other than silver selenide. In another embodiment, the chalcogenide glass is germanium selenide ($Ge_xSe_{(1-x)}$) and at least one of the electrodes is silver (Ag).

Another embodiment according to the present invention includes a process that forms an active layer of a memory cell by forming a layer of both germanium selenide ($Ge_xSe_{(1-x)}$) and silver (Ag) and forming a layer of silver selenide.

Brief Description of the Drawings

These and other features of the invention will now be described with reference to the drawings summarized below. These drawings and the associated description are provided to

illustrate preferred embodiments of the invention and are not intended to limit the scope of the invention.

Figure 1 illustrates a process according to an embodiment of the invention of forming an active layer by layering silver selenide and a chalcogenide glass.

Figure 2 illustrates a process according to an embodiment of the invention of forming an active layer by co-depositing silver selenide and a chalcogenide glass.

Figure 3 illustrates a process according to an embodiment of the invention of forming an active layer by depositing a layer of germanium selenide ($Ge_xSe_{(1-x)}$) and silver (Ag) and a layer of silver selenide.

Figure 4 illustrates a memory cell with an active layer formed by layering silver selenide and a chalcogenide glass.

Figure 5 illustrates a memory cell with an active layer formed by co-depositing silver selenide and a chalcogenide glass.

Figure 6 illustrates a memory cell with an active layer formed by layering silver (Ag), layering a chalcogenide glass, and layering silver selenide.

Detailed Description of the Preferred Embodiments

Although this invention will be described in terms of certain preferred embodiments, other embodiments that are apparent to those of ordinary skill in the art, including embodiments which do not provide all of the benefits and features set forth herein, are also within the scope of this invention. Accordingly, the scope of the invention is defined only by reference to the appended claims.

While illustrated in the context of silver selenide and germanium selenide, the skilled artisan will appreciate that the principles and advantages described herein are applicable to other types of silver chalcogenides and chalcogenide glasses. For example, other silver chalcogenides include silver sulfide, silver telluride, and silver oxide. Another chalcogenide glass includes arsenic selenide (As_xSe_y).

Applicant has discovered that regions of silver selenide within germanium selenide ($Ge_xSe_{(1-x)}$) are the source of the memory switching characteristic of silver (Ag) ultraviolet (UV) photodoped germanium selenide glasses in a resistance variable material memory cell. Mitkova, et al., observed with Modulated Differential Scanning Calorimetry (MDSC) experiments that silver (Ag) photodoping of germanium selenide ($Ge_xSe_{(1-x)}$) glasses of glass forming region I (selenide rich glasses) resulted in phase separation of silver selenide and a new stoichiometry of germanium selenide ($Ge_ySe_{(1-y)}$) backbone.

Figure 1 illustrates a process 100 according to an embodiment of the invention of forming an active layer for a memory cell by layering silver selenide and a chalcogenide glass. The term "silver selenide," as used herein, includes stoichiometric silver selenide (Ag_2Se), silver-rich silver selenide ($Ag_{2+x}Se$), and silver-poor silver selenide ($Ag_{2-x}Se$). The term "chalcogenide glass," as

used herein, includes glasses with an element from group VIA (or group 16) of the periodic table. Group VIA elements include sulfur (S), selenium (Se), tellurium (Te), polonium (Po), and oxygen (O). In one embodiment, the process advantageously eliminates the UV photodoping step.

The process can be applied to a broad variety of substrate assemblies. Advantageously, many configurations for a resistance variable material cell, such as the "PROM configured MDM" described by Kozicki, et al., in U.S. Patent No. 6,084,796, do not require local transistors as part the storage element and can thus be formed on a variety of substrates and not just semiconductors. For example, a resistance variable material cell can be formed on other materials such as a plastic substrate. The substrate assembly should be electrically insulating so that a difference in electric potential can be applied between electrodes to form or to disrupt a conductive pathway in the cell. Where the substrate assembly is not intrinsically insulating, the process can also form an insulating layer, such as a layer of silicon oxide (SiO_2), to electrically insulate the resistance variable material cell. In one embodiment, the substrate assembly is silicon to facilitate the integration of the fabricated memory cell with electronic devices such as switches or transistors.

The process forms 110 a conductive film on the substrate assembly to form a first electrode of the memory cell. The material used to form the conductive film can be selected from a variety of conductive materials. In one embodiment, the process deposits tungsten (W) as the first electrode. The process advances from forming 110 the first electrode to forming 120 a silver selenide layer.

The process forms 120 a film or layer of silver selenide onto the first electrode. In the process illustrated by Figure 1, the process first forms 120 a silver selenide layer and then forms 130 a germanium selenide ($Ge_xSe_{(1-x)}$) layer. It will be understood by one of ordinary skill in the art that in another embodiment, the process first forms 130 a germanium selenide layer ($Ge_xSe_{(1-x)}$) and then forms 120 a silver selenide layer. A variety of processes can be used to form 120 the layer of silver selenide. Preferably, physical vapor deposition (PVD) techniques, such as evaporative deposition and sputtering, are used to form 120 the layer of silver selenide. Other processes, such as chemical vapor deposition (CVD), co-evaporation, and depositing a layer of selenide (Se) above a layer of silver (Ag) to form silver selenide can also be used.

Advantageously, silver selenide is directly deposited, thereby obviating the need to photodope the substrate with UV radiation. Of course, UV photodoping can still be used. Where UV photodoping is still used, the direct forming of a layer of silver selenide can still advantageously reduce the intensity and/or the duration of the applied UV radiation. Further advantageously, since light does not need to shine on the silver selenide layer, the silver selenide layer can be formed 120 prior to the forming 130 of the chalcogenide layer as shown in Figure 1. The process advances from forming 120 the silver selenide layer to forming 130 the chalcogenide layer.

The process forms 130 a layer of a chalcogenide glass. For example, the chalcogenide glass can be germanium selenide ($Ge_xSe_{(1-x)}$), arsenic selenide (As_2Se_3), and the like. Preferably, the

chalcogenide glass formed is germanium selenide ($Ge_xSe_{(1-x)}$). In one embodiment, x is in a range of about 0.2 to about 0.43. An exemplary chalcogenide glass is $Ge_{40}Se_{60}$.

Preferably, the process forms 120 the silver selenide layer, and the process forms 130 the layer of germanium selenide ($Ge_xSe_{(1-x)}$) such that the silver selenide layer is between about 300 to 1000 Angstroms (Å) thick, and such that the germanium selenide ($Ge_xSe_{(1-x)}$) layer is between about 200 to 1000 Å thick. In one embodiment, the silver selenide layer is about 400 Å thick, and the germanium selenide ($Ge_xSe_{(1-x)}$) layer is a layer of $Ge_{40}Se_{60}$ that is about 250 Å thick.

The process forms 140 a second electrode of the resistance variable material cell, and the process ends. It will be understood by one of ordinary skill in the art that the first electrode and the second electrode can correspond to, for example, a top electrode and a bottom electrode, respectively, or to side electrodes. The layer of silver selenide formed 120 by the process and the layer of chalcogenide glass formed 130 by the process are disposed between the first electrode and the second electrode. When an electric potential is applied between the first electrode and the second electrode, a conductive pathway is formed or is disrupted in the layer of silver selenide and the layer of chalcogenide glass.

The formation of the conductive pathway lowers the resistance between the electrodes. The conductive pathway persists after the removal of the applied electric potential. This property can permit some embodiments of a resistance variable material cell to retain information in a nonvolatile manner.

Figure 2 illustrates another process 200 according to an embodiment of the invention of forming an active layer for a memory cell. In the illustrated process, the active layer is formed by depositing silver selenide and a chalcogenide glass substantially in a single step. In one embodiment, the process advantageously eliminates the UV photodoping step.

The process illustrated in Figure 2 can also be applied to a broad variety of substrate assemblies as described earlier in connection with Figure 1. The process forms 210 a conductive film on the substrate assembly to form a first electrode of the memory cell. The material used to form the conductive film can be selected from a variety of conductive materials as described earlier in connection with Figure 1. The process advances from forming 210 the first electrode to forming 220 an active layer.

The process forms 220 the active film in which a conductive pathway forms and/or is disrupted. The illustrated process co-deposits 220 silver selenide and a chalcogenide glass to form 220 the active layer. In one embodiment, physical vapor deposition (PVD) techniques such as evaporative deposition, sputtering, and the like, are used to form 220 the active layer. The chalcogenide glass can include materials such as germanium selenide ($Ge_xSe_{(1-x)}$), arsenic selenide (As_2Se_3), and the like. In one embodiment, the chalcogenide glass is germanium selenide ($Ge_xSe_{(1-x)}$), where x is between about 0.2 and about 0.43.

The thickness of the active layer formed by the process can vary in a relatively broad range. Preferably, the process forms 220 the active layer to a thickness between about 500 Å and about 2000 Å. More preferably, the process forms 220 the active layer to a thickness between about 500 Å and about 700 Å. In one example, the process forms 220 the active layer to a thickness of about 500 Angstroms (Å).

Advantageously, the illustrated process can form an active layer without silver (Ag) photodoping with UV radiation. In another embodiment, UV photodoping is still used. The process advances from forming 220 the active layer to forming 230 a second electrode.

The process forms 230 a conductive film on the substrate assembly to form a second electrode of the memory cell, and the process ends. The active layer formed 220 is disposed between the first electrode and the second electrode. When an electric potential is applied between the first electrode and the second electrode, a conductive pathway is formed or disrupted depending on the polarity of the applied electric potential. The formation and/or disruption of the conductive pathway is stable and can be detected as a change in impedance.

Figure 3 illustrates a process 300 according to an embodiment of the invention of forming an active layer of a memory cell by depositing a layer of germanium selenide ($Ge_xSe_{(1-x)}$) and silver (Ag), and a layer of silver selenide. In one embodiment, x is in a range of about 0.2 to about 0.43.

The process forms 310 a conductive film on a substrate assembly to form a first electrode of the memory cell. The material used to form the conductive film can be selected from a variety of conductive materials. In one embodiment, the process deposits tungsten (W) as the first electrode. The process advances from forming 310 the first electrode to forming 320 a film or layer of germanium selenide ($Ge_xSe_{(1-x)}$) and silver (Ag).

The process forms 320 the layer(s) of germanium selenide ($Ge_xSe_{(1-x)}$) and silver (Ag) onto the first electrode. The process can form the layer(s) of germanium selenide ($Ge_xSe_{(1-x)}$) and silver (Ag) in one layer or as separate layers. In one embodiment, the process co-deposits germanium selenide ($Ge_xSe_{(1-x)}$) and silver (Ag) to form 320 the layer. In another embodiment, the process forms 320 the layer(s) of germanium selenide ($Ge_xSe_{(1-x)}$) and silver (Ag) by depositing separate layers of germanium selenide ($Ge_xSe_{(1-x)}$) and silver (Ag). One embodiment according to the invention forms a relatively thin layer of silver (Ag), and then forms the layer of germanium selenide ($Ge_xSe_{(1-x)}$). In one embodiment, the relatively thin layer of silver (Ag) is about 50 Å thick. A layer of silver selenide should not be formed adjacent to the relatively thin layer of silver (Ag). Preferably, the process forms 320 the film or layer of germanium selenide ($Ge_xSe_{(1-x)}$) and silver (Ag) to a thickness between about 250 Å and 1000 Å.

In the process illustrated by Figure 3, the process forms 320 the layer(s) of both germanium selenide ($Ge_xSe_{(1-x)}$) and silver (Ag) and then forms 330 a layer of silver selenide. Preferably, the process forms 330 the layer of silver selenide to a thickness between about 300 Å and about 1000 Å. It will be understood by one of ordinary skill in the art that in another embodiment, the process

first forms 330 the silver selenide layer and then forms 320 the layer(s) of germanium selenide ($Ge_xSe_{(1-x)}$) and silver (Ag). In addition, the deposition of the relatively thin film of silver (Ag) advantageously allows the silver selenide layer to be formed slightly silver-poor because an extra amount of silver (Ag) is available to the memory cell.

A variety of processes can be used to form 320 the layer(s) of germanium selenide ($Ge_xSe_{(1-x)}$) and silver (Ag). Preferably, physical vapor deposition (PVD) techniques, such as evaporative deposition and sputtering, are used to form 320 the layer of germanium selenide ($Ge_xSe_{(1-x)}$) and silver (Ag). Other processes, such as chemical vapor deposition (CVD) and co-evaporation can also be used. The process advances from forming 320 the layer of germanium selenide ($Ge_xSe_{(1-x)}$) and silver (Ag) to forming 330 a layer of silver selenide.

The process forms 330 a layer of a silver selenide. The layer of silver selenide should be formed on the germanium selenide ($Ge_xSe_{(1-x)}$) layer or on a co-deposited layer of silver (Ag) and germanium selenide ($Ge_xSe_{(1-x)}$), but not directly on a silver (Ag) layer. Advantageously, silver selenide is directly deposited and a UV photodoping step is not needed.

The process forms 340 a second electrode of the memory cell, and the process ends. It will be understood by one of ordinary skill in the art that the first electrode and the second electrode can correspond to, for example, a top electrode and a bottom electrode, respectively, or to side electrodes. The layer(s) of germanium selenide ($Ge_xSe_{(1-x)}$) and silver (Ag) formed 320 by the process and the layer of silver selenide formed 330 by the process are disposed between the first electrode and the second electrode. When an electric potential is applied between the first electrode and the second electrode, a conductive pathway is formed or is disrupted in the layer of silver selenide and the layer(s) of germanium selenide ($Ge_xSe_{(1-x)}$) and silver (Ag).

The stored information can correspond to programmable resistances and to binary data storage. In one embodiment, where the memory cell stores binary data, a first state corresponds to a relatively low resistance between the electrodes and a second state corresponds to a relatively high resistance between the electrodes. In addition, the polarity of the electrodes can be reversed to alter the conductive pathway, thereby allowing the memory cell to be erased and reprogrammed.

Figure 4 illustrates one embodiment according to the present invention of a memory cell 400 with an active layer formed by layering silver selenide and a chalcogenide glass. The illustrated memory cell 400 includes a first electrode 402, a first body layer 404, a second body layer 406, an insulator 408, and a second electrode 410.

The first electrode 402 is formed on and in contact with a substrate assembly. In one embodiment, the substrate assembly is silicon, and the first electrode 402 is coupled to a conductor such as a crosspoint so that the memory cell 400 can be programmed and read. The skilled artisan will appreciate that the memory cell 400 can be formed on a variety of substrate materials and not just semiconductors such as silicon. For example, the memory cell 400 can be formed on a plastic substrate. The first electrode 402 can be made from a variety of materials and from combinations

of materials. For example, the first electrode 402 can be made from tungsten (W), tungsten nitride (WN), polysilicon, and the like.

When the memory cell 400 is fabricated, the first body layer 404 and the second body layer 406 form a body of the memory cell 400. The first body layer 404 is formed on the first electrode 402, and the second body layer 406 is formed on the first body layer 404.

In the illustrated embodiment, the first body layer 404 is a layer of silver selenide and the second body layer 406 is a layer of a chalcogenide glass such as germanium selenide ($Ge_xSe_{(1-x)}$). In another embodiment, the first body layer 404 is the layer of chalcogenide glass and the second body layer 406 is the layer of silver selenide.

In the illustrated embodiment, the insulator 408 surrounds the body formed by the first body layer 404 and the second body layer 406. The insulator 408 insulates the body from the bodies of other memory cells and also prevents the undesired diffusion of active material. The insulator 408 can be formed from a variety of materials such as silicon nitride (Si_3N_4). Of course, the insulator 408 can be formed in multiple steps and can include multiple structures.

The second electrode 410 is formed on the second body layer 406 and on the insulator 408. The second electrode 410 can be formed from a variety of materials such as silver (Ag), titanium (Ti), tungsten (W), tungsten nitride (WN), and the like. An electric potential applied between the first electrode 402 and the second electrode 410 causes the formation or alteration of conductive pathways in the body of the memory cell 400.

Figure 5 illustrates one embodiment according to the present invention of a memory cell 500 with an active layer formed by co-depositing silver selenide and a chalcogenide glass. The illustrated memory cell 500 includes a first electrode 502, an active layer 506, an insulator 508, and a second electrode 510.

The first electrode 502 is formed on a substrate assembly. The substrate assembly can correspond to a variety of materials including plastic and silicon. Preferably, the first electrode 502 is coupled to a conductor such as a crosspoint so that the memory cell 500 can be programmed and read. The first electrode 502 can be made from a variety of materials and from combinations of materials.

The active layer 506 is formed on the first electrode 502. In the illustrated embodiment, the active layer 506 is a co-deposited layer of silver selenide and a chalcogenide glass such as germanium selenide ($Ge_xSe_{(1-x)}$).

In the illustrated embodiment, the insulator 508 surrounds the active layer 506. The insulator 508 insulates the active layer 506 from other memory cells and also prevents the undesired diffusion of active material. The insulator 508 can be formed from a variety of materials such as silicon nitride (Si_3N_4).

The second electrode 510 is formed on the active layer 506 and on the insulator 508. The second electrode 510 can be formed from a variety of materials such as silver (Ag), titanium (Ti),

tungsten (W), tungsten nitride (WN), and the like. An electric potential applied between the first electrode 502 and the second electrode 510 causes conductive pathways in the active layer 506 to form or to disrupt in response to the applied electric potential.

Figure 6 illustrates one embodiment according to the present invention of a memory cell 600 with an active layer formed by layering silver (Ag), layering a chalcogenide glass, and layering silver selenide. The illustrated memory cell 600 includes a first electrode 602, a first body layer 603, a second body layer 604, a third body layer 606, an insulator 608, and a second electrode 610.

The first electrode 602 is formed on and in contact with a substrate assembly. In one embodiment, the substrate assembly is silicon, and the first electrode 602 is coupled to a conductor such as a crosspoint so that the memory cell 600 can be programmed and read. The first electrode 602 can be made from a variety of materials and from combinations of materials such as tungsten (W), tungsten nitride (WN), titanium (Ti), and the like.

When the memory cell 600 is fabricated, the first body layer 603, the second body layer 604, and the third body layer 606 form a body of the memory cell 600. The first body layer 603 is formed on the first electrode 602, the second body layer 604 is formed on the first body layer 603, and the third body layer 606 is formed on the second body layer 604.

In the illustrated embodiment, the first body layer 603 is a layer of silver (Ag), the second body layer 604 is a layer of a chalcogenide glass such as germanium selenide ($Ge_xSe_{(1-x)}$), and the third body layer 606 is a layer of silver selenide. In another embodiment, the first body layer 603 is the layer of silver selenide, the second body layer 604 is the layer of chalcogenide glass, and the third body layer 606 is the layer of silver (Ag).

In the illustrated embodiment, the insulator 608 surrounds the body formed by the first body layer 603, the second body layer 604, and the third body layer 606. The insulator 608 insulates the body from the bodies of other memory cells and also prevents the undesired diffusion of active material. The insulator 608 can be formed from a variety of materials such as silicon nitride (Si_3N_4). Of course, the insulator 608 can be formed in multiple steps and can include multiple structures.

The second electrode 610 is formed on the third body layer 606 and on the insulator 608. The second electrode 610 can be formed from a variety of materials such as tungsten (W). An electric potential applied between the first electrode 602 and the second electrode 610 causes the formation or alteration of conductive pathways in the body of the memory cell 600.

Various embodiments of the invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined in the appended claims.

I CLAIM:

1. A memory cell comprising:

a first electrode deposited on a substrate body;

a second electrode, where the first electrode and the second electrode provide access to the memory cell;

a first layer of a silver chalcogenide disposed between the first electrode and the second electrode, where the first layer forms a first portion of a memory cell body; and

a second layer of a chalcogenide glass that forms a second portion of the memory cell body, where the second layer is also disposed between the first electrode and the second electrode, where the chalcogenide glass permits a conductive pathway to form between the first electrode and the second electrode in response to an electric potential applied between the first electrode and the second electrode.

2. The memory cell as defined in Claim 1, wherein the first layer of the silver chalcogenide is formed directly on the first electrode.

3. The memory cell as defined in Claim 1, wherein the second layer of the chalcogenide glass is formed directly on the first electrode.

4. The memory cell as defined in Claim 1, wherein the silver chalcogenide comprises silver selenide.

5. The memory cell as defined in Claim 1, wherein the silver chalcogenide comprises silver sulfide.

6. The memory cell as defined in Claim 1, wherein the silver chalcogenide comprises silver telluride.

7. The memory cell as defined in Claim 1, wherein the silver chalcogenide comprises silver oxide.

8. The memory cell as defined in Claim 1, wherein the chalcogenide glass comprises germanium selenide ($Ge_xSe_{(1-x)}$).

9. The memory cell as defined in Claim 1, wherein the chalcogenide glass comprises arsenic selenide (As_xSe_y).

10. The memory cell as defined in Claim 1, wherein the chalcogenide glass comprises germanium sulfide ($Ge_xS_{(1-x)}$).

11. The memory cell as defined in Claim 1, wherein the chalcogenide glass is selected from the group of chalcogenide glasses that comprise selenium, can be doped with silver, and can remain an amorphous material after the doping with silver.

12. The memory cell as defined in Claim 1, further comprising a third layer of a silver (Ag) that forms a third portion of the memory cell body, where the third layer is also disposed between the first electrode and the second electrode, where the first layer, the second layer, and the

third layer are arranged such that the second layer of chalcogenide glass is disposed between the first layer of the silver chalcogenide and the third layer of silver (Ag).

13. The memory cell as defined in Claim 1, wherein at least one of the first electrode and the second electrode comprises tungsten (W).

14. A memory cell comprising;

a first electrode;

a second electrode, where the first electrode and the second electrode provide access to the memory cell; and

a memory cell body disposed between the first electrode and the second electrode, where the memory cell body comprises a layer of intermixed silver selenide and germanium selenide ($Ge_xSe_{(1-x)}$), wherein said layer has substantially no sliver dispersed therein except where present in a conductive pathway.

15. The memory cell as defined in Claim 14, wherein x is in the range of about 0.2 to about 0.43.

16. The memory cell as defined in Claim 14, wherein the germanium selenide ($Ge_xSe_{(1-x)}$) is $Ge_{40}Se_{60}$.

17. The memory cell as defined in Claim 14, wherein the germanium selenide ($Ge_xSe_{(1-x)}$) is $Ge_{25}Se_{75}$.

18. The memory cell as defined in Claim 14, wherein the memory cell body is from about 1:1 to about 5:1 silver selenide to germanium selenide ($Ge_xSe_{(1-x)}$).

19. The memory cell as defined in Claim 14, wherein the memory cell body is from about 1.43:1 to about 2:1 silver selenide to germanium selenide ($Ge_xSe_{(1-x)}$).

20. The memory cell as defined in Claim 14, wherein the memory cell body is from about 1.72:1 to about 1.75:1 silver selenide to germanium selenide ($Ge_xSe_{(1-x)}$).

21. A process of fabricating a memory structure in a substrate assembly, the process comprising:

forming a bottom electrode in contact with a conductive region in the substrate assembly;

forming an active layer on the bottom electrode, where the active layer includes a silver chalcogenide and a selenium-including glass, where the active layer is formed substantially in the absence of an ultraviolet (UV) photodoping step and in the absence of a thermal doping step; and

forming a top electrode layer such that a voltage applied across the top electrode layer and the bottom electrode layer generates an electric field in the active layer.

22. The process as defined in Claim 21, wherein the selenium-including glass is germanium selenide ($Ge_xSe_{(1-x)}$) wherein x is selected from a range of about 0.2 to about 0.43.

23. The process as defined in Claim 21, wherein the silver chalcogenide comprises silver selenide.

24. A physical vapor deposition (PVD) process of fabricating an active layer in a memory cell, the process comprising:

forming a bottom electrode in contact with a conductive region in a semiconductor base material;

depositing both a silver chalcogenide and a chalcogenide glass at the same time on the bottom electrode; and

forming a top electrode layer, where a voltage applied to the top electrode layer and the bottom electrode layer generates the electric field in the active layer.

25. The process as defined in Claim 24, wherein the depositing both the silver chalcogenide and the chalcogenide glass further comprises:

evaporating silver selenide as the silver chalcogenide;

evaporating germanium selenide ($Ge_xSe_{(1-x)}$) as the chalcogenide glass;

introducing the vaporized silver selenide and the vaporized germanium selenide ($Ge_xSe_{(1-x)}$) to the interior of a deposition chamber; and

depositing the vaporized silver selenide and the vaporized germanium selenide ($Ge_xSe_{(1-x)}$) at the same time onto the bottom electrode to form the active layer.

26. The process as defined in Claim 24, wherein x is in a range from about 0.2 to about 0.43.

27. The process as defined in Claim 24, wherein the active layer is deposited such that a ratio of silver selenide as the silver chalcogenide to germanium selenide ($Ge_xSe_{(1-x)}$) as the chalcogenide glass in the active layer is in a range of about 1:1 to about 5:1 by volume.

28. A deposition process of fabricating at least a portion of an integrated circuit, the process comprising:

forming a bottom electrode in contact with a conductive region in a semiconductor base material;

forming a layer of a chalcogenide glass;

forming a layer of a silver chalcogenide, where the layer of the chalcogenide glass and the layer of the silver chalcogenide are adjacent to each other and form an active layer that is capable of supporting the formation of a conductive pathway in the presence of an electric field; and

forming a top electrode layer such that the layer of the chalcogenide glass and the layer of the silver chalcogenide are disposed between the top electrode layer and the bottom electrode layer, where an electric potential applied between the top electrode layer and the bottom electrode layer generates the electric field in the active layer.

29. The process as defined in Claim 28, wherein the layer of chalcogenide glass is germanium selenide ($Ge_xSe_{(1-x)}$), and where the process forms the layer of chalcogenide glass to a thickness within a range of about 200 Angstroms (Å) to about 1000 Å.

30. The process as defined in Claim 28, wherein the chalcogenide glass comprises germanium selenide ($Ge_xSe_{(1-x)}$).

31. The process as defined in Claim 28, wherein the chalcogenide glass comprises arsenic selenide (As_2Se_3).

32. The process as defined in Claim 28, wherein the chalcogenide glass comprises germanium sulfide ($Ge_xS_{(1-x)}$).

33. The process as defined in Claim 28, wherein the silver chalcogenide comprises silver selenide.

34. The process as defined in Claim 28, wherein the silver chalcogenide comprises silver sulfide.

35. The process as defined in Claim 28, wherein the silver chalcogenide comprises silver telluride.

36. The process as defined in Claim 28, wherein the silver chalcogenide comprises silver oxide.

37. The process as defined in Claim 28, wherein the process forms the layer of the chalcogenide glass and the layer of silver chalcogenide by evaporative deposition.

38. The process as defined in Claim 28, wherein the process forms the layer of the chalcogenide glass and the layer of silver chalcogenide by sputtering deposition.

39. A process of forming an active layer in a substrate assembly, where the active layer is capable of supporting the formation of conductive pathways in the presence of an electric potential applied to electrodes, the process comprising:

providing a first amount of germanium selenide ($Ge_xSe_{(1-x)}$) and a second amount of silver (Ag);

depositing the first amount of germanium selenide ($Ge_xSe_{(1-x)}$) and the second amount of silver (Ag);

providing a third amount of silver selenide; and

depositing the third amount of silver selenide.

40. The process as defined in Claim 39, wherein the first amount of germanium selenide ($Ge_xSe_{(1-x)}$) and the second amount of silver (Ag) deposited form a layer that is in a range of about 250 Angstroms (Å) to about 1000 Å thick.

41. The process as defined in Claim 39, wherein the third amount of silver selenide is in a range of about 300 Angstroms (Å) to 1000 Å thick.

42. The process as defined in Claim 39, wherein the first amount of the germanium selenide ($Ge_xSe_{(1-x)}$) and the second amount of silver (Ag) are deposited separately, and where the first amount of germanium selenide ($Ge_xSe_{(1-x)}$) is deposited such that the deposited germanium selenide ($Ge_xSe_{(1-x)}$) lies between the deposited silver (Ag) and the deposited silver selenide.

43. A process of forming an active layer in a substrate assembly, where the active layer is capable of supporting the formation of conductive pathways in the presence of an electric field, the process comprising:

providing silver selenide and no other source of silver (Ag);

providing germanium selenide ($Ge_xSe_{(1-x)}$); and

forming the active layer by combining the silver selenide and the germanium selenide ($Ge_xSe_{(1-x)}$).

44. The process as defined in Claim 43, wherein x is in the range of about 0.2 to about 0.43.

45. The process as defined in Claim 43, wherein the process forms the active layer by combining the silver selenide and the germanium selenide ($Ge_xSe_{(1-x)}$) to a ratio within a range of about 1:1 to about 5:1 silver selenide to germanium selenide ($Ge_xSe_{(1-x)}$) by volume.

46. A memory device, comprising:

a memory body between a first and a second electrode, said memory body comprising a plurality of layers;

a first layer of said plurality of layers being silver selenide;

a second layer of said plurality of layers being germanium selenide;

a third layer of said plurality of layers being silver.