

WHAT IS CLAIMED IS:

1. An integrated circuit device comprising:

a substrate comprising a cell region and an extension region arranged along a horizontal direction;

a plurality of conductive layers stacked on the cell region in a vertical direction that is perpendicular to the horizontal direction, wherein the plurality of conductive layers extend onto the extension region and have a stair-step structure on the extension region; ~~and~~

a plurality of vertical structures on the substrate, wherein each of the plurality of vertical structures extends in the vertical direction, and the plurality of vertical structures comprise a first vertical structure on the cell region and comprise a second vertical structure and a third vertical structure on the extension region; ~~and~~

a dielectric layer on the stair-step structure of the plurality of conductive layers;

wherein the first vertical structure extends through the plurality of conductive layers and comprises a first channel layer,

wherein the second vertical structure is in the stair-step structure of the plurality of conductive layers and comprises a second channel layer, ~~and~~

wherein the second channel layer is spaced apart from the substrate in the vertical direction,

wherein the third vertical structure extends through the stair-step structure of the plurality of conductive layers, and

wherein the dielectric layer covers at least a portion of a top surface of the third vertical structure.

2. The integrated circuit device of claim 1, wherein the first channel layer directly contacts the substrate.

3. The integrated circuit device of claim 1 or claim 2, wherein the second vertical structure comprises a lower portion and an upper portion sequentially stacked on the substrate, and

wherein the lower portion of the second vertical structure has a unitary structure comprising an insulating material.

4. The integrated circuit device of claim 1 or claim 2, wherein the second vertical structure comprises a lower portion and an upper portion sequentially stacked on the substrate, and

wherein the lower portion of the second vertical structure is free of the second channel layer.

5. The integrated circuit device of any one of claims 1 to 4, wherein the plurality of vertical structures further comprises ~~a third vertical structure and~~ a fourth vertical structure on the extension region,

~~wherein the fourth vertical structure extends through the stair step structure of the plurality of conductive layers, and~~

wherein the fourth~~third~~ vertical structure overlaps the third~~fourth~~ vertical structure and is spaced apart from the third~~fourth~~ vertical structure in the vertical direction.

6. The integrated circuit device of claim 5, wherein the first vertical structure, the second vertical structure, and the third~~fourth~~ vertical structure are sequentially arranged along the horizontal direction, and

wherein a lowermost end of the second channel layer of the second vertical structure is at a first level, and an uppermost end of the third~~fourth~~ vertical structure is at a second level that is lower than the first level.

7. The integrated circuit device of claim 5 or claim 6, wherein the fourth~~third~~ vertical structure comprises a third channel layer, and

wherein the ~~fourth~~^{third} channel layer is spaced apart from the stair-step structure of the plurality of conductive layers in the vertical direction.

8. The integrated circuit device of any one of claims 1 to 4, wherein the plurality of vertical structures further comprises a ~~fourth~~^{third} vertical structure on the extension region, and the first vertical structure, the second vertical structure, and the ~~fourth~~^{third} vertical structure are sequentially arranged along the horizontal direction,

wherein the ~~fourth~~^{third} vertical structure ~~extends through the stair-step structure of the plurality of conductive layers and~~ comprises a third channel layer that is spaced apart from the substrate in the vertical direction, and

wherein a lowermost end of the second channel layer is at a first level, and a lowermost end of the third channel layer is at a second level that is lower than the first level.

9. An integrated circuit device comprising:

a substrate comprising a first region and a second region arranged along a horizontal direction;

a stack structure on the substrate, wherein the stack structure comprises a plurality of conductive layers stacked on the first region of the substrate in a vertical direction that is perpendicular to the horizontal direction, and wherein the plurality of conductive layers extend onto the second region of the substrate and have a stair-step structure on the second region of the substrate; ~~and~~

a plurality of vertical structures on the substrate, wherein each the plurality of vertical structures extends in the vertical direction; ~~;~~ and

a dielectric layer on the stair-step structure of the plurality of conductive layers, and

wherein the plurality of vertical structures comprise:

a first vertical structure that is on the first region of the substrate and extends through the plurality of conductive layers;

a second vertical structure that is on the second region of the substrate and extends through the stair-step structure of the plurality of conductive layers; ~~and~~

a third vertical structure that is on the second region of the substrate and extends through the stair-step structure of the plurality of conductive layers; and
wherein the dielectric layer covers at least a portion of a top surface of the third vertical structure~~overlaps and is spaced apart from the second vertical structure in the vertical direction.~~

10. The integrated circuit device of claim 9, wherein the first vertical structure comprises a first channel layer that directly contacts the substrate, and

wherein the second~~third~~ vertical structure comprises a second channel layer that is spaced apart from the substrate in the vertical direction.

11. The integrated circuit device of claim 10, wherein an uppermost end of the first channel layer and an uppermost end of the second channel layer are at an equal level.

12. The integrated circuit device of any one of claims 9 to 11, ~~wherein the plurality of vertical structures further comprises a fourth vertical structure extending through the stair-step structure of the plurality of conductive layers,~~

wherein the first vertical structure, the second vertical structure, and the third~~fourth~~ vertical structure are sequentially arranged along the horizontal direction, and

wherein an uppermost end of the second vertical structure is at a first level, and an uppermost end of the third~~fourth~~ vertical structure is at a second level that is lower than the first level.

13. An integrated circuit device comprising:

a substrate comprising a cell region and an extension region arranged along a horizontal direction;

a stack structure on the substrate, wherein the stack structure comprises a plurality of conductive layers stacked on the cell region in a vertical direction that is perpendicular to the

horizontal direction, and wherein the plurality of conductive layers extend onto the extension region and have a stair-step structure on the extension region; ~~and~~

a plurality of vertical structures on the substrate, wherein the plurality of vertical structures comprise a first vertical structure extending through the plurality of conductive layers on the cell region and comprise a second vertical structure and a third vertical structure extending through the stair-step structure of the plurality of conductive layers, wherein the second vertical structure comprises a lower portion and an upper portion sequentially stacked on the substrate, and wherein the upper portion of the second vertical structure comprises a material different from the lower portion of the second vertical structure; and

a dielectric layer on the stair-step structure of the plurality of conductive layers;

wherein the dielectric layer covers at least a portion of a top surface of the third vertical structure.

14. The integrated circuit device of Claim 13, wherein the first vertical structure comprises a first channel layer, and

wherein the upper portion of the second vertical structure comprises a second channel layer that is spaced apart from the substrate.

15. The integrated circuit device of Claim 14, wherein the lower portion of the second vertical structure has a unitary structure comprising an insulating material.

16. The integrated circuit device of Claim 13, wherein the first vertical structure comprises a first channel layer, and ~~a~~ lowermost end of the first channel layer is at a first level, and

wherein the second vertical structure comprises a second channel layer and ~~a~~ lowermost end of the second channel layer is at a second level that is higher than the first level.

17. The integrated circuit device of any one of claims 14 to 16, wherein the first channel layer directly contacts the substrate.

18. The integrated circuit device of any one of claims 14 to 17, wherein an uppermost end of the first channel layer and an uppermost end of the second channel layer are at an equal level.

19. The integrated circuit device of any one of claims 13 to 18, wherein a lowermost end of the upper portion of the second vertical structure has a first width in the horizontal direction, an uppermost end of the lower portion of the second vertical structure has a second width in the horizontal direction, and the second width is greater than the first width.

20. The integrated circuit device of any one of claims 13 to 19, wherein the upper portion of the second vertical structure and the lower portion of the second vertical structure are formed by different processes.