1298272

PATENT SPECIFICATION (11) 1298272

DRAWINGS ATTACHED

(21) Application No. 9876/70 (22) Filed 2 March 1970

(31) Convention Application No. 803920 (32) Filed 3 March 1969 in

(33) United States of America (US)

(45) Complete Specification published 29 Nov. 1972

(51) International Classification H03D 1/02//H03F 1/34

(52) Index at acceptance

H3T 1A1 1D 1R 2J 2RX 2T2X 2T2Z 2T3J 2T4 2W2 3J 3N 4A2 4A3 4C 4E2N 4G 4R 4X 5E 5S 5X

(54) DETECTOR CIRCUITS

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to signal modulation detector circuitry, and more particularly to integrated circuit configurations for providing detection of the amplitude modulation components of relatively high frequency intermediate frequency waves. Circuitry embodying the invention is particularly suitable for use as the video detector of television receivers.

In present day technology, integrated circuits are receiving increasing attention. Although there is published material concerning the use of integrated circuit devices in signal receivers such as television receivers, the actual use of such devices has been limited. In most cases, prior proposals for the circuitry to be integrated either involve the use of general purpose integrated circuit devices, or use lumped circuit design philosophy, both of which tend to require a large number of components; which cannot be satisfactorily incorporated in integrated circuit form, and hence must be provided externally of the chip. It is desirable to limit the number of external components for reasons of circuit economy and because of the packaging limitations in the number of external available terminals which can be conveniently and economically provided on an integrated circuit chip.

In the design of amplitude modulation detectors, such as video detectors for television receivers. It is desirable to provide direct coupling between the detector and a preceding intermediate frequency amplifier which may be located on the same integrated circuit chip. The reason for the direction coupling is to avoid the necessity for external connections between the two stages or for the integrations of a coupling capacitor or transformer which are not susceptible of economical fabrication using integrated circuit techniques. The direct coupling of an intermediate frequency amplifier to the detector then also presents a problem in that the detector is subjected to an undesirable direct current component which can adversely affect the detector performance. A further drawback is that the direct current component is translated through the detector to a succeeding low frequency amplifier which is desirably direct current coupled thereto, thereby limiting the signal exclusion range over which the detected signal may drive the amplifier. Apart from the direct coupling of the detector to the preceeding intermediate frequency amplifier, it is often desirable to provide a biasing current for the amplifier to improve the detected linearity. Such biasing current constitutes a direct current component in the detected signal which is not due to the signal.

It is therefore an object of the present invention to provide an improved detector configuration capable of linear, repeatable operation while providing detected video signals more independent of undesired d.c. components applied thereto.

According to one aspect of the present invention, there is provided a signal modulation detector circuit including: an input circuit for applying a signal modulated carrier wave and an unrelated direct voltage; an output circuit for deriving the modulation components of said carrier wave; a rectifier device coupled between said input and output circuits; a stabilization circuit for said rectifier device comprising: means coupled to said input circuit for deriving a direct voltage responsive to substantially only said unrelated direct voltage, and means for applying said derived direct voltage to said rectifier device.

According to a second aspect of this invention, there is provided an AM demodulator circuit for processing the a.c. component only

of a signal with an uncertain d.c. level while using d.c. interstage signal coupling, comprising a differential circuit with its inputs coupled to the signal by d.c. couplings and its output connected to the output of the circuit, one of the two couplings having low pass filter means and the other coupling having the rectifier device means bringing about the demodulation, furthermore comprising a d.c. cross-coupling from the low pass filtered coupling to the rectifier, whereby said uncertain d.c. level has minimal deleterious effect on the small-signal detection capabilities of the rectifier device.

In an embodiment of the invention, a circuit including a first rectifying junction is connected between a source of signal modulated carrier waves including an undesired direct current component and a utilization circuit for deriving the modulation components from the carrier wave. Another circuit responsive substantially only to the undesired direct current component and including the series connection of a second rectifying junction and a dynamic impedance element is connected across the source of carrier waves. An impedance element couples the terminals of the two rectifying junctions remote from the source of carrier waves to stabilize the bias current through the first rectifying junction. A feedback circuit is provided from the utilization means to the dynamic impedance element for varying the impedance thereof as an inverse function of detected signal amplitude.

These and other objects of the present invention will become clearer as reference is made to the following specification and figures in which:—

FIGURE 1 is a schematic diagram in block form of a portion of a television receiver.

FIGURE 2 is a schematic circuit diagram of a video detector according to this invention.

FIGURE 3 is a schematic circuit diagram of an integrated circuit configuration employing a detector according to this invention.

FIGURE 4 is a schematic diagram of a video processing integrated circuit chip, not to scale, showing related circuit configurations in block form.

FIGURE 1 shows a schematic circuit diagram, in block form, of a portion of a television receiver. Signals intercepted by an antenna 10 are applied to a tuner 11 which includes the radio frequency (RF) amplifier, mixer and local oscillator, necessary for selecting one of a plurality of television channels. Circuits, not shown, tuned to the intermediate frequency (IF) select and apply the resulting IF signals to a first IF amplifier 13. Additional selectivity is provided by a filter 12 connected between a first IF amplifying stage 13 and a second IF amplifying stage 14. The IF amplifying stage 14 is, as will be further described, a direct coupled wideband amplifier, included on an integrated circuit substrate.

The IF amplifier 14 is coupled to a video detector and amplifying circuit 15. The output signal from the video detector and amplifier 15 is utilized in a television receiver to drive the video signal amplifier 16, synchronizing circuitry 17 and AGC circuitry 18.

The stages described above are included in most conventional television receivers. The portion of the circuit included in the dashed rectangle 19 are included on a single integrated circuit chip. Such an integrated circuit device, constructed in accordance with known techniques, is described in our British Patent Specification 1285493.

As stated above, in the integrated circuit environment it is desirable to have a video detector 15, which requires no external connections to or from the integrated chip while exhibiting substantially linear detection of the video signals at the relatively low signal levels.

The ability of the detector to work linearly at low levels indicates that the IF signal, applied thereto to be detected, may be of relatively low voltage levels and power levels, as compared to the magnitude of such signals found in receivers, using present design philosophy.

Secondly, the complete inclusion of the video detector within or on the integrated circuit assembly eliminates the input connection thereto which would normally require at least one pin or connector terminal for interfacing with the external environment.

Thirdly, this location of the video detector on the integrated circuit assembly avoids the necessity of bringing the high level amplifier high frequency IF signal to an output terminal for interfacing with external circuitry.

FIGURE 2 shows a transistor 20 arranged in an emitter follower configuration to be utilized as a video detector. Transistor 20 has a collector electrode returned to a point of reference potential designated as $+V_{cc}$. The base electrode of transistor 20 is coupled to a source of video intermediate frequency IF signals, which also includes an undesirable d.c. component because of a direct coupling to the IF amplifier 14 shown in FIGURE 1. The emitter electrode of transistor 20 is coupled to a point of reference potential, such as ground, through a filtering or detector capacitor 21. Also coupled to the base electrode of transistor 20 is a series combination of a resistor 22 and capacitor 23 coupled between said base electrode and a point of reference potential.

The junction between resistor 22 and capacitor 23 is coupled to the base electrode

of a bias reference transistor 24. Transistor 24 is arranged in an emitter follower configuration having the collector electrode coupled to $+V_{cc}$ and the emitter electrode returned to ground through the collector to emitter path of a dynamic impedance element represented by modulated bias transistor 25. The emitter electrode of transistor 24 is coupled to the base electrode of transistor 26 functioning as part of a d.c. bias circuit. A resistor 36, for discharging the capacitor 21 is coupled between the emitter electrodes of transistors 20 and 24. Transistor 26 is also connected in an emitter follower configuration having the collector electrode returned to $+V_{cc}$. The emitter electrode of transistor 26 is coupled to ground through the series combination of a resistor 27 and the anode to cathode path of diode 28.

Diodes as 28, as utilized in the integrated circuit environment, are preferably collector to base shorted transistors. Such devices provide impedance matching and temperature stabilization for the transistors with which they are used.

The junction between resistor 27 and the anode of diode 28 is coupled to the base electrode of a transistor 29. Transistor 29 has its emitter electrode coupled to ground and its collector electrode coupled to the junction of a resistor 30 and the anode of a diode 31. The cathode of diode 31 is coupled to ground, while the opposite terminal of resistor 30 is coupled to the emitter electrode of a transistor 32, arranged in an emitter followed configuration, and having its base electrode directly coupled to the emitter electrode of the video detector transistor 20. The collector electrode of transistor 29, and therefore the junction between resistor 30 and the anode of diode 31 is connected to the base electrode of a video output transistor 33, having its emitter electrode coupled to ground and its collector electrode coupled to $+V_{cc}$ through a load resistor 35.

All of the above described circuit elements are incorporated on a single integrated circuit chip. The several emitter follower transistor configurations lend themselves to integrated circuit environments in that the area required on an integrated circuit substrate for the deposition of an emitter follower circuit is approximately five times less than that area required for the deposition of an alternate configuration such as a common collector or common base amplifier. Therefore utilization of the emitter follower to perform circuit functions results in enabling more circuit functions on a given size substrate.

In order to assure optimum detector linearity for relatively small video input signals, as applied to the base electrode of the video detector transistor 20, very small biasing currents must be utilized. Such small biasing currents may be of the order of magnitude of 5 to 50 micro-amperes. A detector circuit so biased, with the configuration shown, is capable of providing a detected output which will be linear for signals two times smaller than those capable of being detected by a conventional unbiased point contact diode detector.

Linear small signal operation of this detector is associated with low current bias plus a low impedance drive. Linear large signal operation is associated with the high input impedance of the emitter follower detector. The low impedance drive assures that the detector capacitor 21 will be charged to the peak value of low amplitude signals.

The low bias required for transistor 20 is associated with still another separate, although related consideration. Because the IF amplifier is d.c. coupled to the detector, the input signal to be detected by video detector transistor 20 also contains an undesired d.c. component which is some fraction of the supply potential $+V_{cc}$. Therefore the video detector transistor 20 must be stably biased for linear operation at relatively low current levels while being subjected to a d.c. component applied to its base electrode and derived from the IF output amplifier stage. In order to accomplish low current biasing of transistor 20, transistor 24 is employed to sense the d.c. voltage at the base of transistor 20 via resistor 22.

Resistor 22 in combination with capacitor 23 also provides filtering action at the base electrode of transistor 24 of a sufficient magnitude to remove the signal components from influencing the d.c. potential on the base electrode of transistor 24. To assure low emitter current in the transistor 20 and d.c. tracking, the low voltage drop across resistor 22 must be small; and the voltage drop across the base to emitter junction of transistor 24 must closely match the voltage drop across the base to emitter junction (V_{be}) of transistor 20. The above conditions as determined by the low bias currents in transistor 20, specify, in turn, that very low currents must flow through transistor 24. However, when a large signal is detected by transistor 20 a large voltage is developed across capacitor 21. This voltage is of a polarity in a direction tending to cutoff or reverse bias transistor 24 via resistor 36.

Accordingly, during a large signal condition the large current induced through resistor 36 would tend to reverse bias transistor 24 if the transistor 25 were not present. Transistor 25 derives a modulated base signal from the collector electrode of transistor 29, forming part of the biasing scheme as follows.

The d.c. voltage at the base electrodes of

transistors 20 and 24 are relatively equal and can be generally designated as V_{bl}. The voltage at the emitter electrode of transistor 20, is therefore $V_{bl}-V_{be}$, where V_{be} is the voltage drop across the base to emitter junction of transistor 20. Accordingly the voltage at the emitter electrode of transistor 32 would be $V_{bl}-2V_{be}$ assuming equal base to emitter voltage drops for transistors 20 and 32. In the same manner the voltage at the emitter electrode of transistor 26 is also approximately equal to $V_{bl}-2V_{be}$, further assuming that there is no significant d.c. drop across resistor 22, which assumption is valid as only small magnitude base current flows therethrough. However, there is actually a small potential difference between these stages of the order of magnitude of .01 to .05 volts, the lower potential being at the emitter electrode of transistor 24. This low potential difference specifies the biasing current for transistor 20 as that flowing through resistor 36.

If resistor 27 located in the emitter path of transistor 26, and resistor 30 located in the emitter path of transistor 32, are made approximately equal then the current flowing from the emitter of transistor 32 approximately equals the current flowing from the emitter of transistor 26. It can be seen that by biasing transistor 29, with reference to the voltage drop across diode 28 and the current flowing through resistor 27, transistor 29 will require as much collector current as is flowing through resistor 30. Therefore there can be no substantial current flow in diode 31, transistor 33 or transistor 25.

What is meant by no substantial current flow in the above description, is that the current flow through the devices is substantially small when compared to the total current flowing through resistor 30. Accordingly, the voltage across diode 31 is essentially the small current anode to cathode drop which is on the order of about .5 to .6 volts. The voltage at the collector of transistor 33 in this condition is approximately at $+V_{cc}$, due to the small base current.

As soon as signal is present, a voltage is detected across capacitor 21 due to the peak detection action of the capacitor 21 in conjunction with the base to emitter diode of transistor 20. The detected d.c. potential is applied to the base electrode of transistor 32 which increases its conduction and hence increases the amount of current flowing through resistor 30. The potential at the anode of diode 31 goes from the small current anode to cathode voltage to the large current anode to cathode voltage, which levels differ by approximately one tenth of a volt. However, due to the relatively low dynamic impedance of diode 31, compared to the relatively higher dynamic impedance, seen looking into the base of transistor 33, a smaller portion of the signal current flows through the base to emitter junction of transistor 33 causing the collector electrode potential of transistor 33 to decrease from $+V_{cc}$ towards ground. Depending upon the amount of signal current coupled to transistor 33 the collector voltage can exhibit a swing practically equivalent to the full $+V_{cc}$ supply. In this manner, irrespective, of the d.c. component existing at the base electrode of transistor 20, the collector electrode of transistor 33 can exhibit large voltage swings below V_{cc} towards ground. This operation is obtained for small IF signal levels superimposed on that d.c. component and applied to the base electrode, and of detector 20 as further coupled through the complete d.c. coupled amplifier configuration, described.

As indicated above, the base to emitter diode of transistor 25 is also coupled to the collector electrode of transistor 29, and receives a portion of the increased current through diode 31 due to signal conditions. This, then, causes transistor 25 to conduct in accordance with the magnitude of the detected signal amplitude. The conduction of transistor 25 assures that transistor 24 will not become back biased due to large signal levels which condition would otherwise upset the prearranged biasing levels. The detector circuit of FIGURE 2 is inherently temperature stable as the voltage drops across the base to emitter junctions of the transistors and those across the collector to base shorted diodes, in the schematic shown, serve to track with temperature. In summation the circuit described in FIGURE 2 provides linear detection of low level video signals, irrespective of a d.c. component applied with said signals; by functioning to effectively cancel the d.c. component from the output amplifying stage. Such cancellation is provided while maintaining a high gain to the detected video signals with voltage swings comparable to the magnitude of the d.c. operating supply.

FIGURE 3 shows a schematic circuit diagram showing those circuit elements incorporated in the integrated circuit device within the dashed rectangle of Figure 1. It includes the subject of our Application 9875/70 (Serial No. 1298271).

An input terminal 110 is coupled to the base electrode of a double emitter transistor 40 having the collector electrode returned to terminal 112, through a series resistor 41. An integrated zener diode 42 is connected between the collector electrode and ground and functions to provide decoupling and impulse noise current limiting. One emitter electrode of transistor 40 is coupled to the base electrode of transistor 46, arranged in a common emitter configuration, and returned to terminal 114 through resistor 45. A second

emitter electrode of transistor 40 is returned to terminal 114, through resistor 47, and is coupled to terminal 111, designated as AFC (automatic frequency control).

Common emitter stage transistor 46 has the collector electrode returned to terminal 112 through a load resistor 48 in series with the emitter to collector path of a transistor 49.

The collector electrode of transistor 46 is also coupled to the base electrode of a follower configuration employing transistor 50. The output emitter electrode of transistor 50 is returned to terminal 114 through a resistor 51 and is coupled to the base electrode of transistor 52. Transistor 52 has a split collector load comprising series resistors 53 and 54, the junction therebetween being connected to the base electrode of transistor 49. The emitter electrode of transistor 52 is returned to ground through a self biasing and degenerative feedback resistor 59, which is bypassed for high frequency by the series R-C network 60 enclosed within dashed lined rectangle.

The series R-C network 60 is provided by integrated circuit techniques by depositing a lossy capacitor on the integrated circuit substrate. The component within rectangle 60 represent the circuit equivalent of the lossy capacitor and frequency compensation is thereby provided by selecting the component to furnish approximately ten degrees of phase shift at the higher IF frequencies.

The above described circuit includes a two stage wideband IF amplifier utilizing negative feedback with direct coupling between stages. In operation, a source of potential is connected between terminals 112 and 114, with the more positive terminal of the source connected to terminal 112. Such a source may conveniently be regulated by suitable circuitry included on the integrated circuit substrate assembly, such as that described in the aforementioned US Patent 3564125.

The double emitter follower stage affords to isolate a selective filtering network, having a terminal coupled to terminal 110. This permits the filter to operative relatively unloaded so as not to adversely affect the desired bandpass. To assure further isolation the emitter follower including the emitter electrode 44 isolates the same selective network as operated with low IF signals from the automatic frequency control circuitry included in certain television receivers. The follower circuit including emitter electrode 43 drives the common emitter amplifier 46 which provides voltage gain for the low level IF signals in accordance with the impedance of the controllable collector load comprising resistor 48 in series with the collector to emitter path of transistor 49. The amplified IF signal is applied to the base of an emitter follower 50 which drives the common collector amplifier 52. A portion of the output of amplifier 52, i.e. that voltage appearing between the junction of resistors 53 and 54, is fed back to the base electrode of transistor 49 to maintain the gain of the above mentioned IF stage relatively constant. The negative feedback afforded by transistor 49 as controlled by the collector swing of transistor 52 serves to stabilize the IF amplifier operating performance and maintain the signal gain relatively constant within the IF frequency range. The negative feedback is important as the common emitter stage 52 is direct coupled to the base electrode of the video detector follower 65. The emitter follower 65 has a high input impedance which is subjected to relatively large variations according to the input signal applied. Therefore the video detector 65 reflects back a non-linear load to the collector electrode of the IF amplifier stage 52. This effect is compensated for by the negative feedback arrangement just described to maintain the IF gain constant in spite of the varying loading conditions. The output emitter electrode of follower transistor 65 operating as a video detector, has a capacitor 69 connected between the emitter electrode and terminal 114 or reference potential.

The video detector circuitry, to be described, is similar to that circuitry already described in FIGURE 2 but some actual integrated circuit problems will be described in greater detail. As indicated above an undesired direct voltage from the collector electrode of transistor 52 is applied to the base electrode of transistor 65 along with the IF signal when present. In order for transistor 65 to provide linear detection for low level signals it is desirable to stably bias the follower stage at low current levels for the base to emitter diode of transistor 65. Accordingly the direct voltage coupled from the collector electrode of transistor 52 is also applied to the base electrode of transistor 66 via a resistor 67. Resistor 67 in conjunction with capacitor 64, coupled from the base electrode of transistor 66 to ground, serves to bypass the IF video frequencies from the base electrode of transistor 66 to ground to thereby maintain the voltage at the base representative only of that d.c. component applied to the base electrode of transistor 65. Resistor 67 is selected of a magnitude so that there is no substantial voltage drop across the same, while being large enough so as not to load the IF amplifier 52. Therefore, the voltage at the emitter electrodes of transistors 65 and 66 are approximately equal. The emitter electrode of transistor 66 is coupled through resistor 67A to the base electrode of an emitter follower configuration including transistor 68 which corresponds to transistor 26 of FIGURE 2. In a similar manner the emitter electrode of tran-

sistor 65 is coupled to the base electrode of the follower transistor 70 through resistor 71. Resistor 71 serves with capacitor 72 as a selective filter for bypassing the 45 MHz signal, corresponding to the video IF carrier, from the base electrode of transistor 70. A capacitor 77 is coupled between the emitter electrodes of transistors 65 and 70. Capacitor 77 serves to bootstrap the signal when the R—C network of resistor 71 and capacitor 72, begins to roll-off; to maintain the follower action of transistor 70 at high frequencies. Transistor 70 performs similar to transistor 32 of FIGURE 2. Considering the various V_{be} drops, if resistor 73 in series with the emitter electrode of transistor 70, and resistor 74 in series with the emitter electrode of transistor 68 are made approximately equal, the current flowing through each resistor is approximately equal.

Transistor 75 is biased by means of a diode 76 which actually comprises a transistor with the collector connected to the base. The diode 76 is coupled between the base electrode of transistor 75 and ground so that transistor 75 emitter of collector current equals the current flowing through resistor 73. The collector electrode of transistor 75 is coupled to the base electrode of transistor 78 which functions in a manner similar to that of transistor 33 of FIGURE 2. Base voltage for transistor 78 which, in the absence of a.c. signal, operates close to cutoff, is developed across diode 79 coupled between the base electrode and the point of reference potential.

As described previously, the detected video signal charges capacitor 69, increasing the current flowing through resistor 73. Most of the increment of the current due to the detected video signal is returned to ground through diode 79 in parallel with the base electrode of transistor 78. Transistor 78 receives a corresponding amount of base current in relation to its dynamic impedance when compared to that dynamic impedance of the diode 79. This current transfer across the constant V_{be} drop of the diode, swings the collector of transistor 78 from B+ towards ground only upon the detection of the video signal. The output signal at the collector electrode of transistor 78 is therefore independent of the undesired d.c. component applied to the base electrode of transistor 65, even though the entire amplifier chain is d.c. coupled to maintain the detected d.c. component of the video signal. Transistor 80 and resistor 85 perform the equivalent functions as their counterparts transistor 25 and resistor 36, shown in FIGURE 2.

The large collector swing obtainable from the collector electrode of transistor 78 is isolated from an output terminal 116 on the integrated circuit substrate 100 by the pair of emitter follower circuits including transistors 81 and 82. The video signal swing at output terminal 116 is $2V_{be}$ less than the side swing at the collector electrode of transistor 78. The video signal available at terminal 116 is suitable for driving the sync and high level video amplifier stages which may be included within the television receiver. The magnitude of video swing available at terminal 116 is still a considerable portion of the V_{cc} supply as applied between terminals 112 and 114.

In order to further assure operating point stabilization with temperature changes, and to maintain large signal linearity, a d.c. loop is closed from the video detector circuitry back to the input terminal 110 associated with the IF amplifiers.

The d.c. feedback, is obtained via resistor 90, in series with the collector electrode of transistor 68 and terminal 112, and the zener diode 91, coupled between the collector electrode of transistor 68 and terminal 113.

A voltage appears across resistor 90 which is dependent upon the current flowing through transistor 68 and therefore through resistor 74. This current as, previously explained, is the bias reference current for the video detector output stages. The voltage is reduced in level by zener diode 91 action, which affords temperature compensation as well, and is eventually, as will be described with reference to FIGURE 4, applied to terminal 110 for controlling the quiescent bias of transistor 40.

FIGURE 4 shows a plan view, not to scale of an integrated circuit chip which includes the circuitry described in conjunction with FIGURE 3 plus additional circuitry described in our British Specification 1285493 noted hereinbefore. Filtering for IF bandwidth shaping is accomplished by a selective network 120 coupled between a first IF amplifier which is also included on the integrated circuit chip, although not described herein, and a second IF module including transistor 40, 46, 49, 50 and 52 of FIGURE 3. The output from the first IF amplifier is obtained at terminal 108 and is applied to the selective filter 120. Filter 120 contains suitable trap circuits for separating the sound IF carrier and for applying it to terminal 109 of the chip and therefrom to a second detecting and amplifying circuit also included on the chip and further described in the above noted Patent Specification 1285493.

A suitable terminal of the filter is likewise coupled to terminal 110 which as seen from FIGURE 3 is the input terminal to the emitter follower 40 of the IF amplifier described in conjunction with FIGURE 3. The filter network includes a d.c. path between terminal 110 and terminal 113 which path is generally represented by resistor 121 included within the selective filter network.

The signal at terminal 113 is representative of the d.c. reference current used for biasing the video detector portion of the circuitry described in FIGURE 3. The voltage at terminal 113, dependent upon this current, is feedback to the input terminal 110 to assure optimum biasing of the IF amplifier and video detector stage for maximum linear operation.

The IF carrier waves from the RF tuner are applied to the input of a selective network 122 located off the integrated circuit substrate. The filtered IF is applied to terminal 105 which is the input terminal of a first stage IF circuit included on this chip and described in said Specification 1285493.

An AGC signal is also developed on this chip for application to the input IF stage. The AGC signal is developed at terminal 103 and is applied through a filtering circuit 123 to the input terminal 105. An AGC signal to be applied directly to the tuner RF amplifier is also developed on the chip and is available at terminal 106. Our British Application 9873/70 (Serial No. 1290091) entitled "AUTOMATIC GAIN CONTROL CIRCUIT" describes the AGC circuit and operation in greater detail.

The termnial 107 on the chip is connected to an external current source reference used for establishing quiescent operating characteristics in the low level first IF stage (not shown) and necessary for determining the AGC delay characteristics of the same. Terminal 111, described in FIGURE 3, provides an IF signal for application to automatic frequency control circuitry. Terminal 101 is an output terminal for the 4.5 MHz sound signal generated on the chip and necessary for providing the audio portion of the television display. Terminal 102 is adapted to receive a horizontal keying pulse necessary for a keyed AGC operation. The demodulated and amplified video signal is derived from terminal 116. Coupled to terminal 116 is a "tee" network including the tapped inductor 125 having its end terminals shunted by a capacitor 126. The tap of inductor 125 is referenced to ground through a voltage divider comprising resistors 126 and 127. Resistor 127 is shunted by a capacitor 128. The signal at the junction between resistors 126 and 127 is used to drive the synchronizing signal separator circuits and provides the video signal containing the synchronizing component necessary for sync separator operation. In a color receiver the output terminal of the inductor 125 is coupled to the video amplifier channel and to a chroma channel. The main function of the tee network is to drop the 4.5 MHz sound carrier and to provide impedance matching between the integrated circuit chip and the video channel delay line, as well as the chroma stage for a color receiver.

WHAT WE CLAIM IS:—

1. A signal modulation detector circuit including: in an input circuit for applying a signal modulated carrier wave and an unrelated direct voltage; an output circuit for deriving the modulation components of said carrier wave; a rectifier device coupled between said input and output circuits; a stabilization circuit for said rectifier device comprising: means coupled to said input circuit for deriving a direct voltage responsive to substantially only said unrelated direct voltage, and means for applying said derived direct voltage to said rectifier device.

2. A circuit as claimed in claim 1 wherein the rectifier device is a first transistor in emitter follower configuration, a first resistance connects its emitter to the emitter of a second, emitter follower, transistor used for deriving said direct voltage, an impedance connects the emitter of the second transistor to a reference potential, and a low pass filter connects said input circuit to the base of said second transistor.

3. A circuit as claimed in claim 2 wherein said impedance element comprises the collector-to-emitter current path of a third transistor.

4. A circuit as claimed in claim 3 wherein the third transistor has its collector connected to the emitter of the second transistor, its emitter connected to a common terminal, and its base connected to said output circuit.

5. A circuit as claimed in claim 4 comprising second means coupled to the rectifier output for providing an output current dependent on the unrelated direct voltage plus a current dependent on the intelligence, means coupled to the previous means for by-passing the unrelated DC voltage while directing the intelligence portion through a second path.

6. A circuit as claimed in claim 5 wherein the last means includes a fourth transistor having its emitter coupled to reference, a diode coupling the base of the fourth transistor and the reference potential, and similarly directed to the emitter/base diode part thereof, a second resistor coupling the base of the fourth transistor to the second transistor output, a third resistor equal to the second resistor coupled between the collector electrode of said fourth transistor and the emitter output, whereby the current is the same through the second and third resistors and also the same current flows through the diode and said fourth transistor, wherein a second diode is coupled between the collector of said fourth transistor and the same reference potential, for producting any current derived from the rectifier and denoting intelligence.

7. A circuit as claimed in claim 6 for video detection, comprising a first capacitor

The signal at terminal 113 is representative of the d.c. reference current used for biasing the video detector portion of the circuitry described in FIGURE 3. The voltage at terminal 113, dependent upon this current, is feedback to the input terminal 110 to assure optimum biasing of the IF amplifier and video detector stage for maximum linear operation.

The IF carrier waves from the RF tuner are applied to the input of a selective network 122 located off the integrated circuit substrate. The filtered IF is applied to terminal 105 which is the input terminal of a first stage IF circuit included on this chip and described in said Specification 1285493.

An AGC signal is also developed on this chip for application to the input IF stage. The AGC signal is developed at terminal 103 and is applied through a filtering circuit 123 to the input terminal 105. An AGC signal to be applied directly to the tuner RF amplifier is also developed on the chip and is available at terminal 106. Our British Application 9873/70 (Serial No. 1290091) entitled "AUTOMATIC GAIN CONTROL CIRCUIT" describes the AGC circuit and operation in greater detail.

The termnial 107 on the chip is connected to an external current source reference used for establishing quiescent operating characteristics in the low level first IF stage (not shown) and necessary for determining the AGC delay characteristics of the same. Terminal 111, described in FIGURE 3, provides an IF signal for application to automatic frequency control circuitry. Terminal 101 is an output terminal for the 4.5 MHz sound signal generated on the chip and necessary for providing the audio portion of the television display. Terminal 102 is adapted to receive a horizontal keying pulse necessary for a keyed AGC operation. The demodulated and amplified video signal is derived from terminal 116. Coupled to terminal 116 is a "tee" network including the tapped inductor 125 having its end terminals shunted by a capacitor 126. The tap of inductor 125 is referenced to ground through a voltage divider comprising resistors 126 and 127. Resistor 127 is shunted by a capacitor 128. The signal at the junction between resistors 126 and 127 is used to drive the synchronizing signal separator circuits and provides the video signal containing the synchronizing component necessary for sync separator operation. In a color receiver the output terminal of the inductor 125 is coupled to the video amplifier channel and to a chroma channel. The main function of the tee network is to drop the 4.5 MHz sound carrier and to provide impedance matching between the integrated circuit chip and the video channel delay line, as well as the chroma stage for a color receiver.

WHAT WE CLAIM IS:—

1. A signal modulation detector circuit including: in an input circuit for applying a signal modulated carrier wave and an unrelated direct voltage; an output circuit for deriving the modulation components of said carrier wave; a rectifier device coupled between said input and output circuits; a stabilization circuit for said rectifier device comprising: means coupled to said input circuit for deriving a direct voltage responsive to substantially only said unrelated direct voltage, and means for applying said derived direct voltage to said rectifier device.

2. A circuit as claimed in claim 1 wherein the rectifier device is a first transistor in emitter follower configuration, a first resistance connects its emitter to the emitter of a second, emitter follower, transistor used for deriving said direct voltage, an impedance connects the emitter of the second transistor to a reference potential, and a low pass filter connects said input circuit to the base of said second transistor.

3. A circuit as claimed in claim 2 wherein said impedance element comprises the collector-to-emitter current path of a third transistor.

4. A circuit as claimed in claim 3 wherein the third transistor has its collector connected to the emitter of the second transistor, its emitter connected to a common terminal, and its base connected to said output circuit.

5. A circuit as claimed in claim 4 comprising second means coupled to the rectifier output for providing an output current dependent on the unrelated direct voltage plus a current dependent on the intelligence, means coupled to the previous means for by-passing the unrelated DC voltage while directing the intelligence portion through a second path.

6. A circuit as claimed in claim 5 wherein the last means includes a fourth transistor having its emitter coupled to reference, a diode coupling the base of the fourth transistor and the reference potential, and similarly directed to the emitter/base diode part thereof, a second resistor coupling the base of the fourth transistor to the second transistor output, a third resistor equal to the second resistor coupled between the collector electrode of said fourth transistor and the emitter output, whereby the current is the same through the second and third resistors and also the same current flows through the diode and said fourth transistor, wherein a second diode is coupled between the collector of said fourth transistor and the same reference potential, for producting any current derived from the rectifier and denoting intelligence.

7. A circuit as claimed in claim 6 for video detection, comprising a first capacitor

shunting the base of the second transistor to reference potential, a fourth resistor connecting the bases of the first and second transistors, the base of the latter being thus low pass filtered, and a second capacitor shunting the rectifier output, to remove carrier from the video intelligence and the direct voltage.

8. A circuit as claimed in claim 1 comprising a first point to which the composite signal is to be applied, a first low-pass filter means connected to said first point and providing to a second point a second direct voltage component substantially free of the carrier wave component and directly dependent upon the direct voltage component, the rectifier device and a first resistance element connected in series combination coupling said first and second points, a second low-pass filter means connected to the junction of said rectifier device and the first resistive element and providing to a third point a filtered rectified intelligence signal superimposed upon a third direct component directly dependent upon said first and second direct voltage components, and a differential amplifier having its inputs each connected to a different one of said second and third points and providing at its output a filtered rectified intelligence.

9. A circuit as claimed in claim 8, comprising first and second transistors each having base, emitted and collector electrodes; the base electrode of said first transistor being identifiable with said first point, the emitter electrode of said first and second transistors being identifiable with said third and second points respectively, a fourth point for application of energizing potential to which each of said collector electrodes are coupled, a fifth point for application of reference potential; said first low-pass filter means comprising a (fifth) resistor coupling the base electrode of said second transistor to said first point, a first capacitor or coupling the base electrode of said second transistor to said fifth point, and said second transistor used as an emitter-follower; said rectifier device comprising the base-emitter current path of said first transistor; said resistive element comprising a (first) resistor linking the emitter electrodes of said first and second transistors; said second low-pass filter means comprising a second capacitor coupling the emitter electrode of said first transistor to said fifth point, and an impedance element coupling said second and fifth points.

10. A circuit as claimed in claim 9, comprising a third transistor having base, emitter and collector electrodes, said impedance element corresponding to the collector-emitter current path of said third transistor, and the base electrode of said third transistor being direct current coupled to a signal proportional to the signal at said differential amplifier output, thereby causing said second capacitor to be discharged in accordance with the amplitude of said filtered rectifier intelligence.

11. A circuit as claimed in claim 10 where said differential amplifier comprises fourth, fifth, sixth and seventh transistors each having base, emitter and collector electrodes; first and second semiconductor diode devices each having anode and cathode electrodes; third and fourth resistors having similar resistance values; and signal utilization means, the collector electrodes of said fourth and fifth transistors each being coupled to said fourth point, the base electrode of said fourth and fifth transistors being respectively coupled to said second and third points, the emitter electrodes of said sixth and seventh transistors being connected to said fifth point, the anode and cathode electrodes of said first semiconductor diode device each being connected to a different one of the base and emitter electrodes of said sixth transistor and poled between said connections similarly to the base-emitter junction also therebetween of said sixth transistor, the anode and cathode electrodes of said second semiconductor diode device each being connected to a different one of the base and emitter electrodes of said seventh transistor and poled between said connections similarly to the base-emitter junction also therebetween of said seventh transistor, the collector electrode of said sixth transistor being connected to the base electrode of said seventh transistor, said third resistor coupling the base electrode of said sixth transistor to the emitter electrode of said fourth transistor, said fourth resistor coupling the base electrode of said seventh transistor to the emitter of said fifth transistor, and the collector electrode of said seventh transistor providing said differential amplifier output and being coupled to said fourth point by signal utilization means.

12. A circuit as claimed in claim 11 wherein each of said semiconductor diode devices is formed from a transistor having collector and base electrodes connected in common corresponding to one diode device electrode and an emitter electrode corresponding to the other.

13. A signal modulation detector as claimed in any of claims 8—12 in which said transistors, said semiconductor diode devices, and said resistors are all disposed in a single integrated circuit.

14. A circuit as claimed in claim 13, in which said capacitors are also disposed in said single integrated circuit.

15. A circuit as claimed in claim 13 or 14 comprising said signal utilization means comprising a further resistor disposed in said single integrated circuit.

16. An AM demodulator circuit for processing the a.c. component only of a signal

with an uncertain d.c. level while using d.c. interstage signal coupling, comprising a differential circuit with its inputs coupled to the signal by d.c. couplings and its output connected to the output of the circuit, one of the two couplings having low pass filter means and the other coupling having the rectifier device means bringing about the demodulation, furthermore comprising a d.c. cross-coupling from the low pass filtered coupling to the rectifier, whereby said uncertain d.c. level has minimal deleterious effect on the small-signal detection capabilities of the rectifier device.

17. A circuit as claimed in claim 16 having said d.c. cross-coupling from the emitter of an emitter follower in said low pass filtered coupling, and, to minimize reaction on the emitter follower via said cross-coupling due to the intelligence signal arising from AM detection operation, a reverse coupling from the differential circuit output to the base of a further transistor rectifier, which influences the emitter impedance of said emitter follower by means of the emitter/collector path of the further transistor.

18. A circuit as claimed in claim 17 wherein the differential circuit comprises a transistor to shunt the output of said other coupling to reference potential and arranged to take a current representing said uncertain d.c., by means of an input diode across its emitter and base, and comprises a further diode connected to the output of said other coupling and itself connected across the emitter and base of an output transistor.

19. A detector circuit substantially as described in conjunction with Figure 2, or Figures 2 and 3, or Figures 2, 3 and 4 of the accompanying drawings.

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Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1972.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

