

A Bi-directional Current Switching Circuit for a Load

Field of the Invention

5 This invention relates to a bi-directional current switching circuit for a load, and particularly, though not exclusively, to such a circuit for use in a preamplifier write driver circuit for use in magnetic storage systems to drive an inductive head for writing on a magnetic storage medium.

Background of the Invention

10 In magnetic disc storage systems, the information stored on the magnetic disc depends on the polarization state of each individual bit on the disc surface. The write driver circuit is connected to two terminals of the inductive head, which contains an inductive coil. During a write operation, a large current is delivered
15 from the writer circuit through the inductive coil thereby generating a magnetic field, which magnetizes an individual bit on the adjacent disc in a selected direction. The direction of the polarisation is controlled by the selection of the direction in which current flows through the inductive coil. Therefore, the rate of writing
20 information onto a disc depends upon the speed at which the current direction through the inductive coil can be switched.

A well-known prior-art write driver circuit 1 is shown in FIG. 1. It is formed in an H-bridge configuration with top switchable current sources 2 and 3 being coupled between an upper voltage
25 V_{dd} supply line 4 and either side of the inductive head 5 and bottom switches 6 and 7 coupled between either side of the inductive head 5 and a ground reference line 8. Differential data signals are applied to switch the two current sources 2 and 3 ON and OFF in opposite phase, with the two switches 6 and 7 similarly being controlled by a
30 differential data signal to be turned ON and OFF in opposite phases, such that the current I_{U1} flows in one direction through the inductive head 5 whenever current source 2 and the corresponding switch 7 are turned ON and the current I_{U2} flows through the inductive head 5 in the opposite direction when the current source 3
35 and the corresponding switch 6 are turned ON. It will, of course, be appreciated that the top current sources could be replaced by switches and the bottom switches by current sinks.

The speed at which the inductive head can write on the disc can be explained with reference to the following relationship:

$$di/dt = V_h/L_h$$

where di/dt is the rate of change of current with time across the inductive coil, V_h is the available voltage swing across the coil, and L_h is the inductance of the coil.

It can be seen that for fast rise and fall times, the writer should have (1) a higher supply voltage, (2) reduced head inductance and (3) a large effective head voltage. These are the first order assumptions as adopted in prior art circuits. However, second-order effect such as base-storage charge effect can also degrade the turn-off time of bipolar devices and with variations in process and design parameters, the switching speed of the write driver circuit can vary significantly.

In US Patent No. 5,132,852 there is disclosed an inductive head read/write preamplifier circuit in which the core write circuit is composed of a first top pair of transistors, acting as switches, and a second bottom pair of transistors coupled to a current source, acting as the current sources, with the inductive head coupled between the junctions between the two pairs of transistors. The rest of the circuit (except for the reading part of the circuit) is mainly for biasing, level-shifting and driving the output transistors. This circuit has several disadvantages: firstly, the stack structure reduces the available voltage applied across the head coil, so that the head voltage is very small, being particularly pronounced in low-voltage (for example, 5V) applications, and secondly, the voltage spikes induced across the head terminals could cause breakdown of the base-emitter junctions of the bipolar transistors, since due to heavy doping in the base-emitter region, the breakdown voltage is around 6V.

The head voltage swing and bipolar transistor break-down problems have been solved using an H-bridge configuration, as disclosed in US Patent Nos. 5,287,231 and 5,291,347. This implementation is based on the architecture described above with reference to FIG. 1. In this case, the fundamental H-bridge circuit is made up of bipolar transistors, current sources and Schottky transistors, where the Schottky transistors are used to improve both turn-on and turn-off times, and complementary Pseudo Emitter-

Coupled Logic (PECL) differential-pair circuits are used to drive the head by turning ON or OFF the individual output transistors. Furthermore, base current compensation plus degenerated current mirrors are used to control the precision of the circuit. In addition,
5 the head terminals are connected to the collectors of transistors, which does not impose any potential breakdown problem due to the flyback voltage of the inductive coil. Thus, this structure displays higher speed and can be operated at lower supply voltage.

Although Schottky bipolar transistors are very useful for
10 high-speed switching, they do require a more complicated and expensive manufacturing process, whereas replacing the Schottky bipolar transistor by a standalone bipolar transistor would be inferior in switching characteristics. However, the switching speed of a bipolar transistor is related to the excess base storage time
15 which is, on the other hand, a strong function of biasing current. It is particularly pronounced if the bias current is changed according to the change in head current. Using a MOS transistor as an alternative switch would eliminate this drawback but the high-swing requirement to turn OFF the switch would restrict its scope in high
20 frequency operation.

A known structure using a BICMOS process is shown in US Patent No. 5,386,328. In this structure, the top switches are implemented using PMOS transistors, and the current sinks are based on bipolar transistors. The ON and OFF states of the current
25 sinks are controlled by turning OFF or ON Schottky transistors by diverting the currents. This approach yields similar levels of head voltage swing as that in the structure disclosed in US Patent Nos. 5,287,231 and 5,291,347.

Brief Summary of the Invention

30 The present invention therefore seeks to provide a bi-directional current switching circuit for a load which overcomes, or at least reduces the above-mentioned problems of the prior art.

Accordingly, in a first aspect, the invention provides a bi-directional current switching circuit for a load, the circuit comprising
35 a differential output having first and second output terminals for connection to the load, a first current source circuit coupled between a first power supply line and the first output terminal and being coupled to a first input terminal, a second current source circuit

coupled between the first power supply line and the second output terminal and being coupled to a second input terminal, a third current source circuit coupled between the first output terminal and a second power supply line and being coupled to a third input terminal, a fourth current source circuit coupled between the second output terminal and the second power supply line and being coupled to a fourth input terminal, the first and second input terminals receiving a first differential current switching control signal for switching the first and second current source circuits in anti phase and the third and fourth input terminals receiving a second differential current switching control signal for switching the third and fourth current source circuits in anti phase, whereby the first and fourth current source circuits are switched on and off together and the second and third current source circuits are switched off and on together.

In one embodiment, the first, second, third and fourth current source circuits are preferably formed by first, second, third and fourth current mirror circuits, respectively. Preferably, each current mirror circuit comprises a first MOS transistor having a source coupled to a supply terminal, a drain coupled to an output terminal and a gate and a second MOS transistor having a source coupled to a supply terminal, a drain coupled to an input terminal and a gate coupled to its drain and to the gate of the first MOS transistor.

In a preferred embodiment, each current mirror circuit preferably further comprises a resistor coupled the gate and the drain of the second MOS transistor.

Conveniently, the first and second current mirror circuits can be formed of PMOS transistors and the third and fourth current mirror circuits can be formed of NMOS transistors.

Preferably, a fifth current mirror circuit is coupled between the first power supply line and the fourth input terminal and being coupled to the first input terminal and a sixth current mirror circuit is coupled between the first power supply line and the third input terminal and being coupled to the second input terminal.

The fifth current mirror circuit preferably comprises a first MOS transistor having a source coupled to the first supply terminal, a drain coupled to the fourth input terminal and a gate coupled to the second MOS transistor of the first current mirror circuit.

Similarly, the sixth current mirror circuit preferably comprises a first MOS transistor having a source coupled to the first supply terminal, a drain coupled to the third input terminal and a gate coupled to the second MOS transistor of the second current mirror circuit.

In a second aspect, the invention provides an inductive head writer circuit comprising a current switching circuit as defined above, an inductive head, a current bias generator circuit and a differential pair predriver circuit, wherein the inductive head is coupled between the first and second output terminals of the current switching circuit, the differential pair predriver circuit comprises first and second bipolar transistors, the first bipolar transistor having a base coupled to a first data terminal, a collector coupled to the first input terminal of the current switching circuit and an emitter coupled to the current bias generator circuit and the second bipolar transistor having a base coupled to a second data terminal, a collector coupled to the second input terminal of the current switching circuit and an emitter coupled to the current bias generator circuit.

Brief Description of the Drawings

Several embodiments of the invention will now be more fully described, by way of example, with reference to the drawings, of which:

FIG. 1 is a schematic illustration of a conventional H-switch write driver architecture;

FIG. 2 is a circuit diagram of a conventional H-switch write driver architecture similar to that of FIG. 1;

FIG. 3 is a schematic illustration of an H-switch write driver architecture according to one embodiment of the invention;

FIG. 4 is a schematic illustration of an H-switch write driver architecture similar to that of FIG. 3;

FIG. 5 is a circuit diagram of an embodiment of the present invention;

FIG. 6 is a circuit diagram of a preferred, second embodiment of the present invention; and

FIG. 7 is a circuit diagram of a third embodiment of the present invention.

Detailed Description of the Drawings

Thus, FIG. 2 shows a practical example of implementing the prior art architecture using BiCMOS technology instead of bipolar technology. In this case, the write driver circuit 10 includes a current bias generator circuit 20, a predriver circuit 30 and a driver circuit 40, with data input terminals 11 and 12, output terminals 13 and 14 and supply terminals 15 and 16 at V_{dd} and ground, respectively. A load, for example an inductive head 5 of a magnetic storage system, shown as comprising inductive coil 18 and damping resistor 19, is coupled to the differential output terminals 13 and 14.

The current bias generator 20 is coupled to the predriver 30 and supply terminals 15 and 16. The predriver 30 is coupled to supply terminal 15 and the driver 40 and the driver 40 is coupled to the predriver 30, supply terminals 15 and 16 and the output terminals 13 and 14.

The current bias generator 20 consists of a current source 21 and an emitter-degenerated precision current mirror 22 formed by NPN transistors 23, 24, 25 and resistors 26 and 27. The first terminal of current source 21 is coupled to V_{dd} supply terminal 15. The second terminal of current source 21 is coupled to the base of transistor 25 and the collector of transistor 24. The collector of transistor 25 is coupled to the V_{dd} supply terminal 15 and the base is coupled to the second terminal of current source 21. The emitter of transistor 25 is coupled to the bases of transistors 23 and 24. The emitters of transistors 23 and 24 are coupled to first terminals of resistors 26 and 27, respectively and the second terminals of resistors 26 and 27 are coupled to ground terminal 16. The collector of transistor 23 is coupled to the predriver 30.

The predriver 30 includes two NPN transistors 31 and 32 and two PMOS transistors 33 and 34. The data input terminal 11 is coupled to the base of transistor 31 and the data input terminal 12 is coupled to the base of transistor 32. The emitters of transistors 31 and 32 are both coupled to the collector of transistor 23 in the current bias generator 20. V_{dd} supply terminal 15 is connected to the sources of transistors 33 and 34. The drain of transistor 33 is coupled to its gate, the collector of transistor 31 and to the driver 40. Similarly, the drain of transistor 34 is coupled to its gate, the collector of transistor 32 and the driver 40.

The driver 40 includes two NPN transistors 41 and 42, two resistors 43 and 44 and four PMOS transistors 45, 46, 47 and 48. The sources of PMOS transistors 45, 46, 47 and 48 are coupled to the V_{dd} supply terminal 15. The gates of transistors 45 and 46 are
5 coupled to the drain of transistor 33 in predriver 30, whilst the gates of transistors 47 and 48 are coupled to the drain of transistor 34. The collector of transistor 41 is coupled to the output terminal 13 and the collector of transistor 42 is coupled to the other output terminal 14. The bases of transistors 41 and 42 are coupled to first
10 terminals of resistors 43 and 44, respectively. The emitters of transistors 41 and 42 and the second terminals of resistors 43 and 44 are coupled to the ground terminal 16.

The current source 21 is controlled by a bias circuit (not shown). The transistor 25 is used to improve the precision of the
15 current mirror formed by transistors 23 and 24, whereas the emitter resistors 26 and 27 improve the matching characteristic and stability of the current mirror formed by transistors 23 and 24. The bias current coupled to the predriver 30 is thereby given as:

$$I_{23} = (R_{27}/R_{26}) * I_{21}$$

20 where I_{23} is the current through transistor 23 coupled to predriver 30;

R_{27} is the resistance of resistor 27;

R_{26} is the resistance of resistor 26; and

I_{21} is the current from current source 21.

25 This tail current I_{23} is steered by the data inputs 11 and 12 to generate differential voltages across the self-biased PMOS transistors 33 and 34 by the Pseudo Emitter-Coupled Logic (PECL) transistor pair 31 and 32. These differential voltages are coupled to the transistors 45, 46, 47 and 48 with a ratio M. Thus, the current-
30 mirrors formed by transistors 33 and 46 and transistors 34 and 47 form top current sources. Due to the differentially-driven signals, one of the top current sources is ON when the other is OFF. Similarly, the currents in the two current mirrors formed by transistor pair 33 and 45 and transistor pair 34 and 48 are switched
35 to drive the base resistors 43 and 44, respectively. Therefore, differential voltages established across the resistors 43 and 44 will turn one of the bipolar voltage switches formed by transistors 41 and 42 ON and the other OFF. These voltage switches are switched

in such a way that either transistors 46 and 42 are ON while transistors 47 and 41 are OFF or transistors 46 and 42 are OFF while transistors 47 and 41 are ON. Based on the resistor ratio (R_{27}/R_{26}) and PMOS current mirror ratio ($M/1$), the write current I_w would be:

5
$$I_w = (R_{27}/R_{26}) * M * I_{21}.$$

This equation indicates the relationship between the write current and design parameters. In addition, the maximum head voltage of this circuit is approximately:

$$V_h = V_{dd} - V_{DSp} - V_{CEn}$$

10 where V_{DSp} is the saturation voltage of the PMOS transistor, V_{CEn} is the saturation voltage of the NPN transistor. This is a low-stack H-switch structure which is dedicated for speed enhancement by maximising the head voltage across the inductive head.

The embodiment of the present invention to be described
15 below contributes improvements by reducing sensitivity to design and process parameters by using an entire CMOS output driving stage operated in current-mode domain. It should be mentioned that the small swing in current-mode circuit is particularly useful in high-speed circuit design. FIG. 3 shows an embodiment of the
20 invention in simplified form. When compared with FIG. 1, it can be seen that the bottom voltage switches 6 and 7 are replaced by switchable current source circuits 50 and 51 providing current flows I_{D1} and I_{D1} , respectively. This write driver circuit exhibits low sensitivity to switching speed with variation in design and process
25 parameters. The write driver circuit is powered at 5V and can be operated down to 3.3V applications. As shown in FIG. 4, it is based on PECL current-steering techniques in association with CMOS current mirrors configured in a high-speed complementary push-pull H-switch. These complementary current mirrors are
30 synchronized with each other.

Thus, the write driver circuit 52 is made up of a basic differential pair circuit 53, a pair of multiple current mirror circuits 54 and 55, a pair of single current mirror circuits 56 and 57 with the inductive head 5 connected between the two arms formed by
35 connections between corresponding multiple and single current mirror circuits. The differential data is input at data terminals 58 and 59 to the differential pair circuit 53 causing one branch of the differential pair circuit to be current-steered. This current is

amplified by the multiple current mirror circuit for sourcing. The single current mirror circuit is arranged in a synchronized way to sink the respective head current. The magnitude of the write current is arranged to be proportional to the bias current of the differential pair circuit. Programming the bias current therefore controls the magnitude of the write current through the inductive head 5. A circuit implementation of this embodiment is shown in FIG. 5, in which identical components to those of the prior art circuit described with reference to FIG. 2 have the same reference numerals.

Thus, referring to FIG. 5, the write driver circuit 60 includes the current bias generator circuit 20, a differential pair predriver circuit 53 and a driver circuit 70, with data input terminals 58 and 59, output terminals 61 and 62 and supply terminals 15 and 16. The inductive head 5 is coupled to the differential output terminals 61 and 62. It is composed of inductive coil 18 together with damping resistor 19, as previously described.

The current bias generator circuit 20 is identical to that described with reference to FIG. 2 and will not be described further. Similarly, the differential pair predriver circuit 53 is identical to predriver circuit 30 and will not be further described.

The driver circuit 70 includes four NMOS transistors 71, 72, 73 and 74, as well as the four PMOS transistors 45, 46, 47 and 48, which are the same as in FIG. 2 having their sources coupled to the supply terminal 15. As before, the gates of transistors 45 and 46 are coupled to the drain of transistor 33 in differential pair predriver circuit 53, whilst the gates of transistors 47 and 48 are coupled to the drain of transistor 34. The drain of transistor 72 is coupled to the output terminal 61. Similarly, the drain of transistor 73 is coupled to the other output terminal 62. The gates of transistors 71 and 72 are coupled to the drain of transistor 71 and to the drain of PMOS transistor 48. Similarly, the gates of transistors 73 and 74 are coupled to the drain of transistor 74 and to the drain of PMOS transistor 45. The sources of all the NMOS transistors 71, 72, 73 and 74 are coupled to ground terminal 16.

As before, the bias current coupled to the differential pair predriver circuit 53 is given by:

$$I_{23} = (R_{27}/R_{26}) * I_{21}$$

This tail current I_{23} is steered by the data inputs 58 and 59 to generate differential voltages across the self-biased PMOS transistors 33 and 34 by the Pseudo Emitter-Coupled Logic (PECL) transistor pair 31 and 32. These differential voltages are coupled to the transistors 46 and 47 with a ratio M and to transistors 45 and 48 with a ratio N . Thus, the current-mirrors formed by transistors 33 and 46 and transistors 34 and 47 form top current sources. Due to the differentially-driven signals, one of the top current sources is ON while the other is OFF. Similarly, the currents in the PMOS-type current-mirrors formed by transistor pair 33 and 45 and transistor pair 34 and 48 are switched to drive the bottom NMOS-type current mirrors formed by transistor pair 71 and 72 and transistor pair 73 and 74, respectively. Thus, it will be appreciated that the current mirrors formed by transistors 33, 45 and 46 form the multiple current mirror circuit 54, the current mirrors formed by transistors 34, 47 and 48 form the multiple current mirror circuit 55, the current mirror formed by transistors 71 and 72 form the single current mirror circuit 56 and the current mirror formed by transistors 73 and 74 form the single current mirror circuit 57. Thus the bi-directional current switching to the floating load (inductive coil 18 in parallel with damping resistor 19) is either in one direction with current mirror circuits 54 and 57 ON, while current mirror circuits 55 and 56 are OFF or in the other direction with current mirror circuits 54 and 57 OFF, while current mirror circuits 55 and 56 are ON. The lower NMOS current mirror transistor pairs 71, 72 and 73, 74 sink the same amount of write current from that of their PMOS counterparts. If the copy ratio is N for transistor 45 with respect to transistor 33 and transistor 48 with respect to transistor 34, the ratio for transistor 72 and transistor 73 are (M/N) times transistor 71 and transistor 74. The write current floating via the load is given by:

$$I_w = (R_{27}/R_{26}) * M * I_{21}.$$

Moreover, the maximum head voltage of this structure is approximately:

$$V_h = V_{dd} - V_{DSp} - V_{DSn}$$

where V_{DSn} is the saturation voltage of the NMOS transistor. This shows that this is also a low-stack structure which is comparable with the prior-art low-stack circuits.

The use of top and bottom current source circuits in an H-switch configuration is different from the prior art circuits using top current source circuits and bottom voltage switch circuits. In the prior art, the voltage switch circuits are biased in saturation when
5 bipolar devices are used and non-saturation when MOS devices are used. However, in the present embodiment of the invention, the top and bottom current source circuits are biased in saturation. It will be appreciated that because in actual implementation, it is difficult to achieve identical top and bottom current sources, one of the
10 current source devices may be driven into a barely-saturated region or even non-saturation region in order to satisfy Kirchoff's current law. The depth of non-saturation depends on the mismatches between the top and bottom current sources, second-order effects of the devices and terminal voltages. Thus, although the top and
15 bottom current source circuits are described as current mirror circuits, the description refers to their structure, rather than their operation, since both top and bottom source circuits of a pair cannot both operate as sources at the same time, if they are not identical. Due to manufacturing limitations, one will provide a slightly smaller
20 current than the other and will thus determine the current through the head, while the other will function more as a switch. However, despite the fact that one of devices may deviate from the expected operating region, the architecture of this embodiment is improved in terms of sensitivity to process and design parameters, speed and
25 settling behaviour under practical conditions.

Considering voltage switch design, bipolar transistors have the disadvantage of excess base storage time being a function of the biasing current. It turns out that the write circuit is more sensitive to the variations in process, temperature and design parameters.
30 Although the replacement of bipolar transistors by non-saturated MOS transistors can solve the base storage time problem, it generates another two problems. Firstly, the high swing requirement to turn ON or OFF a MOS voltage switch would slow the speed. Secondly, a MOS transistor exhibits higher effective drain-to-
35 substrate parasitic capacitance together with stronger capacitive variation against change of drain-to-source voltage when operating in deep non-saturation. The first problem can be improved by reduced swing, but it increases the circuit sensitivity for tuning of a

wide range of write current or increases the circuit complexity, power consumption and area to ensure the MOS switches are properly biased at all the operating conditions. The second problem can only be minimized using smaller size transistors whilst meeting
5 worst case conditions. The embodiment of the invention described, with CMOS current switch circuits, solves the storage time problem as encountered in the prior art bipolar circuits. Since current-mode signal processing is employed, it does not need to turn ON or OFF current switch circuits in high swing as compared with the MOS
10 voltage-switch cases. Therefore, it is advantageous in high-speed circuit designs. Although the non-ideal effect may drive one of the current-source MOS transistors into non-saturation, it would not be as deep as those of the prior art circuits using MOS voltage switches. As a result of these attributes, the embodiment of the invention
15 operates faster and displays less sensitivity than the prior art in practical implementation.

FIG. 6 illustrates a preferred embodiment of the invention. In this drawing, all the same components as in FIG. 5 are given the same reference numerals. As can be seen in the drawing, additional
20 resistors 75 and 76 are inserted into the top current mirror circuits between the gates and drains of transistors 33 and 34, respectively. Similarly, resistors 77 and 78 are inserted into the bottom current mirror circuits between the gates and drains of NMOS transistors 71 and 74, respectively. The added resistors form resistive-based
25 current mirror circuits so as to enhance their speed. The additional resistors improve both the rise time and fall time of the circuit at the expense of the over-shoot effect. This can be explained by the fact that the resistor tends to compensate the current mirror circuit, extending its operating bandwidth. This results in improvement of
30 the speed of the current mirror.

Turning now to FIG. 7, the same components as in FIG. 5 are given the same reference numerals. However, in this case, the differential pair transistors 31 and 32 can be considered as forming part of a first input stage 80 together with the bias current
35 generator 20. The output of this input stage 80 is passed to the two current mirrors formed by transistors 33 and 46 and transistors 34 and 47, as described above. In this embodiment, however, the current mirrors formed by transistors 71 and 72 and transistors 73

and 74 are not controlled by current mirrors, but by a second differential input stage 81. This second differential input stage 81 is complementary to the first differential input stage 80 and is formed by two PNP transistors 82 and 83 and a current source 84. The
5 transistors 82 and 83 are coupled as a differential pair taking the differential data input at data terminals 58 and 59 at their bases. The current source 84 is coupled between the first supply line 15 and the emitters of the PNP transistors 82 and 83, whose collectors are coupled to the drains of transistors 71 and 74, respectively.
10 Therefore, this second differential input stage 81 has an opposite polarity to that of the first differential input stage 80 and is coupled directly to control the current mirrors formed by transistors 71 and 72 and transistors 73 and 74. Thus, the control signals for the current mirrors formed by transistors 71 and 72 and transistors 73
15 and 74 are taken directly from the second input stage 81 instead of being taken from the first input stage 80 and then being reversed in polarity by the current mirrors formed by transistors 33 and 45 and transistors 34 and 48. Although this second input stage has been described as being formed of bipolar transistors, it will be
20 appreciated that it could, alternatively, be made in MOS technology.

In conclusion, the embodiments of the present invention described above do not suffer from at least some of the disadvantages of the prior art. They exploit the use of current-mode switching techniques in CMOS implementation without resorting to
25 either bipolar or MOS voltage switches. Due to the use of MOS transistors for the whole output stage, the excess base drive and breakdown problems of bipolar devices are eliminated. Thus, the write driver circuit is capable of operating a wide range of write currents. Moreover, not only does this structure exhibit low
30 sensitivity to switching speed in spite of process and design parameter variations, it displays better waveforms in terms of settling characteristic and overshoot effect.

It will be appreciated that although three particular embodiments of the invention has been described in detail, various
35 modifications and improvements can be made by a person skilled in the art without departing from the scope of the present invention.



Claims

1. A bi-directional current switching circuit for a load, the circuit comprising a differential output having first and second output
5 terminals for connection to the load, a first current source circuit coupled between a first power supply line and the first output terminal and being coupled to a first input terminal, a second current source circuit coupled between the first power supply line and the second output terminal and being coupled to a second input
10 terminal, a third current source circuit coupled between the first output terminal and a second power supply line and being coupled to a third input terminal, a fourth current source circuit coupled between the second output terminal and the second power supply line and being coupled to a fourth input terminal,
15 the first and second input terminals being arranged for receiving a first differential current switching control signal for switching the first and second current source circuits in anti phase and the third and fourth input terminals being arranged for receiving a second differential current switching control signal for switching the third
20 and fourth current source circuits in anti phase, whereby the first and fourth current source circuits are switched on and off together and the second and third current source circuits are switched off and on together.
- 25 2. A current switching circuit according to claim 1, wherein the first, second, third and fourth current source circuits are formed by first, second, third and fourth current mirror circuits, respectively.
- 30 3. A current switching circuit according to claim 2, wherein each current mirror circuit comprises a first MOS transistor having a source coupled to a supply terminal, a drain coupled to an output terminal and a gate and a second MOS transistor having a source coupled to a supply terminal, a drain coupled to an input terminal and a gate coupled to its drain and to the gate of the first MOS
35 transistor.



4. A current switching circuit according to claim 3, wherein each current mirror circuit further comprises a resistor coupled the gate and the drain of the second MOS transistor.
5. A current switching circuit according to any one of claims 2, 3 or 4, wherein the first and second current mirror circuits are formed of PMOS transistors.
6. A current switching circuit according to any one of claims 2 to 5, wherein the third and fourth current mirror circuits are formed of NMOS transistors.
7. A current switching circuit according to any one of claims 2 to 6, further comprising a differential pair input circuit coupled to first and second data inputs for receiving a differential data signal and coupled to the first and second input terminals for providing the first differential current switching control signal thereat, a fifth current mirror circuit coupled between the first power supply line and the fourth input terminal and being coupled to the first input terminal and a sixth current mirror circuit coupled between the first power supply line and the third input terminal and being coupled to the second input terminal.
8. A current switching circuit according to claim 7, wherein the differential pair input circuit comprises first and second bipolar transistors, the first bipolar transistor having a base coupled to the first data input, a collector coupled to the first input terminal of the current switching circuit and an emitter coupled to a current bias generator circuit and the second bipolar transistor having a base coupled to the second data input, a collector coupled to the second input terminal of the current switching circuit and an emitter coupled to the current bias generator circuit.
9. A current switching circuit according to either claim 7 or claim 8, wherein the fifth current mirror circuit comprises a first MOS transistor having a source coupled to the first supply terminal, a drain coupled to the fourth input terminal and a gate coupled to the second MOS transistor of the first current mirror circuit.



10. A current switching circuit according to any one of claims 7, 8
or 9, wherein the sixth current mirror circuit comprises a first MOS
transistor having a source coupled to the first supply terminal, a
5 drain coupled to the third input terminal and a gate coupled to the
second MOS transistor of the second current mirror circuit.

11. A current switching circuit according to any one of claims 2 to
6, further comprising a first differential pair input circuit coupled to
10 first and second data inputs for receiving a differential data signal
and coupled to the first and second input terminals for providing the
first differential current switching control signal thereat and a
second differential pair input circuit, complementary to the first
differential pair input circuit, coupled to the first and second data
15 inputs for receiving the differential data signal and coupled to the
third and fourth input terminals for providing the a second
differential current switching control signal thereat.

12. A current switching circuit according to claim 11, wherein the
20 first differential pair input circuit comprises first and second bipolar
transistors, the first bipolar transistor having a base coupled to the
first data input, a collector coupled to the first input terminal of the
current switching circuit and an emitter coupled to a current bias
generator circuit and the second bipolar transistor having a base
25 coupled to the second data input, a collector coupled to the second
input terminal of the current switching circuit and an emitter
coupled to the current bias generator circuit.

13. A current switching circuit according to either claim 11 or
30 claim 12, wherein the second differential pair input circuit
comprises first and second bipolar transistors, the first bipolar
transistor having a base coupled to the first data input, a collector
coupled to the third input terminal of the current switching circuit
and an emitter coupled to a current bias generator circuit and the
35 second bipolar transistor having a base coupled to the second data
input, a collector coupled to the fourth input terminal of the current
switching circuit and an emitter coupled to the current bias
generator circuit.



14. An inductive head writer circuit comprising a current
switching circuit according to any preceding claim and an inductive
head coupled between the first and second output terminals of the
5 current switching circuit.