Claims

What is claimed:

1. A semiconductor device, comprising:

a semiconductor die~~;~~

~~an encapsulant deposited over a first surface of the semiconductor die and around a peripheral region of the semiconductor die;~~

~~a first insulating layer formed over the encapsulant and a second surface of the semiconductor die opposite the first surface of the semiconductor die with multiple dwell curing cycles to enhance adhesion to the semiconductor die and encapsulant;~~

~~a first conductive layer formed over the first insulating layer; and~~

~~a second insulating layer formed over the first insulating layer and first conductive layer with multiple dwell curing cycles to enhance adhesion to the first insulating layer and first conductive layer~~ including a plurality of contact pads;

a first insulating layer formed in contact with an active surface of the semiconductor die;

an encapsulant deposited over a second surface of the semiconductor die opposite the active surface and in a peripheral region around the semiconductor die; and

an interconnect structure formed over the encapsulant and first insulating layer, wherein the interconnect structure includes,

(a) a second insulating layer formed in direct contact with the encapsulant and first insulating layer, wherein a coefficient of thermal expansion (CTE) of the second

insulating layer is within a first range of 30-90 parts per million (ppm),

(b) a first conductive layer formed over the second insulating layer and the plurality of contact pads,

(c) a third insulating layer formed in direct contact with the second insulating layer and first conductive layer, wherein a CTE of the third insulating layer is within a second range of 90-110 ppm,

(d) a second conductive layer formed over the second insulating layer and first conductive layer, and

(e) a fourth insulating layer formed in direct contact with the third insulating layer and second conductive layer, wherein a CTE of the fourth insulating layer is within a third range of 110-150 ppm.

2. The semiconductor device of claim 1, wherein ~~the multiple dwell curing cycles include a first dwell step with a first temperature for a first time period, second dwell step with a second temperature for a second time period, and third dwell step with a third temperature for a third time period~~the second insulating layer, third insulating layer, and fourth insulating layer each have a tensile strength >100 MPa, elongation >20%, and modulus <3.0 Gpa under 25°C.

3. The semiconductor device of claim 1, ~~wherein the multiple dwell curing cycles include a first dwell step with a temperature less than 100 °C~~ further including a bump formed over the second conductive layer.

4. The semiconductor device of claim 1, wherein the second insulating layer ~~includes a coefficient of thermal expansion (CTE) different than a CTE of the first insulating layer~~, third insulating layer, and fourth insulating layer each include a polymer dielectric material having a less than 250°C cure temperature.

5. The semiconductor device of claim 1, ~~further including:~~

~~a second conductive layer formed over the second insulating layer and first conductive layer; and~~

~~a third insulating layer formed over the second insulating layer and second conductive layer~~ wherein the CTE of the second insulating layer is 73 ppm, the CTE of the third insulating layer is 106 ppm, and the CTE of the fourth insulating layer is 126 ppm.

~~6. The semiconductor device of claim 5, wherein the third insulating layer includes a coefficient of thermal expansion (CTE) different than a CTE of the first and second insulating layer.~~

~~7~~6. A semiconductor device, comprising:

a semiconductor die~~;~~

~~an encapsulant deposited over a first surface of the semiconductor die and around a peripheral region of the semiconductor die;~~

~~a first insulating layer formed over the encapsulant and a second surface of the semiconductor die opposite the first surface of the semiconductor die;~~

~~a first conductive layer formed over the first insulating layer; and~~

~~a second insulating layer formed over the first insulating layer and first conductive layer, the second insulating layer including a coefficient of thermal expansion (CTE) different than a CTE of the first insulating layer~~ including a plurality of contact pads;

a first insulating layer formed in contact with an active surface of the semiconductor die;

an encapsulant deposited over a second surface of the semiconductor die opposite the active surface and in a peripheral region around the semiconductor die; and

an interconnect structure formed over the encapsulant and first insulating layer, wherein the interconnect structure includes,

(a) a second insulating layer formed in direct contact with the encapsulant and first insulating layer, wherein a coefficient of thermal expansion (CTE) of the second insulating layer is within a first range of 110-150 parts per million (ppm),

(b) a first conductive layer formed over the second insulating layer and the plurality of contact pads,

(c) a third insulating layer formed in direct contact with the second insulating layer and first conductive layer, wherein a CTE of the third insulating layer is within a second range of 90-110 ppm,

(d) a second conductive layer formed over the second insulating layer and first conductive layer, and

(e) a fourth insulating layer formed in direct contact with the third insulating layer and second conductive layer, wherein a CTE of the fourth insulating layer is within a third range of 30-90 ppm.

~~8~~7. The semiconductor device of claim ~~7~~6, ~~wherein the CTE of the first insulating layer is within a first range~~ wherein the second insulating layer, third insulating layer, and fourth insulating layer each have a tensile strength >100 MPa, elongation >20%, and modulus <3.0 Gpa under 25°C.

~~9~~8. The semiconductor device of claim ~~8~~6, ~~wherein the CTE of the second insulating layer is within a second range different than the first range~~ further including a bump formed over the second conductive layer.

~~10~~9. The semiconductor device of claim ~~7~~6, wherein the ~~first insulating layer is formed with multiple dwell curing cycles to enhance adhesion to the semiconductor die and the second insulating layer is formed with multiple dwell curing cycles to enhance adhesion to the first insulating layer and first conductive layer~~ second insulating layer, third insulating layer, and fourth insulating layer each include a polymer dielectric material having a less than 250°C cure temperature.

1~~1~~0. The semiconductor device of claim ~~10~~6, wherein the ~~multiple dwell curing cycles include a first dwell step with a first temperature for a first time period, second dwell step with a second temperature for a second time period, and third dwell step with a third temperature for a third time period~~ CTE of the second insulating layer is 73 ppm, the CTE of the third insulating layer is 106 ppm, and the CTE of the fourth insulating layer is 126 ppm.

~~12. The semiconductor device of claim 7, further including:~~

~~a second conductive layer formed over the second insulating layer and first conductive layer; and~~

~~a third insulating layer formed over the second insulating layer and second conductive layer~~.

~~13. The semiconductor device of claim 12, wherein the third insulating layer includes a CTE different than the CTE of the first and second insulating layers.~~

141. A semiconductor device, comprising:

a semiconductor die~~;~~

~~a first insulating layer formed over the semiconductor die with multiple dwell curing cycles;~~

~~a first conductive layer formed over the first insulating layer; and~~

~~a second insulating layer formed over the first insulating layer and first conductive layer~~ including a plurality of contact pads;

a first insulating layer formed in contact with a first surface of the semiconductor die;

an encapsulant deposited over a second surface of the semiconductor die opposite the first surface and in a peripheral region around the semiconductor die; and

an interconnect structure formed over the encapsulant and first insulating layer, wherein the interconnect structure includes,

(a) a second insulating layer formed in direct contact with the encapsulant and the first insulating layer, wherein a coefficient of thermal expansion (CTE) of the second insulating layer is within a first range,

(b) a first conductive layer formed over the second insulating layer and the plurality of contact pads,

(c) a third insulating layer formed in direct contact with the second insulating layer and first conductive layer, wherein a CTE of the third insulating layer is within a second range overlapping in part and different in part with respect to the first range,

(d) a second conductive layer formed over the second insulating layer and first conductive layer, and

(e) a fourth insulating layer formed in direct contact with the third insulating layer and second conductive layer, wherein a CTE of the fourth insulating layer is within a third range overlapping in part and different in part with respect to the second range.

12. The semiconductor device of claim 11, wherein the first range is selected from the group consisting of 30-90 parts per million (ppm), 90-110 ppm, and 110-150 ppm.

13. The semiconductor device of claim 11, wherein the second range is selected from the group consisting of 30-90 parts per million (ppm) and 90-110 ppm.

154. The semiconductor device of claim 11, ~~14, further including an encapsulant deposited over a first surface of the semiconductor die and around a peripheral region of the semiconductor die, wherein the first insulating layer is formed over the encapsulant and a second surface of the semiconductor die opposite the first surface of the semiconductor die~~ wherein the third range is selected from the group consisting of 30-90 parts per million (ppm), 90-110 ppm, and 110-150 ppm.

165. The semiconductor device of claim 141, ~~wherein the second insulating layer includes a coefficient of thermal expansion (CTE) different than a CTE of the first insulating layer~~ further including a bump formed over the second conductive layer.

176. The semiconductor device of claim 141, ~~further including:~~

~~a second conductive layer formed over the second insulating layer and first conductive layer; and~~

~~a third insulating layer formed over the second insulating layer and second conductive layer~~ wherein the second insulating layer and third insulating layer each have a tensile strength >100 MPa, elongation >20%, and modulus <3.0 Gpa under 25°C.

1~~8~~7. The semiconductor device of claim 1~~7~~1, wherein the~~ third insulating layer includes a CTE different than a CTE of the first and second insulating layers~~ second insulating layer and third insulating layer each include a polymer dielectric material having a less than 250°C cure temperature.

~~19. The semiconductor device of claim 14, wherein the multiple dwell curing cycles include a first dwell step with a temperature less than 100 °C.~~

~~20~~18. A semiconductor device, comprising:

~~a semiconductor die;~~

~~a first insulating layer formed over the semiconductor die;~~

~~a first conductive layer formed over the first insulating layer; and~~

~~a second insulating layer formed over the first insulating layer and first conductive layer, the second insulating layer having a coefficient of thermal expansion (CTE) different than a CTE of the first insulating layer~~a semiconductor die including a plurality of contact pads;

an encapsulant deposited over the semiconductor die opposite the first surface and in a peripheral region around the semiconductor die; and

an interconnect structure formed over the encapsulant and the semiconductor die, wherein the interconnect structure includes,

(a) a first insulating layer formed over the encapsulant and semiconductor die, wherein a coefficient of thermal expansion (CTE) of the first insulating layer is within a first range,

(b) a first conductive layer formed over the first insulating layer and the plurality of contact pads,

(c) a second insulating layer formed in direct contact with the first insulating layer and first conductive layer, wherein a CTE of the second insulating layer is within a second range overlapping in part and different in part with respect to the first range,

(d) a second conductive layer formed over the second insulating layer and first conductive layer, and

(e) a third insulating layer formed in direct contact with the second insulating layer and second conductive layer, wherein a CTE of the third insulating layer is within a third range overlapping in part and different in part with respect to the second range.

19. The semiconductor device of claim 18, wherein the first range is selected from the group consisting of 30-90 parts per million (ppm), 90-110 ppm, and 110-150 ppm.

20. The semiconductor device of claim 18, wherein the second range is selected from the group consisting of 30-90 parts per million (ppm) and 90-110 ppm.

21. The semiconductor device of claim ~~20~~18, ~~further including an encapsulant deposited over a first surface of the semiconductor die and around a peripheral region of the semiconductor die, wherein the first insulating layer is formed over the encapsulant and a second surface of the semiconductor die opposite the first surface of the semiconductor die~~ wherein the third range is selected from the group consisting of 30-90 parts per million (ppm), 90-110 ppm, and 110-150 ppm.

22. The semiconductor device of claim ~~20~~18, ~~wherein the first insulating layer is formed with multiple dwell curing cycles to enhance adhesion to the semiconductor die, and the second insulating layer is formed with multiple dwell curing cycles to enhance adhesion to the first insulating layer and first~~

~~conductive layer~~ further including a bump formed over the second conductive layer.

23. The semiconductor device of claim ~~22~~18, wherein~~ the multiple dwell curing cycles include a first dwell step with a first temperature for a first time period, second dwell step with a second temperature for a second time period, and third dwell step with a third temperature for a third time period~~ the first insulating layer and second insulating layer each have a tensile strength >100 MPa, elongation >20%, and modulus <3.0 Gpa under 25°C.

24. The semiconductor device of claim ~~20~~18,~~ further including:~~

~~a second conductive layer formed over the second insulating layer and first conductive layer; and~~

~~a third insulating layer formed over the second insulating layer and second conductive layer~~ wherein the first insulating layer and second insulating layer each include a polymer dielectric material having a less than 250°C cure temperature.

~~25. The semiconductor device of claim 24, wherein the third insulating layer includes a CTE different than a CTE of the first and second insulating layers.~~