

Phase shift keying transmitter circuit

Technical Field

5 [001] Various embodiments relate to a phase shift keying transmitter circuit.

Background

10 [002] Industrial scientific medical (ISM) frequency bands are used in biomedical applications.

[003] One particular band of interest, which provides a good compromise between in-body loss and antenna efficiency, falls in the 902-928MHz frequency range and has quite limited bandwidth. For high quality imaging application with typical resolution of 640×480 pixels and frame rate of 10fps, both bandwidth efficient modulation scheme and high ratio of image compression are needed.

15 [004] Datasheet ZL70250 from Zarlink Corporation and A. C. W. Wong, G. Kathiresan, C. K. T. Chan, O. Eljamaly, O. Omeni, D. McDonagh, A. J. Burdett and C. Toumazou, "A 1V wireless transceiver for an ultra-low-power SoC for biotelemetry applications," *IEEE J. Solid-State Circuits*, vol. 43, No. 7, pp.1511-1521, July 2008 disclose wireless transmitters employed in biomedical imaging applications that adopt frequency shift keying (FSK) modulation schemes. However, the data rate of these two transmitters is limited to a few Mbps, due to their bandwidth modulation schemes.

20 [005] Y.-H. Liu, C.-L. Li and T.-H. Lin, "A 200-pJ/b MUX-based RF transmitter for implantable multichannel neural recording," *IEEE T. on Microwave Theory and Techniques*, vol. 57, pp.2533-2541, Oct. 2009 discloses a transmitter used for neural recording application that employs an orthogonal quadrature phase shift keying (O-QPSK) modulation scheme that can achieve data rate up to 17.5Mbps. However, the system complexity limits the achievable power consumption level.

25

30

[006] There is thus a need to have a transmitter with simple architecture, which enables high data rate transmission and consumes low power.

Summary

[007] In various embodiments, there is provided a phase shift keying transmitter circuit including: a variable frequency conversion stage adapted to receive a first data signal, wherein the variable frequency conversion stage comprises a plurality of frequency modulating elements, wherein the first data signal controls the number of the plurality of frequency modulating elements that are operated so as to control an operating frequency of the variable frequency conversion stage; and an output stage configured to switch between one of two possible outputs, the signals provided by one of the two possible outputs having an opposite polarity to the other, wherein the output stage is configured to receive a second data signal to control the switching between the two possible outputs, wherein the output stage is coupled to the variable frequency conversion stage and wherein the switching between the two possible outputs changes the phase of a signal from the variable frequency conversion stage by 180°.

[008] In the context of various embodiments, the term “phase shift keying transmitter circuit” may refer to circuitry that can convey data by changing, or modulating, the phase of a reference signal (the carrier wave). Analog or digital modulation may be used. The circuit may include a modulator using a finite number of distinct signals to represent digital data. A finite number of phases, each assigned a unique pattern of binary digits, may be used. Each phase may encode an equal number of bits. Each pattern of bits forms the symbol that is represented by the particular phase. The phase shift keying transmitter circuit may further include means for the modulated carrier wave (carrying the encoded data) to be transmitted.

[009] In the context of various embodiments, the term “circuit” may be understood as any kind of a logic implementing entity, which may be special purpose circuitry or a processor executing software stored in a memory, firmware, or any combination thereof. Thus, in an embodiment, a circuit may be a hard-wired logic

circuit or a programmable logic circuit such as a programmable processor, e.g. a microprocessor (e.g. a Complex Instruction Set Computer (CISC) processor or a Reduced Instruction Set Computer (RISC) processor). A circuit may also be a processor executing software, e.g. any kind of computer program, e.g. a computer program using a virtual machine code such as e.g. Java. Any other kind of implementation of the respective functions which will be described in more detail below may also be understood as a circuit in accordance with an alternative embodiment.

[0010] In the context of various embodiments, the term “variable frequency conversion stage” may mean a stage having an operating frequency that is variable and determined by external means, such as by data that the phase transmitter circuit transmits. Changing the operating frequency of the variable frequency conversion stage has the effect of changing the phase of the output signal of the phase shift keying transmitter circuit. Thus, in various embodiments, the variable frequency conversion stage provides a means to control the output phase of the phase shift keying transmitter circuit.

[0011] In the context of various embodiments, the term “first data signal” may mean a digital signal of logic levels “1” or “0”. In the context of various embodiments, the first data signal acts as a first means of controlling an output phase of signal emitted from the phase shift keying transmitter circuit.

[0012] In the context of various embodiments, the term “frequency modulating elements” may mean devices that change the phase of a signal that is applied thereto. In various embodiments, the “frequency modulating elements” includes capacitors or inductors.

[0013] In the context of various embodiments, the phrase “the number of the plurality of frequency modulating elements that are operated” may mean the number of frequency modulating elements that are electrically connected at any instance of operation, so that the remaining frequency modulating elements are not connected.

[0014] In the context of various embodiments, the term “output stage” may mean the final stage of the phase shift keying transmitter circuit, so that a signal (the output signal) tapped from the output stage would have been processed by the various

stages in the phase shift keying transmitter circuit. In this manner, the output signal would be a signal having been encoded by the unique phase pattern of the phase shift keying transmitter circuit.

5 [0015] In the context of various embodiments, the term “switch” may mean a selection of possible outputs that the output stage is configured to emit.

[0016] In the context of various embodiments, the term “opposite polarity” may mean between two signals, there is a reversal in the phase of one signal compared to the other, so that there is a phase difference of 180° between the two signals. In various embodiments, the output stage may be used together with the variable frequency conversion stage to control the output phase of the phase shift keying transmitter circuit.

10 [0017] In the context of various embodiments, the term “second data signal” may mean a digital signal of logic levels “1” or “0”. The second data signal may be discrete from the first control signal. In the context of various embodiments, the second data signal acts as a second means of controlling an output phase of signal emitted from the phase shift keying transmitter circuit.

15 [0018] In the context of various embodiments, the term “coupled” may mean an electrical connection between a terminal of a first component and a terminal of one or more other components. The electrical connection may be a direct connection, so that the terminals of all the components are connected to a common point; or an indirect connection, so that the terminal of the first component is connected to the terminal of the one or more other components through an interface.

20 [0019] According to one aspect of the invention, there is provided a phase shift keying receiver adapted to receive and extract data from a phase shift keying transmitter according to various embodiments. In the context of various embodiments, the term “phase shift keying receiver” means a demodulator, which is designed specifically for the symbol-set used by the phase shift keying transmitter circuit of various embodiments, to determine the phase of the received signal and map it back to the symbol it represents, thus recovering the original data.

Brief Description Of The Drawings

[0020] In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the invention are described with reference to the following drawings, in which:

[0021] Figure 1A is a schematic representation of a phase shift keying transmitter circuit according to an embodiment.

[0022] Figure 1B is a schematic representation of a phase shift keying transmitter circuit according to an embodiment.

[0023] Figures 2A and 2B show schematic representations of the output stage of a phase shift keying transmitter, according to an embodiment.

[0024] Figure 3 shows the circuitry of a phase shift keying transmitter circuit, according to an embodiment.

[0025] Figure 4 shows a graph of ϕ , created phase difference, against $\omega - \omega_0$, the difference between free running frequency and targeted carrier frequency.

[0026] Figure 5 shows a table that summarises the output phase shift of a carrier signal when subjected to a respective combination of input from control signals.

[0027] Figure 6 shows a capacitor bank according to an embodiment.

[0028] Figure 7 is a schematic representation of a direct QPSK / O-QPSK modulation architecture, according to one embodiment.

[0029] Figure 8 shows graphs illustrating the effect of phase modulation through modifying the self resonant frequency of a LC (inductor-capacitor) tank, according to an embodiment.

[0030] Figure 9 shows the circuitry of a phase shift keying transmitter circuit, according to an embodiment.

[0031] Figure 10 is a graph showing phase relationship with respect to the frequency difference between the harmonic of an injected signal and the self-

resonant frequency of a phase shift keying transmitter circuit, according to an embodiment.

[0032] Figure 11 shows a capacitor bank, according to an embodiment.

[0033] Figure 12 shows a die photograph of a direct QPSK/O-QPSK transmitter chip, according to an embodiment,

[0034] Figure 13A shows a table that summarises the performance of a transmitter chip, according to an embodiment, under 1.4V and 1.2V voltage supplies.

[0035] Figure 13B shows a table that summarises the comparison of the performance of a chip, according to an embodiment, with other shift key transmitters.

[0036] Figure 14A shows graphs of time-domain measurement results of a phase shift keying transmitter circuit, according to an embodiment.

[0037] Figure 14B shows the power spectrum of a QPSK signal, according to an embodiment, at a symbol rate of 25Mbaud.

[0038] Figure 14C shows measured phase noise.

[0039] Figure 15 shows overlapped 4-phase transient waveforms and a locked spectrum.

[0040] Figure 16 shows a QPSK transient signal in a time-domain axis and its accompanying spectrum plot.

[0041] Figure 17 shows a constellation diagram for the four phase output of a phase shift keying transmitter circuit, according to an embodiment.

[0042] Figure 18 shows a schematic representation of an in-body capsule that incorporates a phase shift keying transmitter circuit, according to an embodiment.

[0043] Figure 19A shows a block representation of frequency bands that fall under a wireless body area network.

[0044] Figure 19B shows a system having a transmitter block that incorporates a phase shift keying transmitter circuit, according to one embodiment.

Detailed Description

[0045] Various embodiments provide for a QPSK (quadrature phase shift keying) /O-QPSK (orthogonal quadrature phase shift keying) transmitter, operating at 900MHz, based on injection-locking technique. The transmitter may achieve desired phase modulation through direct control of self-resonant tank frequency and through the use of a polarity swap circuit. This eliminates the need of PLL (phase lock loop), a mixer and a summer, resulting in better phase noise performance, lower power consumption and smaller die size.

[0046] QPSK modulation is bandwidth efficient, but requires complex circuitry compared to other modulation techniques like ASK (amplitude shift keying) and BPSK (binary phase shift keying). Having complex circuitry reduces power efficiency. Advantageously, various embodiments provide a simple circuit to realise the QPSK modulation, and are compatible with conventional transmitters, without the need for an interface. Various embodiments thus fulfill in-body device requirements of low-power, low-complexity and high-bandwidth efficiency. Various embodiments use injection-lock to realise QPSK modulation with simple circuit implementation.

[0047] Figure 1A is a schematic representation of a phase shift keying transmitter circuit 100 according to an embodiment.

[0048] The phase shift keying transmitter circuit 100 may include: a variable frequency conversion stage 106 adapted to receive a first data signal 108, wherein the variable frequency conversion stage 106 may include a plurality of frequency modulating elements 136. The first data signal 108 controls the number of the plurality of frequency modulating elements 136 that are operated so as to control an operating frequency of the variable frequency conversion stage 106. The phase shift keying transmitter circuit 100 also includes an output stage 102 configured to switch between one of two possible outputs (190, 192), the signals (194, 196) provided by one of the two possible outputs (190, 192) having an opposite polarity to the other. The output stage 102 is configured to receive a second data signal 114 to control the switching between the two possible outputs (190, 192), wherein the output stage 102

is coupled to the variable frequency conversion stage 106, wherein the switching between the two possible outputs (190, 192) changes the phase of a signal 198 from the variable frequency conversion stage by 180°.

[0049] Figure 1B is a schematic representation of a phase shift keying transmitter circuit 150 according to an embodiment.

[0050] In various embodiments, the phase shift keying transmitter circuit 150 may include: an output stage 102, an oscillation stage 104 coupled to the output stage 102, a variable frequency conversion stage 106 adapted to receive a first data signal 108, wherein an operating frequency of the variable frequency conversion stage 106 is determined by the first data signal 108 and an activation stage 110 to control operation of the oscillation stage 104, the activation stage 110 coupled to the output stage 102. The output stage 102 may include electrical coupling circuitry 112, the electrical coupling circuitry 112 adapted to receive a second data signal 114, the electrical coupling circuitry 112 reconfigurable in response to the second data signal 114 to cause the output stage 102 to operate in either a first position or a second position, wherein the polarity of signals 116 from the output stage 102 in the first position is opposite to the polarity of signals 116 from the output stage 102 in the second position.

[0051] Further detail on the output stage 102 producing one of two possible outputs (190, 192; see Figure 1A) or operating in the first position and the second position (see Figure 1B) is described with reference to Figures 2A and 2B.

[0052] Figures 2A and 2B show schematic representations of the output stage 102 of the phase shift keying transmitter circuit of Figures 1A (100) and 1B (150). Figure 2A shows the output stage 102 operating 206 to produce a first possible output 190 (see Figure 1A) of the two possible outputs (190, 192; see Figure 1A). Figure 2B shows the output stage 102 operating 208 (see Figure 1A) to produce a second possible output of the two possible outputs (190, 192; see Figure 1A). In the embodiment shown in Figures 2A and 2B, the output stage 102 has two output ports 202 and 204. Although not shown, other embodiments have output stages having more than a pair of output ports. It will be appreciated that in Figures 2A and 2B, only a portion 212 of the output stage 102 that causes switching between the two

possible outputs (190, 192) and toggles the polarity of signals in the output stage 102 is shown.

[0053] In Figure 2A, the second data signal 114_1 has configured the output stage 102 to operate 206 to produce a first output 190. In Figure 2B, the second data signal 114_2 has configured the output stage 102 to operate 208 to produce a second output 192. When comparing the first output 190 against the second output 192, there is a change in phase of 180° in the output signal. The numerals “ 114_1 ” and “ 114_2 ” are used to illustrate that in Figures 2A and 2B, the second data signal has a different value.

[0054] Comparing Figures 2A and 2B, application of the second data signal (114_1 and 114_2) reverses the connections 210 to the output ports 202 and 204, so that the polarity of signals at the output stage 102 in Figure 2A is opposite to the polarity of signals at the output stage 102 in Figure 2B. Considering signal 198 (which is the signal from the variable frequency conversion stage 106, see Figure 1A): in Figure 2A, the signal 198 is sent to the output port 204, while in Figure 2B, the signal 198 is sent to the other output port 202. In this manner, the output stage 102 is configurable between two operating polarities, where one operating polarity is the reverse of the other operating polarity.

[0055] In various embodiments, reversing the connection 212 at the output ports (202, 204) creates, from the perspective of external circuitry (not shown) connected to the output ports (202, 204), a phase difference of 180° in the output signal. In various embodiments, the switching that occurs at the output stage 102 may be used together with the variable frequency conversion stage 106 (see Figure 1A) to control the output phase of the phase shift keying transmitter circuit 100.

[0056] Figure 3 shows the circuitry of a phase shift keying transmitter circuit 300 according to an embodiment.

[0057] The phase shift keying transmitter circuit 300 is similar to the phase shift keying transmitter circuit of Figures 1A (100) and 1B (150) in that the phase shift keying transmitter circuit 300 has a variable frequency conversion stage 106 and an output stage 102. The variable frequency conversion stage 106 is adapted to receive a first data signal 108, wherein the variable frequency conversion stage 106 may

include a plurality of frequency modulating elements (336, 338, 340 and 342). The first data signal 108 controls the number of the plurality of frequency modulating elements (336, 338, 340 and 342) that are operated so as to control an operating frequency of the variable frequency conversion stage 106. The output stage 102 is configured to switch between one of two possible outputs, the signals provided by one of the two possible outputs having an opposite polarity to the other. The output stage 102 is configured to receive a second data signal 114 to control the switching between the two possible outputs, wherein the output stage 102 is coupled to the variable frequency conversion stage 106, wherein the switching between the two possible outputs changes the phase of a signal 198 from the variable frequency conversion stage by 180°.

[0058] Comparing the phase shift keying transmitter circuit 300 of Figure 3 with the phase shift keying transmitter circuit 150 of Figure 1B, the phase shift keying transmitter circuit 300 also has an oscillation stage 104 coupled to the output stage 102, and an activation stage 110 coupled to the output stage 102.

[0059] The various components of the output stage 102 are as follows.

[0060] The output stage 102 has a first terminal 302 to which a first terminal 310 of the variable frequency conversion stage 106 is coupled. The output stage 102 also has a second terminal 304 to which a second terminal 312 of the variable frequency conversion stage 106 is coupled. The first terminals (310, 302) of both the variable frequency conversion stage 106 and the output stage 102 and the second terminals (312 and 304) of both the variable frequency conversion stage 106 and the output stage 102 are located along separate signal paths (384 and 386) of the phase shift keying transmitter circuit 300.

[0061] The first terminal 302 of the output stage 102 is coupled to a respective terminal of each of the oscillation stage 104 and the activation stage 110. Specifically, first terminal 306 of the oscillation stage 104 is coupled to the first terminal 302 of the output stage 102 and first terminal 314 of the activation stage 110.

[0062] The second terminal 304 of the output stage 102 is coupled to a respective terminal of each of the oscillation stage 104 and the activation stage 110.

Specifically, second terminal 308 of the oscillation stage 104 is coupled to the second terminal 304 of the output stage 102 and second terminal 316 of the activation stage 110.

[0063] The output stage 102 further includes a first output port 202; and a second output port 204. The output ports (202 and 204) have an electrical connection with the first and second terminals (302 and 304) of the output stage 102. In one of the two possible outputs provided by the output stage 102, the first terminal 302 of the output stage 102 is coupled to the first output port 202 and the second terminal 304 of the output stage 102 is coupled to the second output port 204. In the other of the two possible outputs provided by the output stage 102, the first terminal 302 of the output stage 102 is coupled to the second output port 204 and the second terminal 304 of the output stage 102 is coupled to the first output port 202.

[0064] In Figure 3, the reference numeral 210 is used to denote the two possible electrical connections between the output ports (202 and 204) and the terminals (302 and 304), both of the output stage 102. In a first connection (denoted by the reference numeral 206), which is effected when the second data signal 114 configures the output stage 102 to produce one of two possible outputs (for example, a high control bit, "1"), the first terminal 302 is connected to the first output port 202 and the second terminal 304 is connected to the second output port 204. In a second connection (denoted by the reference numeral 208), which is effected when the second data signal 114 configures the output stage 102 to produce the other of two possible outputs (for example, a low control bit, "0"), the first terminal 302 is connected to the second output port 204 and the second terminal 304 is connected to the first output port 202. A transmission gate circuit (not shown) may be used to realise the two possible electrical connections. When the transmission gate circuit is implemented by, for example, NMOS transistors, the second data signal 114 controls which of the transistors will be activated to achieve the required connection.

[0065] The output stage 102 includes electrical coupling circuitry 112, the electrical coupling circuitry 112 controllable by the second data signal 114. The electrical coupling circuitry 112 controls switching of the electrical connection 210 between the output ports (202 and 204) of the output stage 102 and the terminals

(302 and 304) of the output stage 102. The electrical coupling circuitry 112 is reconfigurable in response to the second data signal 114 to cause the output stage 102 to operate in either the first connection (depicted by the circled portions 206) or the second connection (depicted by the circled portions 208), wherein the polarity of the signal 320 from the output stage 102 in the first connection 206 is opposite to the polarity of the signal 320 from the output stage 102 in the second connection 208.

[0066] By toggling the electrical connection 210 within the electrical coupling circuitry 112, a simple mechanism to effect changing the phase of an output signal 320 of the output stage 102 is provided, so as to facilitate the creation of a distinct signal that represents the digital data encoded within the output signal 320.

[0067] In the embodiment shown in Figure 3, the electrical coupling circuitry 112 is a swap circuit.

[0068] The output stage 102 further includes a buffer 318 connected between the electrical coupling circuitry 112 and both the first output port 202 and the second output port 204.

[0069] The oscillation stage 104 of the phase shift keying transmitter circuit 300 is coupled to the output stage 102.

[0070] In the context of various embodiments, the term “oscillation stage” may mean a stage that by itself, or together with one or more of the variable frequency conversion stage and the output stage, changes the phase of the output signal of the phase shift keying transmitter circuit. The various components of the oscillation stage 104 are as follows.

[0071] The oscillation stage 104 includes a plurality of inductors (322, 324), each coupled to the first terminal 302 or the second terminal 304 of the output stage 102; and a plurality of capacitors (326, 328), each coupled to the first terminal 302 or the second terminal 304 of the output stage 102. In the embodiment shown in Figure 3, there are only two inductors (322, 324) and two capacitors (326, 328), wherein the capacitors (326, 328) are of the variable type. An analogue signal V_{tune} may be used to fine frequency tune the operating frequency of the variable frequency conversion stage 106, through the two tunable capacitors (326, 328). Such a fine frequency tuning complements the discrete operating frequency changes of the variable

frequency conversion stage 106 brought about by the number of capacitors C_1' and C_2' that are activated and the minimum capacitance of the activated capacitors C_1' and C_2' . In other embodiments (not shown), there may be any number of inductors and capacitors, where either or both of the inductors and capacitors may have a fixed or variable rating. Specifically, several inductors connected in series or in parallel may be used in place of each of the plurality of inductors (322, 324) or several capacitors connected in series or in parallel may be used in place of each of the plurality of capacitors (326, 328).

[0072] A first terminal 306 of a first inductor 322 of the plurality of inductors (322, 324) is coupled to the first terminal 302 of the output stage 102 and a second terminal 330 of the first inductor 322 is coupled to a reference potential VDD. A first terminal 306 of a first capacitor 326 of the plurality of capacitors (326, 328) is coupled to the first terminal 302 of the output stage 102. A first terminal 308 of a second capacitor 328 of the plurality of capacitors (326, 328) is coupled to the second terminal 304 of the output stage 102 and a second terminal 332 of the second capacitor 328 is coupled to a second terminal 332 of the first capacitor 326. A first terminal 308 of a second inductor 324 of the plurality of inductors (322, 324) is coupled to the second terminal 304 of the output stage 102 and a second terminal 334 of the second inductor 324 is coupled to the reference potential VDD.

[0073] There may be one or more components (not shown) between the terminals within each of the various stages (102, 104, 106 and 110). Examples of these components include inductors and capacitors. For instance, there may be (not shown) an inductor or an additional capacitor located between the first terminal 306 of the oscillation stage 104 and the second terminal 308 of the oscillation stage 104. Similarly, there may be (not shown) an inductor or an additional capacitor located between the first terminal 310 of the variable frequency conversion stage 106 and the second terminal 312 of the variable frequency conversion stage 106.

[0074] In the embodiment shown in Figure 3, the variable frequency conversion stage 106 is coupled to the output stage 102. The various components of the variable frequency conversion stage 106 are as follows.

[0075] The variable frequency conversion stage 106 includes a plurality of frequency modulating elements (336, 338, 340 and 342), each of the frequency modulating elements (336, 338, 340 and 342) coupled to the first terminal 302 or the second terminal 304 of the output stage 102. The variable frequency conversion stage 106 further includes a plurality of switches (344, 346), each coupled to a frequency modulating element from the plurality of the frequency modulating elements (336, 338, 340 and 342). Operation of the plurality of switches (344 and 346) is controlled by the first data signal 108 to operate the frequency modulating element (336, 338, 340 and 342). An NMOS transistor (not shown) may be used for each of the plurality of switches (344, 346), the operation of the NMOS transistor being controlled by the first data signal 108. In a first operation mode, none of the frequency modulating elements (336, 338, 340 and 342) is activated. In a second operation mode, either the frequency modulating elements (336 and 338) or the frequency modulating elements (340 and 342) is activated. In a third operation mode, all the frequency modulating elements (336, 338, 340 and 342) are activated.

[0076] A first terminal 370 of a first frequency modulating element 336 of the plurality of the frequency modulating elements (336, 338, 340 and 342) is coupled to the first terminal 302 of the output stage 102. A first terminal 348 of a switch 344 of the plurality of the switches (344 and 346) is coupled to a second terminal 348 of the first frequency modulating element 336. A first terminal 372 of a second frequency modulating element 338 of the plurality of the frequency modulating elements (336, 338, 340 and 342) is coupled to the second terminal 304 of the output stage 102, and a second terminal 350 of the switch 344 is coupled to a second terminal 350 of the second frequency modulating element 338.

[0077] Similarly, a first terminal 370 of a third frequency modulating element 340 of the plurality of the frequency modulating elements (336, 338, 340 and 342) is coupled to the first terminal 302 of the output stage 102. A first terminal 352 of a switch 346 of the plurality of the switches (344 and 346) is coupled to a second terminal 352 of the third frequency modulating element 340. A first terminal 372 of a fourth frequency modulating element 342 of the plurality of the frequency modulating elements (336, 338, 340 and 342) is coupled to the second terminal 304

of the output stage 102, and a second terminal 354 of the switch 346 is coupled to a second terminal 354 of the fourth frequency modulating element 342.

[0078] The variable frequency conversion stage 106 further includes a logic circuit 356 adapted to receive the first data signal 108 and the second data signal 114; and a plurality of multiplexers 358. Each of the multiplexers ($358_1, \dots, 358_n$) is coupled to the output of the logic circuit 356 and adapted to receive an element of a binary input ($360_1, \dots, 360_n$), wherein operation of a switch (344, 346) of the plurality of the switches (344, 346) is controlled by the output ($362_1, \dots, 362_n$) of a respective multiplexer ($358_1, \dots, 358_n$) of the plurality of multiplexers 358. In this manner, an option is provided to control operation of the switches (344, 346) using both the first data signal 108 and the second data signal 114.

[0079] In various embodiments, the term "element" in the phrase "element of a binary input" may refer to any bit of a binary input. For instance, the element may be the most significant bit or least significant bit in a digital word input.

[0080] In one embodiment, the logic circuit 356 performs an XOR operation. In one embodiment, the plurality of frequency modulating elements (336, 338, 340 and 342) and the plurality of switches (344, 346) are arranged in an array. For example, in the embodiment shown in Figure 3, the array has two rows of frequency modulating elements, where each row has two frequency modulating elements (336 and 338; 340 and 342) with a switch (344, 346) connecting the two respective frequency modulating elements (336 and 338; 340 and 342) together. In another embodiment, it is possible that the array has any number of rows of frequency modulating elements (for instance, Figure 6 shows an array where there are six rows of capacitors). The number of the plurality of the frequency modulating elements (336, 338, 340 and 342) that are operated causes a 45° phase change of signals processed by the variable frequency conversion stage 106.

[0081] In the embodiment shown in Figure 3, the plurality of frequency modulating elements (336, 338, 340 and 342) includes capacitors (C_1', C_2'). Although other values are possible, the capacitor (C_1', C_2') has a value in the range of 1pF to 5pF, for example around 3pF. Further, while the embodiment shown in Figure 3 uses capacitors (C_1', C_2') for the frequency modulating elements (336, 338,

340 and 342), other components, such as inductors, may be used. In the embodiment shown in Figure 3, there are only two capacitors (C_1 , C_2) per row, but in other embodiments (not shown), any number of capacitors may be used.

[0082] The activation stage 110 of the phase shift keying transmitter circuit 300 is coupled to the output stage 102. In the context of various embodiments, the term “activation stage” may mean a stage that is used to switch the phase shift keying transmitter circuit on or off.

[0083] The various components of the activation stage 110 are as follows.

[0084] The activation stage 110 includes a plurality of transistors (364, 366), each coupled to the first terminal 302 or the second terminal 304 of the output stage 102, wherein the first terminal 302 of the output stage 102 and the second terminal 304 of the output stage 102 are connected to a reference current I_{inj} . In the embodiment shown in Figure 3, the reference current I_{inj} is an injected signal having a designated harmonic that is chosen to be the same as the targeted carrier frequency of the phase shift keying transmitter circuit 300. Also, in the embodiment shown in Figure 3, the connection of the first terminal 302 of the output stage 102 to the reference current I_{inj} is controlled via a switch 374. The connection of the second terminal 304 of the output stage 102 to the reference current I_{inj} is controlled via a switch 376.

[0085] A control terminal 364₁ of a first transistor 364 of the plurality of the transistors (364, 366) is coupled to the second terminal 304 of the output stage 102, a first controlled terminal 364₂ of the first transistor 364 is coupled to the first terminal 302 of the output stage 102 and a second controlled terminal 364₃ of the first transistor 364 is coupled to a biasing current I_{osc} . A control terminal 366₁ of a second transistor 366 of the plurality of the transistors (364, 366) is coupled to the first terminal 302 of the output stage 102, a first controlled terminal 366₂ of the second transistor 366 is coupled to the second terminal 304 of the output stage 102 and a second controlled terminal 366₃ of the second transistor 366 is coupled to the biasing current I_{osc} . In the embodiment shown in Figure 3, both the reference current I_{inj} and the biasing current I_{osc} are connected to ground. In another embodiment (not shown), both the reference current I_{inj} and the biasing current I_{osc} may each be connected to different reference potentials or a same non-zero reference potential.

[0086] The first data signal 108 and the second data signal 114 are elements of data to be transmitted. In the embodiment shown in Figure 3, where the first data signal 108 and the second data signal 114 are each a discrete single bit of data, the phase of an output signal 320 of the output stage 102 becomes modulated by only two bits of data, so that the circuit 100 becomes a quadrature phase shift keying (QPSK) RF transmitter. At any instance, the output signal 320 will then have encoded therein, digital data belonging to any one of the following combinations: 00, 01, 10 or 11.

[0087] At the receiver end, a phase shift keying receiver 368 is adapted to receive and extract data from a signal transmitter, such as the phase shift keying transmitter circuit 300. With reference to receiving the output signal 320 from the phase shift keying transmitter circuit 300, the phase shift keying receiver 368 is configured to recover the original data transmitted, through the use of, for example, mapping circuitry.

[0088] For the sake of simplicity, several same reference numerals (such as 306, 308, 332, 350, 352, 354, 370 and 372) have been used above to denote terminals belonging to different components, especially since these same reference numerals indicate terminals that are respectively coupled together. For example:

the same reference numeral 306 is used to denote the first terminals of all of the first inductor 322, the first capacitor 326 and the oscillation stage 104;

the same reference numeral 308 is used to denote the first terminal of the second inductor 324, the first terminal of the second capacitor 328 and the second terminal of the oscillation stage 104;

the same reference numeral 332 is used to denote the second terminals (332 and 332) of both the first capacitor 326 and the second capacitor 328;

the same reference numeral 350 is used to denote the second terminal of the switch 344 and the second terminal of the second frequency modulating element 338;

the same reference numeral 352 is used to denote the first terminal of the switch 346 and the second terminal of the third frequency modulating element 340;

the same reference numeral 354 is used to denote the second terminal of the switch 346 and the second terminal of the fourth frequency modulating element 342;

the same reference numeral 370 is used to denote the first terminals of both the first frequency modulating element 336 and the third frequency modulating element 340; while

the same reference numeral 372 is used to denote the first terminals of both the second frequency modulating element 338 and the third frequency modulating element 340.

[0089] However, it is not the case that only terminals denoted with the same reference numeral are those that are coupled together. For example:

terminal 306 is coupled together with terminals 310, 302, 314 and 370 and also with the reference current I_{inj} , where connection of any of these terminals 306, 310, 302, 314 and 370 to the reference current I_{inj} is through the switch 374;

terminal 308 is coupled together with terminals 312, 304, 316 and 372 and also with the reference current I_{inj} , where connection of any of these terminals 308, 312, 304, 316 and 372 to the reference current I_{inj} is through the switch 376; and

terminals 330 and 334 are coupled together with the reference potential VDD.

[0090] The phase shift keying transmitter circuit 300 is a low-power low-complexity transmitter based on injection-lock technology. From Figure 3, the phase shift keying transmitter circuit 300 includes an LC VCO (inductor-capacitor voltage controlled oscillator, implemented by the oscillation stage 104), a capacitor bank 378 (inside the variable frequency conversion stage 106), a pair of differential injection signals (ω_0 and ω_0_bar), a swap circuit (implemented by the electrical coupling circuitry 112) and a buffer 318. In various embodiments, the term "injection-lock" may mean that an oscillation stage (the LC tank) of the voltage controlled oscillator (VCO) of a phase shift keying transmitter circuit locks to the frequency ω_0 of an injected signal. A created phase shift depends on the frequency difference between the LC VCO free-running frequency and the injected frequency.

[0091] In the embodiment shown in Figure 3, the VCO is designed to generate a frequency which is around a targeted carrier frequency, ω_0 . The VCO is designed to cover a certain range sufficient enough to generate the required phase shift. The injected differential signals (ω_0 and ω_0_bar) have frequency ω_0/N , where N is an even number.

[0092] Operation of the phase shift keying transmitter circuit 300 is as follows.

[0093] Figure 4, which shows a graph 400 being a plot of θ , created phase difference, against $\omega - \omega_0$, the difference between LC VCO free running frequency and targeted carrier frequency. Associating the symbols shown in Figure 4 with the phase shift keying transmitter circuit 300 of Figure 3: ω is the LC VCO free running frequency, ω_0 is the N^{th} harmonic of the injected signal (shown as ω_0 and $\omega_0\text{-bar}$ in Figure 3); Q is the quality factor of the LC VCO 104; I_{inj} is the injected current located at ω_0 ; I_{osc} is the LC VCO 104 bias current; and θ is the created phase difference.

[0094] As illustrated in Figure 4, with constant injected frequency ω_0 , if the free running frequency ω changes from $-(\omega_0/2Q) * (I_{\text{inj}}/I_{\text{osc}})$ to $(\omega_0/2Q) * (I_{\text{inj}}/I_{\text{osc}})$, the relative phase will change 180° (indicated by the reference numeral 402).

[0095] For a QPSK transmitter, 90° phase difference should be achieved. In one embodiment, injection lock technology can be used to provide a sufficient range to achieve the 90° phase difference between a 45° phase shift (indicated by reference numeral 404) and a -45° phase shift (indicated by reference numeral 406).

[0096] With reference to Figure 3, data0 (the first data signal 108) controls the capacitor bank 378 and switches the free-running frequency between ω_1 and ω_2 , where

$$\omega_1 = \frac{1}{\sqrt{LC_1}} = \frac{1}{\sqrt{L(C'_1 + C)}} \quad (1)$$

and

$$\omega_2 = \frac{1}{\sqrt{LC_2}} = \frac{1}{\sqrt{L(C'_2 + C)}} \quad (2).$$

In the embodiment shown in Figure 3, when the first data signal 108 has a digital value of "1", the switch 344 will be closed, while the switch 346 remains open, so that the capacitors 336 and 338 (each having capacitance of C'_1) are connected to the output stage 102 to provide the free-running frequency of ω_1 , while the capacitors 340 and 342 are disconnected from the output stage 102. On the other hand, when the first data signal 108 has a digital value of "0", the switch 346 will be closed, while the switch 344 remains open, so that the capacitors 340 and 342 (each having capacitance of C'_2) are connected to the output stage 102 to provide the free-running

frequency of ω_2 , while the capacitors 336 and 338 are disconnected from the output stage 102. It is also possible that the operation of the switches (344 and 346) are reversed, so that when the first data signal 108 has a digital value of "1", the switch 344 will open and the switch 346 close; and when the first data signal 108 has a digital value of "0", the switch 344 will close and the switch 346 open. Thus, input of the first data signal 108 and maintenance at one of its discrete values, has the variable frequency conversion stage 106 kept at a free-running frequency (two free-running frequencies, ω_1 and ω_2 , are described, although more free-running frequencies are possible when there are more rows of capacitors within the capacitor bank 378). Further, from equations (1) and (2), the capacitance values of the capacitors (326, 328, 336, 338, 340 and 342) and the inductance values of the inductors (322 and 324) have an impact on the free-running frequency ω_1 and ω_2 .

[0097] Returning to Figure 4, taking the phase of the injected signal (I_{inj} shown in Figure 3) as a reference, though the absolute phase difference will not be 45° , the relative phase shift will be 90° (indicated by the span of the reference numerals 404 and 406 along the θ axis) between the free-running frequency ω_1 and ω_2 . Through injection lock technology, a phase shift of 45° and -45° are achieved on the injected signal I_{inj} .

[0098] After undergoing phase shift of 45° and -45° , the injected signal I_{inj} is sent to the swap circuit (within the electrical coupling circuitry 112), which is controlled by data1 (the second data signal 114) as shown in Figure 3.

[0099] In the embodiment shown in Figure 3, when the second data signal 114 has a digital value of "1", the connection within the swap circuit is as per the connection shown as unbroken lines in the electrical coupling circuitry 112. In more detail, the first terminal 302 of the output stage 102 will be coupled to an output port 380 of the electrical coupling circuitry 112, while the second terminal 304 of the output stage 102 will be coupled to an output port 382 of the electrical coupling circuitry 112.

[00100] When the second data signal 114 has a digital value of "0", the connection within the swap circuit is as per connection shown as dashed lines in the electrical coupling circuitry 112. In more detail, the first terminal 302 of the output stage 102

will be coupled to the output port 382 of the electrical coupling circuitry 112, while the second terminal 304 of the output stage 102 will be coupled to the output port 380 of the electrical coupling circuitry 112.

[00101] It is also possible that the operation of the swap circuit is reversed. When the second data signal 114 has a digital value of "1", the first terminal 302 of the output stage 102 will be coupled to the output port 382 of the electrical coupling circuitry 112, while the second terminal 304 of the output stage 102 will be coupled to the output port 380 of the electrical coupling circuitry 112. When the second data signal 114 has a digital value of "0", the first terminal 302 of the output stage 102 will be coupled to an output port 380 of the electrical coupling circuitry 112, while the second terminal 304 of the output stage 102 will be coupled to an output port 382 of the electrical coupling circuitry 112.

[00102] Thus, the effect of the swap circuit of the electrical coupling circuitry 112 would be to reverse the phase of the carrier signal, so that for the injected signal I_{inj} already with 45° and -45° phase shift (compared with the original phase of the injected signal I_{inj}), an overall phase shift of -135° and 135° (compared with the original phase of the injected signal I_{inj}) would be achieved. The table 500 in Figure 5 summarises the output phase shift 502 of a carrier signal when subjected to a respective combination of input from the first data signal 108 and the second data signal 114.

[00103] In order to get an accurate 90° phase shift by using injection lock technology, various embodiments use a binary weighted capacitor bank for the variable frequency conversion stage 106 (see Figure 3). Figure 6 shows an embodiment 600 of such a capacitor bank.

[00104] The capacitor bank 600 includes a plurality of capacitors (602, 604, 606, 608, 614, 616, 618 and 620), each of the capacitors (602, 604, 606, 608, 614, 616, 618 and 620) coupled to the first terminal 302 (compare Figure 3) of the output stage 102 through a first terminal 610 of the capacitor bank 600 or the second terminal 304 (compare Figure 3) of the output stage 102 through a second terminal 612 of the capacitor bank 600. Each of a plurality of switches (622, 624, 626 and 628) is

coupled to a respective capacitor from the plurality of capacitors (602, 604, 606, 608, 614, 616, 618 and 620).

[00105] All the rows of the capacitor bank 600 have an identical electrical arrangement. Taking the first row as an example, a first terminal 630 of a first capacitor 602 is coupled to the first terminal 610 of the capacitor bank 600. A first terminal 632 of the switch 622 is coupled to a second terminal 632 of the first capacitor 602. A first terminal 636 of a second capacitor 604 is coupled to the second terminal 612 of the capacitor bank 600, and a second terminal 634 of the switch 622 is coupled to a second terminal 634 of the second capacitor 604.

[00106] A logic circuit 656 is adapted to receive the first data signal 108 and the second data signal 114. Each (658₀, ..., 658₅) of a plurality of multiplexers 658 is coupled to the output of the logic circuit 656 and adapted to receive an element of a binary input (660₀, ..., 660₅). Operation of a switch (622, 624, 626 and 628) of the plurality of switches (622, 624, 626 and 628) is controlled by the output (662₀, ..., 662₅) of a respective multiplexer (658₀, ..., 658₅) of the plurality of multiplexers 658.

[00107] Since each of the multiplexers (658₀, ..., 658₅) receives, as one of its input, an output of the logic circuit 656, the operation of each switch (622, 624, 626 and 628) is controlled by the first data signal 108 and the second data signal 114. In addition, since each of the multiplexers (658₀, ..., 658₅) also receives, as another of its input, a respective one of the binary inputs (660₀, ..., 660₅), operation of each switch (622, 624, 626 and 628) is also dependent on the respective one of the binary input (660₀, ..., 660₅), in that the capacitor bank 600 value is binary-oriented. In the embodiment shown in Figure 6, the logic circuit 656 performs an XOR operation. Although other values are possible, each of the capacitors (602, 604, 606, 608, 614 and 616) has a value in the range of 1pF to 5pF, for example around 3pF.

[00108] The phase shift keying transmitter circuit 300 (see Figure 3) provides a QPSK (Quadrature Phase Shift Keying) RF transmitter based on injection-lock technology. The QPSK transmitter, according to various embodiments, demonstrates features such as low-power, low-complexity and higher bandwidth efficiency comparing to other known modulation techniques. Various embodiments find

application in wireless communication systems like GSM (Global System for Mobile Communications) and is also suitable for biomedical applications.

[00109] In designing various embodiments, a balance is sought between the power consumption and the locking range, the settling time and the power consumption, the locking range and the phase accuracy controlled by the smallest capacitor unit. Since the phase shift keying transmitter circuit 300 (see Figure 3) is applied to an in-body pill (see Figure 18), various embodiments have power consumption as the first priority. As various embodiments use QPSK, phase accuracy is more easily satisfied compared to 8PSK and 16PSK.

[00110] For injection lock technology, phase noise is mainly determined by the reference signal phase noise. Various embodiments adopt a crystal, which demonstrates quite good phase noise. For instance, there are known crystal oscillator that can achieve -150dBc/Hz phase noise. Various embodiments use such a crystal oscillator and when 11th order harmonics injection is used, the phase noise is around -140dBc/Hz, which is sufficient to satisfy design requirement. As there is no LO leakage problem, because the injected signal is quite far from the final output carrier, design parameters are relaxed for various embodiments.

[00111] Figure 7 is a schematic representation of a direct QPSK / O-QPSK modulation architecture 700, according to one embodiment, employing a subharmonic injection-locked oscillator. The architecture 700 includes an injection-locked VCO (IL-VCO) 702, a polarity swap circuit 704, a buffer 706, a mapping circuitry 708 which transforms input I and Q signals to corresponding output phases, an XOR Gate 710 and an antenna 712. By eliminating the need of multi-phase PLL (phase lock loop) and having the VCO 702 operate at twice the output frequency, the architecture 700 can work with very low power consumption.

[00112] The phase modulation principle of the architecture 700 is illustrated in Figure 8. Figure 8 shows graphs 818 and 820 illustrating the effect of phase modulation through modifying the self resonant frequency of a LC (inductor-capacitor) tank, according to an embodiment. Graph 818 is a plot of output amplitude against frequency. Graph 820 is a plot of output phase shift against frequency.

[00113] Although the output frequency of the IL-VCO 702 (see Figure 7) is locked to the harmonic 802 of the injected signal, its output phase is determined by the difference between the self-resonant frequency of the LC tank (not shown) within the VCO 702 (see Figure 7) and the harmonic 802 of the injected signal. A more detailed discussion on the output phase being determined by the difference between the self-resonant frequency of an LC tank and the harmonic of an injected signal can be found in B. Razavi; "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, No. 9, pp. 1415-1424, Sept. 2004.

[00114] As illustrated by the solid line curves (808 and 810) in Figure 8, by controlling the self-resonant frequency (denoted by the reference numeral 804) of the LC tank to be lower than the harmonic frequency 802 of the injected signal in such a way that the LC tank signal 808 coinciding with the harmonic frequency 802 of the injected signal lags (denoted using the reference numeral 812) behind the harmonic 802 of the injected signal by 45° , an output signal comes to exhibit -45° phase shift. On the other hand, as illustrated by the dotted line curves (806 and 814) by making the self-resonant frequency (denoted by the reference numeral 816) higher than the harmonic signal 802 so that the LC tank signal 806 coinciding with the harmonic frequency 802 can be ahead (denoted using the reference numeral 822) of the harmonic signal by 45° , an output signal phase shift becomes $+45^\circ$. Therefore, by changing the self-resonant frequency (804 and 816) of the LC tank, a phase difference of 90° can be created in an output signal. The self-resonant frequency of an LC tank can be easily modified through capacitor bank switching (as earlier described with reference to Figures 3 and 4).

[00115] With reference to Figure 7, to generate all four phases required for QPSK/O-QPSK modulation, the polarity swap circuit 704 is employed to introduce 180° phase shift to the output signal. By employing both a capacitor bank (which is incorporated inside the VCO 702) and the polarity swap circuit 704, $+45^\circ$, -45° , -135° and $+135^\circ$ phase shifts, required for QPSK/O-QPSK modulation, are realised.

[00116] In addition to having lower power consumption, various embodiments have improved phase noise performance, as the phase noise characteristics of the IL-VCO 702 follows the characteristics of the injected signal (F_{inj} , F_{inj}), rather than that

of the on-chip VCO. A more detailed discussion on phase noise following the characteristics of an injected signal can be found in J. Lee and H. Wang, "Study of subharmonically injection-locked PLLs", *IEEE J. Solid-State Circuits*, vol. 44, No. 5, pp.1539-1553, May 2009. Improved phase noise performance leads to better error vector magnitude (EVM) performance of the QPSK/O-QPSK transmitter. In various embodiments, the power consumption can be as low as 5.88mW at 1.4V supply while transmitting at 50Mbps. The simplicity of the architecture 700 also results in smaller die area.

[00117] Figure 9 is a schematic representation of a phase shift keying transmitter circuit 900 according to an embodiment. Since the architecture of the phase shift keying transmitter circuit 900 of Figure 9 is similar to the phase shift keying transmitter circuit 300 of Figure 3 (which has been described in detail above), only selected features of the phase shift keying transmitter circuit 900 are described.

[00118] The phase shift keying transmitter circuit 900, employing an injection lock voltage controlled oscillator (IL-VCO) 902, includes a symmetrical NMOS cross-coupled pair (NM2, NM3), an LC tank incorporating a center-tapped differential inductor L and a capacitor bank 978, differential pair transistors (NM4, NM5) for signal injection and tail currents (I_{osc} and I_{inj}). F_{inj} and F_{inj_b} are differential injected signals. Comparing the phase shift keying transmitter circuit 900 of Figure 9 with the phase shift keying transmitter circuit 300 of Figure 3, the phase shift keying transmitter circuit 900 uses differential pair transistors (NM4, NM5) as switches (compare switches 374 and 376 in Figure 3) to introduce the differential injected signals, F_{inj} and F_{inj_b} , into the phase shift keying transmitter circuit 900.

[00119] The free-running LC VCO 902 has self-resonant frequency ω_0 centered around the target carrier frequency ω_c . The designated harmonic of the injected signal ω_{inj} is chosen to be the same as ω_c . With reference to the above description associated with Figure 8, the self-resonant frequency ω_0 can be changed by switching the capacitor bank 978 to generate the desired phase shift of $+45^\circ$, -45° , -135° and $+135^\circ$, as explained earlier.

[00120] Figure 10 shows the phase relationship with respect to frequency difference between the harmonic of the injected signal and self-resonant frequency

$(\omega_{inj} - \omega_0)$, as reproduced from B. Razavi; "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, No. 9, pp. 1415-1424, Sept. 2004.

[00121] Figure 10 is a graph 1008 of a plot of θ , created phase difference, against $\omega_{inj} - \omega_0$, the frequency difference between the harmonic of an injected signal and a self-resonant frequency of a LC VCO.

[00122] In the context of the phase shift keying transmitter circuit 900 of Figure 9, where the injected signal ω_{inj} is fixed, the curve 1002 in Figure 10 shows the variation of phase shift with respect to the self-resonant frequency ω_0 of the LC VCO 902. As shown in Figure 10, when the self-resonant frequency ω_0 of an LC tank varies from ω_{01} to ω_{02} , the output phase changes from -45° (see reference numeral 1004) to $+45^\circ$ (see reference numeral 1006). Therefore, the curve 1002 serves as a reference in designing the capacitor bank 978 to have a sufficiently wide range and high resolution to obtain self-resonant tank frequency of ω_{01} and ω_{02} .

[00123] Returning to Figure 9, in one embodiment, the IL-LCVCO 902 is locked to the 9th harmonic of a 100MHz differential injection signal source I_{inj} . The lock range ω_L may be expressed as follows:

$$\omega_L = \frac{\omega_0}{2Q} \cdot \frac{I_{inj,9th}}{I_{osc}} = \frac{\omega_0}{2Q} \cdot \frac{4I_{inj,1st}}{I_{osc} 9\pi}, \quad (3)$$

where Q is the tank quality factor, $I_{inj,9th}$ and $I_{inj,1st}$ are the amplitude of the 9th harmonic and the fundamental of the injected current I_{inj} respectively. The ratio of $I_{inj,1st}$ to I_{osc} is chosen such that the lock range ω_L is smaller than the fundamental injection frequency to avoid false locking, but large enough to achieve the desired phase resolution. A more detailed discussion on obtaining the lock range ω_L can be found in R. Harjani; N. LanKa; S. Patnaik, "Fast hopping injection locked frequency generation for UWB," *IEEE International Conf. on Ultra-Wideband*, pp.502-507, Sept. 2007.

[00124] Figure 11 shows an embodiment of the capacitor bank 978 of the phase shift keying transmitter circuit 900.

[00125] Since the architecture of the capacitor bank 978 of Figure 11 is similar to the capacitor bank 678 of Figure 6 (which has been described in detail above), only

selected features of the capacitor bank 978 are described. Comparing the capacitor bank 978 of Figure 11 with the capacitor bank 678 of Figure 6, the capacitor bank 978 uses a switch 1158 for each of the plurality of multiplexers 658 in Figure 6.

[00126] The capacitor bank 978 is a 6-bit binary capacitor bank implemented to provide sufficient resolution and coverage in self-resonant frequency tuning characteristics. Design of the capacitor bank 978, according to one embodiment, is as follows.

[00127] The resonant frequency of the capacitor bank 978 can be tuned to ω_{01} to ω_{02} (refer to reference numerals 1004 and 1006 in Figure 10) by setting the control words $B\omega_{01}[5:0]$ and $B\omega_{02}[5:0]$ (collectively indicated by the reference numeral 1160) respectively. The minimum phase step depends on both the minimum capacitor value $C_{\min}$ and the lock range ω_L [see equation (3)]. Once the maximum allowable lock range without false locking is determined, the minimum capacitor value $C_{\min}$ can be calculated to achieve the desired phase resolution. Although other values are possible, the minimum capacitor value $C_{\min}$ has a value in the range of 10fF to 100fF, for example around 50fF.

[00128] Considering Figure 9 in conjunction with Figure 11, the phase shift keying transmitter circuit 900 includes a polarity swap circuit 912 and a buffer 918. Two control signals Data0 (denoted using reference numeral 908) and Data1 (denoted using reference numeral 914) will modulate the phase shift keying transmitter circuit 900 to produce QPSK/O-QPSK signal.

[00129] Both Data0 (908) and Data1 (914) control the capacitor bank 978 values that get switched into the LC tank 904 through an XOR gate (refer to Figure 11) to produce the desired resonant frequency ω_{01} or ω_{02} , as described in the description above with reference to Figure 11. Operation of the capacitor bank 978 at ω_{01} or ω_{02} respectively generates -45° and $+45^\circ$ phase modulation. The polarity swap circuit 912 then introduces a 180° phase shift to the output signal depending on the control signal Data1 (914). Operation of the polarity swap circuit 912 gives rise to two additional phases $+135^\circ$ and -135° . The capacitor bank 978, controlled through the XOR output, achieves Gray coding of the modulated phase. With reference to Figure 7, both QPSK and O-QPSK modulation are implementable by the mapping

circuitry 708 that performs the desired mapping between input I and Q data to the control signals Data0 (908) and Data1 (914).

[00130] In one embodiment, an inverter-type output buffer (not shown) may be adopted for the buffer 918. With further detail found in Y.-H. Liu, C.-L. Li and T.-H. Lin, "A 200-pJ/b MUX-based RF transmitter for implantable multichannel neural recording," *IEEE T. on Microwave Theory and Techniques*, vol. 57, pp.2533-2541, Oct. 2009, such an inverter-type output buffer is compatible with the quasi constant-envelope nature of O-QPSK modulation signals. The simulated power efficiency may then be around 20%.

[00131] Figure 12 shows a die photograph of a direct QPSK/O-QPSK transmitter chip 1200, according to an embodiment, fabricated using 0.18 μ m CMOS process. The active core 1202 occupies an area of around 0.4mm $\times$ 0.7mm. The chip 1200 was mounted on a printed circuit board (PCB) for testing. When transmitting at 50Mbps data rate, the transmitter achieved EVM (error vector magnitude) of 6.6% and low power consumption (including buffer) of 5.88mW and 3mW at 1.4V and 1.2V supplies respectively. The table in Figure 13A summarises the performance of the chip 1200 under 1.4V and 1.2V supplies.

[00132] The table in Figure 13B summarises the comparison of the chip 1200 with other shift key transmitters disclosed in the following publications:

1304: A. C. W. Wong, G. Kathiresan, C. K. T. Chan, O. Eljamaly, O. Omeni, D. Mcdonagh, A. J. Burdett and C. Toumazou, "A 1V wireless transceiver for an ultra-low-power SoC for biotelemetry applications," *IEEE J. Solid-State Circuits*, vol. 43, No. 7, pp.1511-1521, July 2008;

1306: Zarlink Corp.: Datasheet ZL70250;

1308: J. L. Bohorquez, A. P. Chandrakasan, and J. L. Daeson, "A 350uW CMOS MSK transmitter and 400uW OOK super-regenerative receiver for medical implant communications," *IEEE J. Solid-State Circuits*, vol. 44, No. 4, pp.1248-1259, Apr. 2009; and

1310: Y.-H. Liu, C.-L. Li and T.-H. Lin, "A 200-pJ/b MUX-based RF transmitter for implantable multichannel neural recording," *IEEE T. on Microwave Theory and Techniques*, vol. 57, pp.2533-2541, Oct. 2009.

In addition, the chip 1200 provides a circuit that is less complex than the transmitters disclosed in the publications 1304 to 1310. In Figure 13B, the term FOM is calculated using the equation:

$$FOM = \frac{DataRate(Mbps) \cdot Freq(GHz) \cdot Ptx(mW)}{Pconsum(mW)} \quad (4)$$

[00133] Figures 14A to 14C show measurement results of the chip 1200 at 1.4V supply voltage.

[00134] Figure 14A shows graphs of time-domain measurement results. The measured phase noise is -121dBc/Hz at 1MHz offset, as shown in Figure 14C and limited by injection signal phase noise. For these measurements, a signal from a pattern generator with phase noise was employed as the injection signal. Nevertheless, the total integrated rms jitter was only 1.8°, which is sufficient for QPSK/O-QPSK transmission. Figure 14B shows the power spectrum of the QPSK signal at symbol rate of 25Mbaud.

[00135] The table below summarises simulation results of a phase shift keying transmitter circuit, according to an embodiment, using injection lock.

Simulated Results of QPSK transmitter using injection lock

Parameter	Symbol	Conditions/Remarks	Typical	Range	units
Centre Frequency	f		900	900	GHz
Supply Voltage	V_{DD}		1.8	1.6 ~ 2.0	V
Current Consumption	I_{dd}	Measured at 1.8V supply	7	3.61~11	mA
Settling Timing	T_{set}		6.7	5~11	ns
Temperature	T	SS:80 TT:27 FF:-40	27	Room temperature	°C
Output Power	P_o		1.43	-11~5.5	dBm
Core Current	I_{core}		2.8	2~3.89	mA
Input / Output Characteristic					
Data Voltage Level	$DI;D0$		1.6	1 ~ 1.8	V
Data Rate	f_{in}	50% duty cycle	20	1 ~ 50	MHz
Output voltage swing	V_o	Differential output @ 400Ω	2.1	0.5 ~ 3.35	V
Output Phase Variation	ψ		±2	±2 ~ ±3	°
Amplitude Variation	A_{var}		0.2	0.01~0.2	V
Modulator Parameters					
Modulation	QPSK				

[00136] Figures 15 to 16 show simulation results of a phase shift keying transmitter circuit, according to one embodiment.

[00137] In Figures 15 and 16, m1 to m6 are position markers used to show performance of the phase shift keying transmitter circuit at various intervals during the simulation run.

[00138] Figure 15 shows overlapped 4-phase transient waveforms (i.e. for an output signal with encoded data "00", "01", "10" and "11") and the locked spectrum. Figure 15 shows that the output of a fabricated phase shift keying transmitter circuit is indistinguishable from the output of an ideal phase shift keying transmitter circuit, thereby establishing that there is little amplitude and phase error comparing the fabricated phase shift keying transmitter circuit against the ideal phase shift keying transmitter circuit.

[00139] Figure 16 shows a QPSK transient signal in a time-domain axis and its accompanying spectrum plot. Simulation results under different operating conditions TT, FF and SS (to measure process variation) are also listed in this figure.

[00140] Figure 17 shows a constellation diagram that may be used to calculate EVM (error vector magnitude) of the four phase output of a phase shift keying transmitter circuit. Figure 17 shows experimental results of a phase shift keying transmitter circuit, according to one embodiment, measured under 50Mbps QPSK signal. The achieved EVM is 6.556%, which is equivalent to a signal-to-noise ratio of around -23dB, therefore meeting the targeted BER of 10^{-4} .

[00141] Figure 18 shows a schematic representation of an in-body capsule 1800 that incorporates a phase shift keying transmitter circuit 1802, according to an embodiment. The capsule 1800 may be introduced into a living organism to provide a means to monitor health signals from the living organism.

[00142] The capsule includes the phase shift keying transmitter circuit 1802; an image sensor 1804; a battery 1806 that powers the phase shift keying transmitter circuit 1802 and the image sensor 1804; and a microheater 1808. The microheater 1808 may be used to change the tilt angle of the image sensor 1804 to widen the optical angle range of capture.

[00143] Figure 19A shows a block representation of frequency bands that fall under a wireless body area network (WBAN) 1904, using IEEE 802.15.6 communication standards. The frequency bands include ultra wide band (UWB)

1906, a Medical Implant Communication Service (MICS) band 1908, ultra low power (ULP) Bluetooth band 1910 and Zigbee 1912. The frequency band 1914 within which a phase shift keying transmitter circuit, according to one embodiment, transmits falls under the WBAN 1904.

5 [00144] Figure 19B shows a system 1916 having a transmitter block 1918 that incorporates a phase shift keying transmitter circuit, according to one embodiment.

[00145] The system 1916 includes the transmitter block 1918; a switch 1922 that switches between allowing the system 1916 to receive or transmit signals to a coupled antenna 1926; a receiver block 1920 and a digital baseband block 1924.

10 [00146] The transmitter block 1918 further includes an amplifier 1918a and a modulator 1918b for I and Q signal paths.

[00147] The receiver block 1920 includes a low noise amplifier 1920a; a radio frequency front-end 1920b; a demodulator 1920c for I and Q signal paths and an amplifier 1920d.

15 [00148] While embodiments of the invention will be shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which
20 come within the meaning and range of equivalency of the claims are therefore intended to be embraced.

CLAIMS

1 A phase shift keying transmitter circuit comprising:

5 a variable frequency conversion stage adapted to receive a first data signal, wherein the variable frequency conversion stage comprises a plurality of frequency modulating elements, wherein the first data signal controls the number of the plurality of frequency modulating elements that are operated so as to control an operating frequency of the variable frequency conversion stage; and

10 an output stage configured to switch between one of two possible outputs, the signals provided by one of the two possible outputs having an opposite polarity to the other, wherein the output stage is configured to receive a second data signal to control the switching between the two possible outputs, wherein the output stage is coupled to the variable frequency conversion stage and wherein the switching between the two possible outputs changes the phase of a signal from the variable frequency conversion stage by
15 180°.

2. The phase shift keying transmitter circuit of claim 1, wherein the output stage further comprises:

20 a first terminal to which a first terminal of the variable frequency conversion stage is coupled; and

25 a second terminal to which a second terminal of the variable frequency conversion stage is coupled, wherein the first terminals of both the variable frequency conversion stage and the output stage and the second terminals of both the variable frequency conversion stage and the output stage are located along separate signal paths of the phase shift keying transmitter circuit.

3. The phase shift keying transmitter circuit of claim 2, wherein the output stage further comprises:

a first output port; and

30 a second output port, the output ports having an electrical connection with the first and second terminals of the output stage, wherein in one of the two possible outputs, the

first terminal of the output stage is coupled to the first output port and the second terminal of the output stage is coupled to the second output port; and wherein in the other of the two possible outputs, the first terminal of the output stage is coupled to the second output port and the second terminal of the output stage is coupled to the first output port.

5 4. The phase shift keying transmitter circuit of claim 3, wherein the output stage comprises electrical coupling circuitry controllable by the second data signal, the electrical coupling circuitry controlling switching of the electrical connection between the output ports of the output stage and the terminals of the output stage.

10 5. The phase shift keying transmitter of claim 4, wherein the electrical coupling circuitry is a swap circuit.

15 6. The phase shift keying transmitter of claim 5, wherein the output stage further comprises a buffer connected between the electrical coupling circuitry and both the first output port and the second output port.

7. The phase shift keying transmitter circuit of claims 2 to 6, further comprising an oscillation stage coupled to the output stage.

20 8. The phase shift keying transmitter of claim 7, wherein the oscillation stage comprises

a plurality of inductors, each coupled to the first terminal or the second terminal of the output stage; and

25 a plurality of capacitors, each coupled to the first terminal or the second terminal of the output stage.

9. The phase shift keying transmitter of claim 8, wherein

30 a first terminal of a first inductor of the plurality of inductors is coupled to the first terminal of the output stage and a second terminal of the first inductor is coupled to a reference potential,

a first terminal of a first capacitor of the plurality of capacitors is coupled to the first terminal of the output stage,

a first terminal of a second capacitor of the plurality of capacitors is coupled to the second terminal of the output stage and a second terminal of the second capacitor is coupled to a second terminal of the first capacitor, and

a first terminal of a second inductor of the plurality of inductors is coupled to the second terminal of the output stage and a second terminal of the second inductor is coupled to the reference potential.

10. The phase shift keying transmitter of claims 2 to 9, wherein each of the frequency modulating elements of the variable frequency conversion stage is coupled to the first terminal of the output stage or the second terminal of the output stage; and the variable frequency conversion stage further comprises:

a plurality of switches, each coupled to a frequency modulating element from the plurality of the frequency modulating elements, wherein operation of the plurality of switches is controlled by the first data signal to operate the frequency modulating element.

11. The phase shift keying transmitter of claim 10, wherein

a first terminal of a first frequency modulating element of the plurality of the frequency modulating elements is coupled to the first terminal of the output stage,

a first terminal of a switch of the plurality of the switches is coupled to a second terminal of the first frequency modulating element,

a first terminal of a second frequency modulating element of the plurality of the frequency modulating elements is coupled to the second terminal of the output stage, and

a second terminal of the switch is coupled to a second terminal of the second frequency modulating element.

12. The phase shift keying transmitter of claims 10 or 11, wherein the variable frequency conversion stage further comprises

a logic circuit adapted to receive the first data signal and the second data signal;
and

a plurality of multiplexers, each coupled to the output of the logic circuit and adapted to receive an element of a binary input, wherein operation of a switch of the plurality of the switches is controlled by the output of a respective multiplexer of the plurality of multiplexers.

13. The phase shift keying transmitter of claim 12, wherein the logic circuit performs an XOR operation.

14. The phase shift keying transmitter of claims 10 to 13, wherein the plurality of the frequency modulating elements and the plurality of the switches are arranged in an array.

15. The phase shift keying transmitter circuit of any one of the preceding claims, wherein the number of the plurality of the frequency modulating elements that are operated causes a 45° phase change of signals processed by the variable frequency conversion stage.

16. The phase shift keying transmitter of any one of the preceding claims, wherein the plurality of the frequency modulating elements comprises capacitors.

17. The phase shift keying transmitter of claim 16, wherein the capacitor has a value of around 3pF.

18. The phase shift keying transmitter circuit of claims 2 to 14, further comprising an activation stage coupled to the output stage.

19. The phase shift keying transmitter of claim 18, wherein the activation stage comprises a plurality of transistors, each coupled the first terminal of the output stage or the second terminal of the output stage, wherein the first terminal of the output stage and the second terminal of the output stage are connected to a reference current.

20. The phase shift keying transmitter of claim 19, wherein

a control terminal of a first transistor of the plurality of the transistors is coupled to the second terminal of the output stage, a first controlled terminal of the first transistor is coupled to the first terminal of the output stage and a second controlled terminal of the first transistor is coupled to a biasing current,

a control terminal of a second transistor of the plurality of transistors is coupled to the first terminal of the output stage, a first controlled terminal of the second transistor is coupled to the second terminal of the output stage and a second controlled terminal of the second transistor is coupled to the biasing current.

21. A phase shift keying receiver adapted to receive and extract data from a phase shift keying transmitter of any one of the preceding claims.