

Description

This invention relates to a method for manufacturing semiconductor devices, and more particularly to a method for manufacturing semiconductor devices having contact holes of different sizes via which the wirings thereof are made.

It is known in the art that a semiconductor integrated circuit is formed to have first and second wiring patterns which are laminated over a semiconductor substrate and are isolated from each other by means of an interlayer insulation film. The first wiring pattern is constituted by a plurality of lower wiring layers and the second wiring pattern is constituted by a plurality of upper wiring layers. The upper wiring layers are connected to the lower wiring layers via a plurality of contact holes formed in the interlayer insulation film. Each contact hole is formed in an area in which one set of upper and lower wiring layers connected to each other via the contact hole overlap each other. The sizes of the contact holes may vary depending on the withstand current determined for each contact hole. However, the matching margin A between the contact hole and the lower wiring layer and the matching margin B between the contact hole and the upper wiring layer are constant. The matching margin A is determined depending on an aligning error of a mask pattern used in a process for forming the first wiring pattern, and the matching margin B is determined depending on an aligning error of mask patterns used in processes for forming the contact hole and the first wiring pattern.

The above semiconductor integrated circuit can be formed at relatively high yield when the integration density is low. However, if the width of the wiring is narrowed with an increase in the integration density and the size C of the contact hole is set, for example, to be less than 1.5 μm according to the width of the wiring, the manufacturing yield of the semiconductor integrated circuit is considerably lowered.

An object of this invention is to provide a method for manufacturing semiconductor devices in which the manufacturing yield can be prevented from being lowered even when the contact hole is made small.

The above object can be attained by a method for manufacturing semiconductor devices, comprising the steps of:

forming a first wiring pattern on a semiconductor body, said wiring pattern including first and second lower conductive layers;

forming an insulation film covering said first wiring pattern;

forming first and second contact holes in said insulation film, said first contact hole having a first size and exposing a portion of said first lower

conductive layer, said second contact hole having a second size, larger than said first size, and exposing a portion of said second lower conductive layer; and

forming a second wiring pattern on said insulation film, said second wiring pattern including first and second upper conductive layers connected to said first and second lower conductive layers via said first and second contact holes; said contact hole forming step including the steps of:

forming a resist film covering said insulation film;

forming a resist pattern by photolithographic processing by exposing said resist film to light using a mask pattern having a first defining area which defines said first contact hole (13B), and a second defining area which defines said second contact hole; and

etching said insulation film with said resist pattern being used as a mask;

characterized by:
a compensation step effected when said semiconductor device is miniaturized to a degree at which said contact hole forming step makes the size of said first contact hole smaller than that of said first defining area while the size of said second contact hole remains equal to that of said second defining area; said compensation step including the substeps of:

determining the increase of said exposing light required to reduce the difference between the sizes of said first contact hole and said first defining area, and

determining the reduction in size of said second defining area to suppress the increase in size of said second contact hole above the second size under the increased amount of said exposing light.

According to the method for manufacturing semiconductor devices, the dependencies of the resist pattern formation sub-step on the contact hole size can be cancelled. When the design size of the first contact hole is reduced to a first size which is less than 3 μm , the actual size of the first contact hole which is formed through the resist pattern formation sub-step and the insulation film etching sub-step, generally becomes smaller than the designed value, thereby increasing the contact resistance. In order to solve this problem, the exposing light amount used in the resist pattern formation sub-step of the method of this invention is previously determined so that the size of the first contact hole which is formed in the insulation film etching sub-step may become equal to the first size or the designed value. In this case, the exposing light amount will increase in comparison with the normal case. Further, it is possible that the size of the second contact hole becomes larger than the second size and extends beyond an area on which

the second lower conductive layer and the second upper conductive layer are overlapped. However, in this invention, the reduced amount of the second hole defining area of the mask pattern is previously determined so that the size of the second contact hole which is formed in the insulation film etching sub-step can be set equal to the second size or the designed value. In this way, if the contact holes are formed with the designed sizes, reduction in the manufacturing yield due to miniaturization of the contact hole can be prevented. Further, since the miniaturization of the contact hole will not be limited by the dependency of the resist pattern formation sub-step and the insulation film etching sub-step on the contact hole size, the semiconductor device can be formed with a further increased integration density.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a plan view of a semiconductor device according to one embodiment of this invention;

Fig. 2 is a cross sectional view of the semiconductor device taken along the line X-X of Fig. 1;

Figs. 3A to 3F are cross sectional views showing the process of manufacturing the semiconductor device shown in Figs. 1 and 2;

Fig. 4 is a graph showing the relation between the size of a contact hole and the size of the contact hole defining area of a mask pattern obtained in a case where exposing light amount used in the step of Fig. 3E is changed;

Fig. 5 is a graph showing the size of the contact hole defining area of a mask pattern which is determined by the designed size of a contact hole;

Fig. 6 is a graph showing the relation between the increase in the exposing light amount and the increase in the contact hole size; and

Fig. 7 is a graph showing the size of the control hole defining area which is determined by the designed size of a contact hole according to another embodiment.

There will now be described a semiconductor device according to an embodiment of this invention with reference to Figs. 1 to 6.

Fig. 1 is a plan view of the semiconductor device and Fig. 2 is a cross sectional view of the semiconductor device taken along the line X-X of Fig. 1. The semiconductor device is a semiconductor integrated circuit having a number of semiconductor elements formed in the surface area of a semiconductor substrate 16. Two semiconductor elements 10A and 10B among the semiconductor elements are shown in Fig. 2. Wirings for the number of semiconductor elements are made by using first and second wiring patterns 11 and 12

which are disposed over the semiconductor substrate 16. The first and second wiring patterns 11 and 12 are formed of aluminum and are isolated from each other by means of interlayer insulation film 14 disposed between the first and second wiring patterns 11 and 12. The first wiring pattern 11 includes a plurality of wiring layers, for example, wiring layers 11A, 11B, 11C, which are formed on a silicon oxide film 15 covering the surface of the semiconductor substrate 16. The wiring layers 11A and 11C are connected to the semiconductor elements 10A and 10B via openings formed in the oxide film 15, thus serving as electrodes of the semiconductor elements 10A and 10B. The second wiring pattern 12 includes a plurality of wiring layers, for example, wiring layers 12A, 12B, 12C, which are formed on a silicon oxide film 15 covering the exposed surface of the oxide film 15 and the first wiring pattern 11 and serving as an interlayer insulation film 14. The wiring layers 12A, 12B and 12C are connected to the wiring layers 12A, 12B and 12C via contact holes 13A, 13B and 13C formed in the interlayer insulation film 14. The contact holes 13A, 13B and 13C are formed so as not to exceed outwardly of the areas of the interlayer insulation film 14 which lie over the wiring layers 12A, 12B and 12C. For this purpose, the reference positions of the contact holes are determined to be at positions displaced from the peripheries of the areas of the interlayer insulation film 14 by a preset distance corresponding to the matching margin A for absorbing a mask alignment error in the same manner as in the prior art. For example, the width of the contact hole 13A is set at 3 μm and the width of the contact holes 13B and 13C is set at, for example, 1.5 μm which is less than 3 μm . In a case where the contact holes 13A, 13B and 13C are formed in a rectangular form as shown in Fig. 1, the width of the contact hole is used to represent the size of the contact hole.

Next, the manufacturing process of the semiconductor device is explained with reference to Figs. 3A to 3F.

In the step of Fig. 3A, a number of semiconductor elements, for example, semiconductor elements 10A and 10B are formed in the surfaces area of the semiconductor substrate 16 and then the silicon oxide film 15 is formed to a thickness of 0.6 μm . The surfaces of the semiconductor substrate 16 and the semiconductor elements 10A and 10B are covered with the silicon oxide film 15. Openings are selectively formed in positions corresponding to the semiconductor elements 10A and 10B, (see Fig. 2 for example) in the silicon oxide film 15 and then an aluminum layer is formed by deposition to a thickness of 1 μm on the exposed portions of the silicon oxide film 15 and the semiconductor elements 10A and 10B. The first

wiring pattern 11 is formed by selectively removing the aluminum layer from the silicon layer 15 by using a mask pattern. The wiring layers 11A, 11B and 11C are formed of portions of the aluminum layer left behind on the silicon oxide film 15.

In the step of Fig. 3B, a silicon oxide film 14A of a thickness of $1.1\text{ }\mu\text{m}$ is formed to cover the exposed portion of the first wiring pattern 11 and the silicon oxide film 15 by the plasma CVD method. The upper surface of the silicon oxide film 15 has convex and concave portions corresponding to the exposed portions of the first wiring pattern 11 and the silicon oxide film 15. A photoresist 17 is formed by coating on the silicon oxide film 14A so as to fill up the concave portions of the upper surface. The thickness of that portion of the photoresist 17 which lies on a portion other than the concave portion is set to $0.8\text{ }\mu\text{m}$.

In the step of Fig. 3C, the photoresist 17 is etched back by the thickness of $1.8\text{ }\mu\text{m}$ together with the convex portions of the silicon oxide film 14A. As a result, the upper surface of the silicon oxide film 14A is made flat.

In the step of Fig. 3D, a silicon oxide film 14B is formed by deposition to a thickness of $1.4\text{ }\mu\text{m}$ on the silicon oxide film 14A by the plasma CVD method. The interlayer insulation film 14 is formed of the silicon oxide films 14A and 14B.

In the step of Fig. 3E, a positive photoresist film 18 is uniformly formed by coating to a thickness of $1.5\text{ }\mu\text{m}$ on the upper surface of the interlayer oxide film 14 and is then subjected to a photolithographic process. In the photolithographic process, a stepper is used to divide the plane of the photoresist film 18 into a plurality of areas and permit the areas to be sequentially exposed. In exposing each of the areas, a mask pattern as will be described later is used and the exposing light amount is set to an adequate value described later. After the completion of the exposing process for all the areas, the exposed portion of the photoresist film 18 is removed and the remaining portion of the photoresist film 18 is used to constitute a resist pattern 18A. After this, a reactive ion etching (RIE) process is effected with the resist pattern 18A used as a mask so as to selectively remove portion of the interlayer insulation film 14 from the first wiring pattern 11. As a result, the contact holes 13A, 13B and 13C are formed. Then, the resist pattern 18A is removed.

In the step of Fig. 3F, an aluminum layer 12A is formed by deposition to a thickness of $1.0\text{ }\mu\text{m}$ on the exposed portion of the interlayer insulation film 14 and the first wiring pattern 11. The aluminum layer 12A is selectively removed from the interlayer insulation film 14 by using a mask pattern and the second wiring pattern 12 shown in Fig. 2 is formed of the remaining portion of the alu-

minum layer 12A.

Now, the photolithographic process effected in the step of Fig. 3E is explained in more detail. In a case where the contact hole is formed in the interlayer insulation film 14, the contact hole defining area having the same size as the designed size of the contact hole is set in the mask pattern in the prior art. When the photoresist film 18 is exposed by using the mask pattern, the exposing light amount is so determined that the size or width of the actually formed contact hole can be set to be equal to that of the contact hole defining area. For example, if the exposing light amount is determined so as to form a contact hole of $3\text{ }\mu\text{m}$ in the interlayer insulation film 14, this exposing light amount can be used for formation of a contact hole having a width of larger than $3\text{ }\mu\text{m}$, for example, $4\text{ }\mu\text{m}$, $6\text{ }\mu\text{m}$ or $8\text{ }\mu\text{m}$ as shown by the line I in Fig. 4. However, it is confirmed from experiments that if the previously determined exposing light amount is used for formation of a contact hole having a width of less than $3\text{ }\mu\text{m}$, for example, $2\text{ }\mu\text{m}$, the width of an actually formed contact hole is set to $1.6\text{ }\mu\text{m}$. Further, if the contact hole is designed to have a width of $1.5\text{ }\mu\text{m}$, the width of an actually formed contact hole is set to $0.8\text{ }\mu\text{m}$. In this case, the contact resistance between the two wiring layers connected to each other via the contact hole becomes extremely high. When the exposing light amount is increased so as to set the width of the contact hole with $1.5\text{ }\mu\text{m}$ width to the designed value based on the above experiments, the width of a further contact hole with more than $3\text{ }\mu\text{m}$ width is actually formed larger than the designed value by $0.6\text{ }\mu\text{m}$ as shown by the line II of Fig. 4.

With the mask pattern of this embodiment, the size of the defined area for the contact hole 13A is set to $2.4\text{ }\mu\text{m}$ which is smaller than the designed value by $0.6\text{ }\mu\text{m}$ and the size of the defined areas for the contact holes 13B and 13C is set to $1.5\text{ }\mu\text{m}$ which is equal to the designed value. In this case, the exposing light amount is set to be twice the stand and exposing light amount at which contact holes of not less than $3\text{ }\mu\text{m}$ width can be actually formed with the designed widths.

Fig. 5 shows the mask size of the contact hole defining area of a mask pattern which is determined according to the designed size of a contact hole, and Fig. 6 shows the relation between the increase in the exposing light amount and the increase in the contact hole size.

According to this embodiment, contact holes of 1.5 and $3\text{ }\mu\text{m}$ widths can be formed with the designed values by changing the size of the mask pattern and at the same time effecting an excessive light exposing step in the photolithographic process. In the process of exposing the photoresist 18A, if the exposing light amount is simply in-

creased, then a contact hole of not larger than 1.5 μm width may be formed with the designed value, but a contact hole of not less than 1.5 μm width cannot be formed with the designed value but may be formed with a width larger than the designed value by 0.6 μm , that is smaller than 0.7 μm saturation value shown in Fig. 6. In order to correct the above error, the size of the contact hole defining area of a mask pattern used for formation of a contact hole with not less than 3 μm width is reduced by 0.6 μm in comparison with the designed value.

With this correction, the error for formation of contact holes of all sizes can be suppressed within 0.2 μm . As a result, it becomes unnecessary to uselessly widen the matching margin of the mask pattern.

Semiconductor integrated circuits having contact holes of various sizes ranging from 2 to 20 μm are manufactured as experiments according to the method of this embodiment. Generally, the mask aligning error of 0.3 μm and the etching error of 0.2 μm occur in the formation of these contact holes. In a case where the matching margin A between the first wiring pattern and each contact hole was set 0.7 μm , the contact hole may not extend outwardly of the first wiring pattern. Since the matching margin A is used for the mask aligning error of 0.3 μm and the etching error of 0.2 μm , 0.2 μm is left unused in the matching margin A when the contact hole is formed with a designed size. Therefore, it was proved that a sufficiently high reliability could be obtained in the manufacturing process.

Unlike this embodiment, if the exposing light amount is increased without correcting the size of the mask pattern for formation of contact holes of not less than 3 μm , the size of the contact hole will increase 0.6 μm . In this case, the size of the contact hole increases by 0.3 μm on one side thereof. Taking the mask aligning error of 0.3 μm and the etching error of 0.2 μm into consideration, there is a possibility that the contact hole may extend outwardly of the first wiring pattern when the matching margin A is set to 0.7 μm . In order to prevent this, it becomes necessary to set the matching margin A to at least 0.8 μm . Further, in order to attain the reliability of the same level as that obtained in the above embodiment, it will be necessary to set the matching margin A to 1.0 μm . Assume that the semiconductor device is manufactured under a condition that the matching margin A is set to 1.0 μm and it includes 9,000 semiconductor elements. Then, the integration density of the semiconductor device manufactured according to the method of the above embodiment may be approx. 1.3 times that of the semiconductor device with the matching margin A of 1.0 μm .

In the step of Fig. 3E, the exposing light amount is increased so that the contact holes 13B and 13C can be formed with designed sizes. Instead, it can be considered that the contact hole defining areas for the contact holes 13B and 13C are enlarged to prevent the contact holes 13B and 13C from being made smaller than the designed sizes. However, this method cannot reliably prevent the manufacturing yield from being lowered since the size of each of the contact holes 13B and 13C is remarkably changed if the size of the corresponding contact hole defining area is slightly changed due to a variation in the mask pattern formation process.

In the embodiment described above, the contact holes of 1.5 and 3 μm are provided to the semiconductor device. In a case where a contact hole of a size larger than 1.5 μm and smaller than 3 μm is further provided to the semiconductor device, the size of the contact hole defining area of a mask pattern is set smaller than the designed size of this contact hole to prevent this contact hole from being made larger than the designed size, as is shown in Fig. 5. Instead, it is possible to set the size of the contact hole defining area equal to the designed size of this contact hole if the matching margin remains, as is shown in Fig. 7.

Further, a contact hole smaller than 1.5 μm can be provided to the semiconductor device. In this case, the exposing light amount used in the step 3E is determined so that this contact hole is actually formed with the designed value. Generally, the exposing light amount is determined according to the size of the smallest one of the contact holes provided in the semiconductor device.

Reference signs in the claims are intended for better understanding and shall not limit the scope.

Claims

1. A method for manufacturing semiconductor devices, comprising the steps of:

forming a first wiring pattern (11) on a semiconductor body (10A, 10B, 15, 16), said wiring pattern (11) including first and second lower conductive layers (11B, 11C; 11A);

forming an insulation film (14) covering said first wiring pattern (11);

forming first and second contact holes (13B, 13C, 13A) in said insulation film (14), said first contact hole (13B, 13C) having a first size and exposing a portion of said first lower conductive layer (11B, 11C), said second contact hole (13A) having a second size, larger than the first size, and exposing a portion of said second lower conductive layer (11A); and

forming a second wiring pattern (12) on said insulation film (14), said second wiring



pattern (12) including first and second upper conductive layers (12B, 12C; 12A) connected to said first and second lower conductive layers (11B, 11C; 11A) via said first and second contact holes (13B, 13C; 13A); said contact hole forming step including the steps of:

forming a resist film (18) covering said insulation film (14);

forming a resist pattern (18A) by photolithographic processing by exposing said resist film (18) to light using a mask pattern having a first defining area which defines said first contact hole (13B, 13C), and a second defining area which defines said second contact hole (13A); and

etching said insulation film (14) with said resist pattern (18A) being used as a mask; characterized by:

a compensation step effected when said semiconductor device is miniaturized to a degree at which said contact hole forming step makes the size of said first contact hole (13B, 13C) smaller than that of said first defining area while the size of said second contact hole (13A) remains equal to that of said second defining area; said compensation step including the substeps of:

determining the increase of said exposing light required to reduce the difference between the sizes of said first contact hole (13B, 13C) and said first defining area; and

determining the reduction in size of said second defining area to suppress the increase in size of said second contact hole (13A) above the second size under the increased amount of said exposing light.

2. A method according to claim 1, characterized in that said first size is less than 3 μm .
3. A method according to claim 2, characterized in that said second defining area is determined to be of a size reduced from the second size by approximately 0.6 μm when the second size is not less than 3 μm .
4. A method according to claim 3, characterized in that the distances between said first and second contact holes (13B, 13C; 13A) and the peripheries of said first and second lower conductive layers (11B, 11C; 11A) are determined as being approximately 0.7 μm to absorb an alignment error of said mask pattern.
5. A method according to claim 1, characterized in that said semiconductor body includes a semiconductor substrate (16) and an insulating film (15) formed on said semiconductor sub-

strate (16).

6. A method according to claim 5, characterized in that said semiconductor elements (10A, 10B) in the surface of said semiconductor substrate (16), and one of said first and second lower conductive layer (11B, 11C; 11A) are connected to one of said semiconductor elements (10A, 10B) through an opening formed in said insulating layer (15) and serving as an electrode for said semiconductor element.
7. A method according to claim 6, characterized in that said first wiring pattern (11) is formed of aluminium.

Patentansprüche

1. Verfahren zur Herstellung von Halbleitervorrichtungen, umfassend die Schritte:
Bilden eines ersten Verdrahtungsmusters (11) auf einem Halbleiterkörper (10A, 10B, 15, 16), wobei das Verdrahtungsmuster (11) die erste und die zweite Leitungsschicht (11B, 11C; 11A) umfaßt;
Bilden eines Isolationsfilms (14), der das erste Verdrahtungsmuster (11) überdeckt;
Bilden erster und zweiter Kontaktlöcher (13B, 13C, 13A) im Isolationsfilm (14), wobei das erste Kontaktloch (13B, 13C) eine erste Größe hat und einen Teil der ersten unteren Leitungsschicht (11B, 11C) freilegt, wobei das zweite Kontaktloch (13A) eine zweite Größe hat, die größer als die erste Größe ist, und einen Teil der zweiten unteren Leitungsschicht (11A) freilegt; und
Bilden eines zweiten Verdrahtungsmusters (12) auf dem Isolationsfilm (14) wobei das zweite Verdrahtungsmuster (12) die erste und die zweite obere Leitungsschicht (12B, 12C; 12A) umfaßt, die mit der ersten und der zweiten Leitungsschicht (11B, 11C; 11A) über die ersten und zweiten Kontaktlöcher (13B, 13C; 13A) verbunden sind; wobei der Schritt des Bildens des Kontaktlochs die Schritte umfaßt:
Bilden eines Abdeckfilms (18) der den Isolationsfilm (14) überdeckt;
Bilden eines Abdeckmusters (18A) durch ein photolithografisches Verfahren, indem der Abdeckfilm (18) belichtet wird unter Verwendung eines Maskenmusters mit einer ersten festlegenden Fläche, welche das erste Kontaktloch (13B, 13C) festlegt, und einer zweiten festlegenden Fläche, welche das zweite Kontaktloch (13A) festlegt; und
Ätzen des Isolationsfilms (14), wobei das Abdeckmuster (18A) als Maske verwendet wird; gekennzeichnet durch:



Einen Ausgleichsschritt, der ausgeführt wird, wenn die Halbleitervorrichtung auf einen Grad miniaturisiert wird, in dem der Schritt des Kontaktlochherstellens die Größe des ersten Kontaktlochs (13B, 13C) kleiner als diejenige der ersten festliegenden Fläche macht, während die Größe des zweiten Kontaktlochs (13A) gleich derjenigen der zweiten festliegenden Fläche bleibt; wobei der Ausgleichsschritt die Unterschritte enthält:

Bestimmen der Steigerung des Belichtungslichts, die benötigt wird, um die Differenz zwischen der Größe des ersten Kontaktlochs (13B, 13C) und der ersten festliegenden Fläche zu verringern; und

Bestimmen der Größenverringerung der zweiten festliegenden Fläche, um die Vergrößerung des zweiten Kontaktlochs (13A) über die zweite Größe unter dem zusätzlichen Einfall von Belichtungslicht zu unterdrücken.

2. Verfahren nach Anspruch 1 dadurch gekennzeichnet, daß die erste Größe weniger als 3 μm ist.
3. Verfahren nach Anspruch 2, dadurch gekennzeichnet, daß die zweite festlegende Fläche aus einer Größe festgesetzt ist, die bezüglich der Zweiten Größe um ungefähr 0,6 μm verringert ist, wenn die zweite Größe nicht weniger als 3 μm ist.
4. Verfahren nach Anspruch 3, dadurch gekennzeichnet, daß die Abstände zwischen den ersten und zweiten Kontaktlöchern (13B, 13C; 13A) und die Ränder der ersten und zweiten unteren Leitungsschichten (11B, 11C; 11A) so bestimmt sind, daß sie ungefähr 0,7 μm betragen, um einen Ausrichtungsfehler des Maskierungsmusters aufzunehmen.
5. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß der Halbleiterkörper ein Halbleitersubstrat (16) und einen Isolierfilm (15) umfaßt, der auf dem Halbleitersubstrat (16) gebildet ist.
6. Verfahren nach Anspruch 5, dadurch gekennzeichnet, daß die Halbleiterelemente (10A, 10B) in der Oberfläche des Halbleitersubstrats (16) und eine der ersten und zweiten unteren Leitungsschichten (11B, 11C; 11A) mit einem der Halbleiterelemente (10A, 10B) durch eine Öffnung verbunden sind, die in der Isolierschicht (15) hergestellt ist und als Elektrode für das Halbleiterelement dient.

7. Verfahren nach Anspruch 6, dadurch gekennzeichnet, daß das erste Verdrahtungsmuster (11) aus Aluminium gebildet ist.

5 Revendications

1. Procédé pour fabriquer des dispositifs semi-conducteurs, comprenant les étapes de :

formation d'un premier motif de câblage (11) sur un corps semi-conducteur (10A, 10B, 15, 16), ledit motif de câblage (11) comportant des première et seconde couches conductrices inférieures (11B, 11C; 11A);

formation d'une couche isolante (14) recouvrant ledit premier motif de câblage (11);

formation de premier et second trous de contact (13B, 13C, 13A) dans ladite couche isolante (14), ledit premier trou de contact (13B, 13C) ayant une première dimension et exposant une partie de ladite première couche conductrice inférieure (11B, 11C), ledit second trou de contact (13A) ayant une seconde dimension, supérieure à la première dimension, et exposant une partie de ladite seconde couche conductrice inférieure (11A); et

formation d'un second motif de câblage (12) sur ladite couche isolante (14), ledit second motif de câblage (12) comprenant des première et seconde couches conductrices supérieures (12B, 12C; 12A) reliées auxdites première et seconde couches conductrices inférieures (11B, 11C; 11A) via lesdits premier et second trous de contact (13B, 13C; 13A); ladite étape de formation des trous de contact comprenant les étapes de :

formation d'une couche de résist (18) recouvrant ladite couche isolante (14);

formation d'un motif de résist (18A) par un procédé de photogravure par l'exposition de ladite couche de résist (18) à la lumière en utilisant un motif de masque ayant une première zone de définition qui définit ledit premier trou de contact (13B, 13C), et une seconde zone de définition qui définit ledit second trou de contact (13A); et

gravure de ladite couche isolante (14) avec ledit motif de résist (18A) utilisé comme masque;

caractérisé par

une étape de compensation effectuée lorsqu'on miniaturise le dispositif semi-conducteur jusqu'à un degré auquel ladite étape de formation du trou de contact rend la dimension dudit premier trou de contact (13B, 13C) inférieure à celle de ladite première zone de définition alors que la dimension dudit second trou de contact (13A) reste égale à celle de ladite seconde zone de définition, ladite étape de

compensation comportant les sous-étapes de :

détermination de l'augmentation de ladite lumière de l'exposition nécessaire pour réduire la différence entre les dimensions dudit premier trou de contact (13B, 13C) et ladite première zone de définition; et

détermination de la diminution de dimension de ladite seconde zone de définition pour supprimer l'augmentation de dimension dudit second trou de contact (13A) au-dessus de la seconde dimension subissant la quantité augmentée de ladite lumière de l'exposition.



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2. Procédé selon la revendication 1, caractérisé en ce que ladite première dimension est inférieure à 3 μm . 15
3. Procédé selon la revendication 2, caractérisé en ce que ladite seconde zone de définition est déterminée pour avoir une dimension réduite à partir de la seconde dimension de 0,6 μm approximativement lorsque la seconde dimension n'est pas inférieure à 3 μm . 20
4. Procédé selon la revendication 3, caractérisé en ce que les distances entre lesdits premier et second trous de contact (13B, 13C; 13A) et les pourtours desdites première et seconde couches conductrices inférieures (11B, 11C; 11A) sont déterminés comme étant approximativement de 0,7 μm pour absorber une erreur d'alignement dudit motif de masque. 25
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5. Procédé selon la revendication 1, caractérisé en ce que ledit corps semi-conducteur comprend un substrat semi-conducteur (16) et une couche isolante (15) formée sur ledit substrat semi-conducteur (16). 35
6. Procédé selon la revendication 5, caractérisé en ce que lesdits éléments semi-conducteurs (10A, 10B) dans la surface dudit substrat semi-conducteur (16), et une desdites première et seconde couches conductrices inférieures (11B, 11C; 11A) sont reliés à un desdits éléments semi-conducteurs (10A, 10B) via une ouverture formée dans ladite couche isolante (15) et servant comme électrode pour ledit élément semi-conducteur. 40
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7. Procédé selon la revendication 6, caractérisé en ce que ledit premier motif de câblage (11) est formé en aluminium. 55