"A semiconductor device and a process for producing the same"

The present invention relates to a semiconductor device, particularly a static memory device employing FET's (field effect transistors), and a process for producing such a device.

The memory portion of a static memory semiconductor device consists of a plurality of memory cells, each made up of a plurality of MOS FET's. In the cells, the electrodes have hitherto been connected to the source or drain regions of the MOS FET by aluminum wiring. However, the memory portion occupies a very large area in a chip in which the device is formed, and this area must be reduced if it is desired to increase the degree of integration of the devices.

In an attempt to reduce the area of the memory portion or to reduce the size of the memory cell, attempts have been made, as illustrated in Figs. 1 and 2 of the accompanying drawings (which respectively show a plan view of a portion of a MOS FET of a conventional memory cell and a section thereof on line A-A'), to connect a wiring 8 of polycrystalline silicon directly to the source or drain region 7 which is surrounded by a field SiO_2 film 5 and a polycrystalline silicon gate 6.

However, the silicon wiring 8 is composed of a layer that is formed simultaneously with the silicon gate 6, and is usually doped with phosphorus ions at high concentration to reduce its resistance. The phosphorus ions are doped simultaneously with the formation of the source region and the drain region. While the phosphorus ions are being doped, the depth of the n^+-type diffusion layer 7 increases beneath the wiring 8, i.e. the layer 7 swells beneath the gate 6 as indicated by a dotted line 10 in Fig. 2. This makes it difficult to obtain an MOSFET having a desired channel length or a desired shallow source region or drain region. To prevent this a sufficient distance d_1 must be provided between one end of the gate 6 and the end of the wiring 8. This, however, does not help in reducing the size of the cell; the degree of integration of the semiconductor device is not increased.

The present inventors have contrived a method by which the polycrystalline silicon gate 6 and the polycrystalline silicon wiring 8 are formed as shown in Fig. 3, and are covered by an insulating film 9 such as PSG (phosphorus silicate glass). A portion of the insulating film 9 is then selectively removed by photoetching, and an aluminum wiring 10 is formed in order to connect the semiconductor region 7

to the wiring 8. It has, however, been discovered that, when the aluminum layer is brought into direct contact with the semiconductor region (source or drain region), there is formed an aluminum-silicon alloy which destroys a pn junction to a depth of about 1 μm in the source or drain region.

An object of the present invention therefore is to provide an MOSFET which enables the degree of integration to be increased.

Embodiments of the invention will now be described by way of example with reference to the accompanying drawings, in which:-

Figs. 1 and 2 have been mentioned above;

Fig. 3 is a section view of an MOSFET also mentioned above;

Fig. 4 is a plan view of a static memory device embodying the present invention;

Fig. 5 is a circuit diagram of a memory cell in the memory device;

Fig. 6 is a plan view of a MOSFET embodying the present invention;

Fig. 7 is a section view of the MOSFET of Fig. 6 along the line A-A';

Figs. 8(a) to 8(f) are section views showing steps in a process for producing the MOSFET of Fig. 7;

Figs. 9(a) to 9(f) are section views showing steps in a process for producing the MOSFET in another embodiment of the present invention; and

Figs. 10(a) to 10(f) are section views showing steps in a process for producing a CMOSIC embodying the present invention.

Referring to Fig. 4, the static memory device shown embodying the invention has a memory portion (memory array) 2 which consists of a plurality of single-channel (for example, n-channel) MOSFET's formed in a well region which is a portion of a silicon semiconductor chip 1. A peripheral circuit 3 consisting of complementary MOSFET's is formed alongside the memory portion 2 to drive it. The required number of bonding pads (terminals) 4 are formed around the periphery of the chip 1.

The memory cell for a single bit consists of four MOSFET's Q_1, Q_2, Q_3 and Q_4 and load resistors R_1 and R_2 as shown in Fig. 5 in which V_{CC} denotes a power supply of a voltage of, for example, +5 volts, W denotes a word line, and D_1 and D_2 denote data lines.

Figs. 6 and 7 show a MOSFET which constitutes the memory cell of Fig. 5. An SiO_2 film (gate

insulation film) 13 of a thickness smaller than a field SiO_2 film 12 is formed on the surface of a region (active region) in a portion of a p-type substrate that is surrounded by the thick field SiO_2 film 12. On the SiO_2 film 13 is selectively formed a gate polycrystalline silicon layer 14 which extends transversely across the active region. Polycrystalline silicon wirings 15 and 15' are selectively formed so as to extend from the SiO_2 film 13 to the field SiO_2 film 12 in a direction at right angles to the gate layer 14. An n^+-type source region 16 and an n^+-type drain region 17 are formed in the surface of the active region which is surrounded by the gate layer 14, the film 12, and the wirings 15,15'.

A second polycrystalline silicon wiring layer 19, 19' has a part 19 which makes direct contact with a portion of the surface of the source region 16 and with a portion of the surface of the wiring layer 15. Another part 19' of the second wiring layer 19,19' makes direct contact with a portion of the surface of the drain region 17 and with a portion of the surface of the wiring layer 15'. An aluminum wiring 21 is connected to the wiring layer 15'.

The process for producing the MOSFET of Figs. 6 and 7 will be described below with reference to

Figs. 8(a) to 8(f).

Referring to Fig. 8(a), first, a field SiO_2 film 12 is formed on one main surface of a p-type silicon substrate 11 by the low-temperature selective oxidation method, and an SiO_2 film (gate insulation film) 13 of a thickness less than that of the film 12 is formed on the surface of the active region surrounded by the

SiO_2 film 12. Then, polycrystalline silicon is deposited on the whole , of the field SiO_2 film 12 and the gate SiO_2 film 13, and is doped with phosphorus ions of a relatively high concentration to decrease its resistance. The polycrystalline silicon is then subjected to the selective photoetching, in order to form a polycrystalline silicon gate 14 and first polycrystalline silicon wiring layers 15, 15'.

Referring to Fig. 8(b), n-type impurities are introduced into the surface of the p-type silicon substrate 11 with the polycrystalline silicon gate 14 and first polycrystalline silicon wiring layers 15, 15' as a mask, in order to form, in the p-type substrate, a semiconductor region that forms a pn junction relative to the substrate. For instance, n-type impurity ions of phosphorus or arsenic are injected into the p-type silicon substrate 11, followed by the annealing (heat treatment), to form the n^+-type source region 16 and drain region 17 having a desired depth in the p-type silicon substrate 11.

Referring to Fig. 8(c), an SiO_2 film 18 is formed as a first interlayer insulation film on the whole surface of the p-type substrate 11 by the thermal oxidation method or the CVD (chemical vapor deposition) method. Then, portions of the surface of the source region 16 and the drain region 17 are exposed by the contact photoetching.

Referring to Fig. 8(d), a second polycrystalline silicon layer is deposited on the whole surface of the substrate 11, and is doped with phosphorus ions of a relatively small concentration. Then, unnecessary portions of the polycrystalline silicon are removed by patterning. Thus, there are formed second polycrystalline silicon wiring layers 19,19' to connect the source region 16 and the drain region 17 to the first polycrystalline silicon wiring layers 15,15'.

Referring to Fig, 8(e), the first polycrystalline silicon wiring layer 15' is selectively exposed and, then, a PSG (phosphorus silicate glass) film 20 is deposited on the whole surface of the p-type substrate 11 to form a second interlayer insulation film (or passivation film).

Referring to Fig. 8(f), portions of the second interlayer insulation film 20 are selectively removed, and an aluminum wiring (third wiring) 21 which connects to the second polycrystalline silicon wiring layer is formed by vaporizing aluminum.

Thus, in this embodiment of the present invention which makes use of a polycrystalline silicon wiring layer (second polycrystalline silicon wiring layer) in addition to the gate wiring layer (first polycrystalline silicon wiring layer) and electrode wiring of aluminum as mentioned above, it is possible to connect the first polycrystalline silicon

wiring layer to a semiconductor region such as source region or drain region selectively formed in the substrate via the second polycrystalline silicon wiring layer. Therefore, there is no need to deeply form the semiconductor region, or to increase the distance between the gate wiring 14 and the first polycrystalline silicon wiring layers 15,15', or between the gate wiring 14 and the second polycrystalline silicon wiring layers 19,19'. Consequently, the degree of integration of the semiconductor devices can be increased. Further, since aluminum is not directly connected to the diffusion layer, there takes place no Al-Si reaction which destroys the pn junction.

Figs. 9(a) to 9(f) are section views showing the steps in a process for producing an MOSFET which constitutes the memory of Fig. 5 according to another embodiment of the present invention.

Referring to Fig. 9(a), a field SiO_2 film 42 is formed on one main surface of a p-type silicon substrate 41 by the low-temperature selective oxidation method, and an SiO_2 film (gate insulation film) 43 having a thickness smaller than that of the field SiO_2 film 42 is formed on the surface of the active region surrounded by the field SiO_2 film 42. Then, polycrystalline silicon is deposited

on the whole surfaces of the field SiO_2 film 42 and the gate SiO_2 film 43, and is doped with phosphorus ions of a relatively high concentration to reduce its resistance. The polycrystalline silicon is then subjected to the selective photoetching to form a polycrystalline silicon gate 44 and first-layer polycrystalline silicon wirings 45,45'. In this case, the polycrystalline silicon wirings 45,45' are not permitted to extend onto the gate SiO_2 film 43.

Referring to Fig. 9(b), n-type impurities are introduced into the surface of the p-type silicon substrate 41 with the polycrystalline silicon gate 44 and the field SiO_2 film 42 as a mask, thereby to form, in the p-type substrate, a semiconductor region that forms a pn junction with respect to the substrate. For example, n-type impurity ions such as phosphorus ions or arsenic ions are introduced into the p-type silicon substrate 41 by the ion injection, followed by annealing (heat treatment) to form the n^+-type source region 46 and drain region 47 having a desired depth in the p-type silicon substrate 41.

Referring to Fig. 9(c), an SiO_2 film 48 is formed as a first interlayer insulation film on the whole surface of the p-type substrate 41 by the thermal oxidation method or the CVD (chemical vapor deposition) method. Then, portions of the surface of the source

region 46 and the drain region 47 are exposed by the contact photoetching. In this case, portions of the first polycrystalline silicon wiring layers 45,45' are also exposed.

Referring to Fig. 9(d), a second polycrystalline silicon layer is deposited on the whole surface of the substrate 41, and is doped with phosphorus ions of a relatively small concentration. Thereafter, unnecessary portions of the polycrystalline silicon are removed by patterning. Thus, there are formed second polycrystalline silicon wiring layers 49,49' to connect the source region 46 and the drain region 47 respectively to the first polycrystalline silicon wiring layers 45,45'.

Referring to Fig. 9(e), the first polycrystalline silicon wiring layer 45' is selectively exposed, and a PSG (phosphorus silicate glass) film 50 is deposited on the whole surface of the p-type substrate 41 to form a second interlayer insulating film (or passivation film).

Referring to Fig. 9(f), a portion of the second interlayer insulation film 50 is selectively removed, and an aluminum wiring (third wiring) 51 which connects to the first polycrystalline silicon wiring layer 45' is formed by vaporizing aluminum.

According to the above-mentioned embodiment, the first polycrystalline silicon wiring layers 45,45' are not permitted to extend onto the gate SiO_2 film 43, but terminate on the thick field SiO_2 film 42. Therefore, the areas of the source region 46 and the drain region 47 can be reduced. In other words, the degree of integration of memory cells can be increased.

Figs. 10(a) to 10(f) illustrate a process when the present invention is adapted to the manufacture of a complementary MOSIC. This will be described below for each of the manufacturing steps.

Referring, first, to Fig. 10(a), boron ions are injected into a portion of the surface of an n-type silicon substrate 23 to form a p-type well region 24. A field SiO_2 film 25 is selectively formed on the surface of the n-type substrate 23 and the well region 24. Then, an SiO_2 film 26 of a thickness of about 380 angstroms is formed by gate oxidation on regions of the surface of the n-type substrate 23 and the well region 24 that are surrounded by the field SiO_2 film 25. Then, the polycrystalline silicon is deposited to a thickness of about 3500 angstroms, and is doped with phosphorus ions (at 1000°C, for 5 minutes, 20 minutes and 5 minutes). A polycrystalline silicon gate 27 and a first polycrystalline silicon wiring layer 28 are formed by photoetching the polycrystalline silicon.

Referring to Fig. 10(b), the surfaces of the polycrystalline silicon gate 27 and the first polycrystalline silicon wiring layer 28 are lightly oxidized at a temperature of 850°C, and an Si_3N_4 is deposited on the whole surface of the substrate to a thickness of 1000 angstroms. Thereafter, only the Si_3N_4 is selectively removed by etching from the surface of the p-type well region 24. Namely, the Si_3N_4 film 29 is left on the surface of the n-type substrate 23 on which the p-type well region 24 has not been formed. Arsenic ions are introduced into the p-type well region by the injection method using the Si_3N_4 film 29 as a mask. Thereafter, an n^+-type source and drain regions 30 are formed by annealing. Then, by using the Si_3N_4 film 29 as a mask for selective oxidation, the low-temperature selective oxidation is effected to increase the thickness of the SiO_2 film 31 on the surfaces of the polycrystalline silicon gate 27, first polycrystalline silicon wiring layer 28, and on the surface of the source or drain region 30.

Referring to Fig. 10(c), the Si_3N_4 film 29 is removed by hot phosphoric acid, and an Si_3N_4 film 32 is newly deposited to a thickness of about 500 angstroms. A portion of the source or drain region 30 is exposed by effecting the contact photoetching onto the Si_3N_4 film 32 and the underlying SiO_2 film 31. A PSG

(phosphorus silicate glass) film 33 is then deposited on the whole surfaces of the n-type substrate 11 and the well region 24, and is annealed at 1000°C in a nitrogen atmosphere.

Referring to Fig. 10(d), a portion of the PSG film 33 is removed by etching, and boron ions are introduced into the p-channel side (n-type substrate) by the ion injection method through the Si_3N_4 film 32. Thus, the p-type source and drain regions 37 are formed.

Referring to Fig. 10(e), the PSG film 33 is removed to expose the surface of the n^+-type diffusion regions 30 and the first polycrystalline silicon wiring layer 28 on the n-channel side (p-well side). A second polycrystalline silicon layer 34 (3500 angstroms) is deposited on the p-channel side and on the n-channel side, and the polycrystalline silicon layer 34 is doped with phosphorus ions while masking the second polycrystalline silicon layer 34 on the p-channel side. Thereafter, unnecessary portions of the polycrystalline silicon layer 34 are removed by photoetching. Thus, the second polycrystalline silicon wiring 34 is formed which connects to the N^+-type region 30 and to the first polycrystalline silicon wiring layer 28.

Referring to Fig. 10(f), the second polycrystalline silicon wiring layer 34 is lightly oxidized,

a PSG film 35 is deposited thereon to a thickness of about 6000 angstroms followed by annealing in a nitrogen atmosphere, and the films are selectively removed by the contact photoetching. Then, aluminum is deposited followed by patterning to form an aluminum wiring (electrode) 36 that connects to the p^+-type diffusion region 37 and to the second polycrystalline silicon wiring layer 34.

In the CMOS device obtained by the above-mentioned process, the aluminum wiring 36 is connected at a portion to the diffusion region (p^+) 37, and is connected at another portion to the diffusion region (n^+) 30 via the second polycrystalline silicon wiring layer 34. At still another portion, furthermore, the aluminum wiring 36 is connected to the first polycrystalline silicon wiring layer 28 via the second polycrystalline silicon wiring layer 34.

As mentioned in the foregoing, the first wiring layer or the third aluminum wiring layer is connected to the diffusion regions via the second wiring layer. Therefore, increased freedom is provided for laying out the wiring. Consequently, the degree of integrating the semiconductor devices can be increased, for example, by 10 to 20%.

The present invention can be effectively adapted to the MOS memory devices having polycrystalline silicon wirings of a multi-layer construction, and especially to static memory devices manufactured by the CMOS process.

~~Attention is drawn to the disclosure and claims of divisional application no. 84.03595 (publication no.).~~

CLAIMS

1. A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a first insulating film formed on a main surface of said semiconductor substrate so as to surround an area of said main surface which area forms the surface of an active region in a portion of the semiconductor substrate;

a second insulating film, of a thickness smaller than said first insulating film, formed on the surface of said active region;

a first conductive layer selectively formed on part of said seccnd insulating film so as to traverse said active region;

a second conductive layer selectively formed so as to extend at least over part of said first insulating film, said second conductive layer being separated from said first conductive layer;

a first semiconductor region, of a seccnd conductivity type opposite to the first conductivity type, formed in a first surface portion of said active region which is surrounded by said first conductive layer, said second conductive layer and said first insulating film;

a second semiconductor region, of said second conductivity type, formed in a second surface portion of said active region which is surrounded by said first conductive layer and said first insulating film and which is positioned on the opposite side of said first conductive layer from said first surface portion;

a third insulating film which at least partly covers said first and second conductive layers and has at least one hole so formed that a portion of said first semiconductor region and a portion of said second conductive layer are exposed; and

a third conductive layer in the form of a polycrystalline silicon layer which is formed in said hole(s) and makes a connection with said first semiconductor region and said second conductive layer.

2. A semiconductor device according to claim 1 wherein said second conductive layer is selectively formed on part of said second insulating film and extends therefrom over part of said first insulating film.

3. A semiconductor device according to claim 1 or claim 2 wherein said third conductive layer fills the whole area (as seen in plan) of said hole(s) in said third insulating film.

4. A semiconductor device according to any one of claims 1 to 3, wherein said first conductive layer serves as a gate electrode.

5. A semiconductor device according to any one of the preceding claims wherein said first insulating film consists of SiO_2.

6. A semiconductor device according to any one of the preceding claims, wherein said second insulating film consists of SiO_2.

7. A semiconductor device according to any one of the preceding claims, wherein a metal wiring is connected to a portion of the second conductive layer.

8. A semiconductor device according to any one of the preceding claims, wherein the first semiconductor region serves as a drain region, and the second semiconductor region serves as a source region.

9. A semiconductor device according to any one of the preceding claims wherein said first and second conductive layers are polycrystalline silicon layers.

10. A semiconductor device according to claim 9 wherein said first and second conductive polycrystalline silicon layers are doped with impurities of the second conductivity type at a concentration sufficient to decrease the resistance thereof substantially.

11. A semiconductor device according to claim 10, wherein said third polycrystalline silicon conductive layer is doped with impurities of the second conductivity type at a relatively lower concentration than said first and second polycrystalline layers.

12. A semiconductor device according to any one of the preceding claims, wherein said second conductive layer is formed so as to have a direction of elongation at right angles to a direction of elongation of the first conductive layer.

13. A semiconductor device according to any one of the preceding claims, wherein the third conductive layer is connected to the second conductive layer at a position on said second insulating film.

14. A semiconductor device according to any one of the preceding claims, wherein said first and second insulating films and said active region are formed in a well region of the first conductivity type formed in said semiconductor substrate.

15. A semiconductor device according to claim 14, wherein the semiconductor substrate is of n-type, and the well region is of p-type.

16. A semiconductor device substantially as herein described with reference to and as shown in Figs. 6 to 8, Fig. 9 or Fig. 10 of the accompanying drawings.

17. A process for producing a semiconductor device comprising the steps of:

forming a first insulating film on a main surface of a semiconductor substrate so as to surround an area of said main surface which area is to define the surface of an active region in a portion of the semiconductor substrate;

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forming a second insulating film, of a thickness smaller than said first insulating film, on at least one part of the surface of said active region;

depositing a first conductive layer over said first and second insulating films;

patterning said first conductive layer thereby to form a first wiring on said second insulating film which traverses said active region, and to form a second wiring extending at least on said first insulating film, said second wiring being separated from said first wiring;

introducing impurities, of a conductivity type opposite to that of said semiconductor substrate, into a first portion of said active region which is surrounded by said first wiring, said second wiring and said first insulating film, and into a second portion of said active region which is surrounded by said first wiring and said first insulating film and which is positioned on the opposite side of said first wiring from said first portion, thereby to form a first semiconductor region and a second semiconductor region at said first portion and said second portion, respectively;

forming a third insulating film over said first and second wirings;

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forming at least one hole in said third insulating film thereby to expose a portion of said first semiconductor region and a portion of said second wiring;

depositing a second conductive layer in the form of a polycrystalline silicon layer over said third insulating film and in said hole(s); and

patterning said second polycrystalline silicon conductive layer thereby to form a third wiring which is connected at said hole(s) to said first semiconductor region and to said second wiring.

18. A process according to claim 17 wherein said third wiring is formed so as to extend over part of said second insulating film and therefrom over part of said first insulating film.

19. A process according to claim 17 or claim 18, wherein the first and second insulating films each consist of SiO_2.

20. A process according to any one of claims 17 to 19 wherein said first conductive layer is a polycrystalline layer.

21. A process according to claim 20 further including introducing impurities, of a conductivity type opposite to that of the semiconductor substrate, into the first polycrystalline silicon layer before patterning thereof, and introducing impurities, of a conductivity type opposite to that of the semiconductor substrate, into the second polycrystalline silicon film before patterning thereof.

22. A process for producing a semiconductor device substantially as herein described with reference to Fig. 8, Fig. 9 or Fig. 10.