

ABSTRACT

A memory device is provided. The memory device includes: a memory cell array including a first string provided in a first layer and a second string provided in a second layer stacked on the first layer; a page buffer circuit including a first page buffer corresponding to the first string of the first layer and a second page buffer corresponding to the second string of the second layer; and a control logic circuit configured to control the first page buffer and the second page buffer independently, in a core operation.

FIG. 1