

## Description

This invention relates to memory circuits, and more particularly, to memory circuits for which column lines are precharged prior to reading data thereon.

### Background of the Invention

Precharging column lines of a memory prior to reading data has been an effective technique for improving speed and power. The precharging can occur in response to a timing signal or a signal generated in response to an address transition. Such a signal generated for precharging column lines is often known as an equalization pulse because it equalizes the voltage on the column lines, particularly for memories for which there are two bit lines for each column. One bit line carries the true data bit and the other carries the complementary data bit. Upon being precharged in response to an equalization pulse, the two bit lines are equalized in voltage. The technique is particularly popular for static random access memories (SRAMs).

One aspect of precharging is that a significant amount of charge is required to charge all of the columns due to the substantial capacitance of each bit line. At a typical operating speed, the power required for precharging is typically more than half of the entire power requirements of the memory. One technique to reduce power consumption is to precharge only one half of the array, the half from which the data is to be selected. A predetermined address bit which indicates which half contains the selected data is also used to determine which half is precharged. For a byte-wide memory, a memory which provides eight parallel bits of data for a single address, the technique of precharging only half of the array has resulted in doubling the required sense amplifiers and output drivers as well as a reduction in speed. The array is divided into left and right halves. The left and right halves are each further divided into eight planes. Consequently, each half is capable of supplying a byte. Each half has its own set of eight sense amplifiers and output drivers. The half which is to provide the byte of data is precharged. The outputs of the output drivers associated with the selected half are coupled to the output pads of the memory while the outputs of the output drivers associated with the unselected and unprecharged half are decoupled from the output pads.

Having as disclosed in EP-A-0069588 an architecture of a byte on the left half of the array and a byte on the right half of the array does allow for reducing the power consumption due to precharging by one half. There are other problems created, however. There are sixteen sense amplifiers

and output drivers instead of eight. The routing of the output is complicated. The distance between the outputs of the output drivers and the output pads is increased, increasing capacitance. Also the post-decoding transistors for coupling drivers of the selected half to the output pads add resistance to the current path which is intended to be a minimum resistance path because it is the path which provides the actual output drive. In order to achieve the reduced power, chip area is increased due to the additional circuitry and routing, and speed is reduced due to increased capacitance and resistance in the output current path.

### Summary of the Invention

The present invention seeks to provide an integrated circuit random access memory in which the above problems are mitigated.

In accordance with the present invention there is provided an integrated circuit random access memory for providing a predetermined number of data bits as an output in a read mode and for receiving the predetermined number of data bits in a write mode, comprising:

a left array comprised of a first plurality of adjacent left subarrays on a left side of the memory; and

a right array comprised of a second plurality of adjacent right subarrays on a right side of the memory;

characterized by further comprising:

a first amplifier coupled to the left array, for providing as a first portion of the output of the memory a first half of the predetermined number of data bits received from a selected one of the adjacent left subarrays; and

a second amplifier coupled to the right array, for providing as a second portion of the output of the memory a second half of the predetermined number of data bits received from a selected one of the adjacent right subarrays;

the selected one of said left subarrays providing, in parallel, the first half of the predetermined number of said data bits; and

the selected one of said right subarrays providing, in parallel, the second half of the predetermined number of said data bits and further characterized in that only the selected one of said left subarrays and the selected one of said right subarrays are precharged in response to an equalization pulse.

### Brief Description of the Drawings

FIG. 1 is a layout of a memory array and output pads of a memory according to a preferred embodiment of the invention.

FIG. 2. is an circuit diagram of a memory cell which may be used in the memory array of FIG. 1.

FIG. 3 is a layout of a portion of an interface between the memory array and output pads of FIG. 1.

#### Description of a Preferred Embodiment

Shown in FIG. 1 is a layout of a memory circuit 10 comprised generally of a precharging circuit 11, a memory array 12, an amplifier-driver 13, an amplifier-driver 14, and a plurality of pads 16. Memory array 12 is comprised of a left half 17, a right half 18, and a power carrier region 19 interposed therebetween. Left half 17 is comprised of a portion 21, and portion 22, and a row decoder 23 interposed therebetween. Right half 18 is comprised of a portion 24, a portion 25, and a row decoder 26 interposed therebetween. Plurality of pads 16 is comprised of a power supply pad 27 for  $V_{ss}$  which is typically connected to ground, an output pad 28 for providing a data output signal  $Q_0$ , an output pad 29 for providing a data output signal  $Q_1$ , an output pad 30 for an output signal  $Q_2$ , an output pad 31 for an output signal  $Q_3$ , an output pad 32 for an output signal  $Q_4$ , an output pad 33 for an output signal  $Q_5$ , an output pad 34 for an output signal  $Q_6$ , and an output pad 35 for an output signal  $Q_7$ . The relative position of pads 28-35 shown in FIG. 1 is that of industry-standard byte-wide SRAMs. Pads 28-35 extend from left to right in consecutive order corresponding to output signals  $Q_0$  to  $Q_7$  with  $V_{ss}$  pad 27 interposed between  $Q_2$  pad 30 and  $Q_3$  pad 31.

Shown in FIG. 2 is a conventional memory cell 36 comprised of a word line 37, two cross-coupled transistors 38 and 39, two coupling transistors 40 and 41, and two loads 42 and 43. Memory cell 37 provides complementary data on bit sense lines 44 and 45 in response to receiving a signal on word line 37. Each portion 21, 22, 24, and 25 of memory array 12 is comprised of a plurality of memory cells, which may be for example, like memory cell 36 of FIG. 2. The memory cells are at intersections of rows and columns. Using memory cell 36 as an example, a single row would be word line 37 and a single column would be bit lines 44 and 45. Prior to reading data from memory cell 36, bit lines 44 and 45 would both be precharged in a conventional manner.

Precharge circuit 11 has a first input for receiving an equalization pulse EQ, a second input for receiving address signal  $A_p$ , a third input for receiving complementary address signal  $\bar{A}_p$ , a first output coupled to portions 21 and 24, and a second output coupled to portions 22 and 25. Portions 21, 22, 24, and 25 are arranged in an adjacent, side-by-side manner. Portion 21 is adjacent to portion

22. Portion 22 is between portion 21 and 24. Portion 23 is between portions 22 and 25. Portion 25 is adjacent to portion 24. Portion 21 has four outputs  $L_0$ ,  $L_1$ ,  $L_2$ , and  $L_3$  coupled to amplifier-driver 13. Portion 22 has four outputs  $R_0$ ,  $R_1$ ,  $R_2$ , and  $R_3$  coupled to amplifier-driver 13. Portion 24 has four outputs  $L_4$ ,  $L_5$ ,  $L_6$ , and  $L_7$  coupled to amplifier-driver 14. Portion 25 has four outputs,  $R_4$ ,  $R_5$ ,  $R_6$ , and  $R_7$  coupled to amplifier-driver 14. Amplifier-driver 13 has outputs  $Q_0$ ,  $Q_1$ ,  $Q_2$ , and  $Q_3$  connected to output pads 28, 29, 30, and 31, respectively. Amplifier-driver 14 has outputs  $Q_4$ ,  $Q_5$ ,  $Q_6$ , and  $Q_7$  connected to output pads 32, 33, 34, and 35, respectively. Address signals  $A_p$  and  $\bar{A}_p$  are coupled to amplifier-drivers 13 and 14. The arrangement of the output pads 28-35 shown in FIG. 1, as stated previously, is that of a conventional byte-wide SRAM. The output pads 28-35 are arranged in order of output bits,  $Q_0$  -  $Q_7$  with a pad 27 for coupling to  $V_{ss}$ , typically ground, interposed between the output pads which provide bits  $Q_2$  and  $Q_3$ .

In operation, circuit 10 responds to an equalization pulse EQ and address signals  $A_p$  and  $\bar{A}_p$  by precharging half of array 12 and then providing bits  $Q_0$  -  $Q_7$  from the precharged half. In response to pulse EQ and the logic state of signals  $A_p$  and  $\bar{A}_p$ , precharging circuit 11 precharges either portions 21 and 24 or portions 22 and 25. If signal  $A_p$  is a logic high then the half of array 12 comprised of portions 21 and 24 is precharged. If signal  $A_p$  is a logic low, then the half of array 12 comprised of portions 22 and 25 is precharged. Amplifier-drivers 13 and 14 provide the data from the precharged half to pads 28-35. If signal  $A_p$  is a logic high, then amplifier-driver 13 provides output bits  $Q_0$  -  $Q_3$  as represented by signals  $L_0$  -  $L_3$ , respectively and amplifier-driver 14 provides output bits  $Q_4$  -  $Q_7$  as represented by signals  $L_4$  -  $L_7$ , respectively. If signal  $A_p$  is a logic low, then amplifier-driver 13 provides output bits  $Q_0$  -  $Q_3$  as represented by signals  $R_0$  -  $R_3$ , respectively and amplifier-driver 14 provides output bits  $Q_4$  -  $Q_7$  as represented by signals  $R_4$  -  $R_7$ , respectively.

Shown in FIG. 3, in more detail and in layout form, are left half 17 of memory array 12 and amplifier-driver 13. Amplifier-driver 13 comprises an  $A_p$  coupler 46, a  $Q_0$  amplifier 47, a  $Q_1$  amplifier 48, a  $Q_2$  amplifier 49, a  $Q_3$  amplifier 50, and a  $\bar{A}_p$  coupler 51. Coupler 46 comprises transistors 52-59. Coupler 51 comprises transistor 60-67. Each of the transistors 52-59 has a gate for receiving signal  $A_p$ . Each of the transistors 60-67 has a gate for receiving signal  $\bar{A}_p$ . There is a pair of transistors associated with each of signals  $L_0$  -  $L_3$  and  $R_0$  -  $R_3$  as follows; transistors 52 and 53 with signal  $L_0$ , transistors 54 and 55 with signal  $L_1$ , transistors 56 and 57 with signal  $L_2$ , transistors 58 and 59 with

signal  $L_3$ , transistors 60 and 61 with signal  $R_0$ , transistors 62 and 63 with signal  $R_1$ , transistors 64 and 65 with signal  $R_2$ , transistors 66 and 67 with signal  $R_3$ . Each amplifier 47-50 is coupled to a pair of transistors of both couplers 46 and 51 by a pair of conductors 69, 70, 71 and 72, respectively. Conductor pair 69 connects transistor pair 52-53 and transistor pair 60-61 to  $Q_0$  amplifier 47. Conductor pair 70 connects transistor pair 54-55 and transistor pair 62-63 to  $Q_1$  amplifier 48. Conductor pair 71 connects transistor pair 56-57 and transistor pair 64-65 to  $Q_2$  amplifier 49. Conductor pair 72 connects transistor pair 58-59 and transistor pair 66-67 to  $Q_3$  amplifier 50. Each signal  $L_0 - L_3$  and  $R_0 - R_3$  has a true and complementary representation. When a logic high is received on the gates of the transistors of a transistor pair, that transistor pair couples the true and complementary representation of the signal, one of  $L_0 - L_3$  and  $R_0 - R_3$ , with which it is associated to the conductor pair, one of 69-72, to which it is connected. Accordingly, when signal  $A_p$  is a logic high, transistor pair 52-53 couples signal  $L_0$  to  $Q_0$  amplifier 47 via conductor pair 69, transistor pair 54-55 couples signal  $L_1$  to  $Q_1$  amplifier 48 via conductor pair 70, transistor pair 56-57 couples signal  $L_2$  to  $Q_2$  amplifier 49 via conductor pair 71, and transistor pair 58-59 couples signal  $L_3$  to  $Q_3$  amplifier 50 via conductor pair 72. With signal  $A_p$  at a logic high, signal  $\bar{A}_p$  is a logic low which turns off transistors 60-67 to prevent interference with signals  $L_0 - L_3$  which are carried on conductors 69-72. In the same way when signal  $A_p$  is a logic low and  $\bar{A}_p$  is a logic high, transistor pairs 60-61, 62-63, 64-65, and 66-67 couple signals  $R_0 - R_3$ , respectively, to amplifiers 47-50, respectively, and transistors 52-59 are turned off. Amplifiers 47-50 sense and amplify the logic state of the received signal to provide output bits  $Q_0 - Q_3$ .

Each signal  $L_0 - L_3$  and  $R_0 - R_3$  is representative of a logic state of a memory cell such as memory cell 36 of FIG. 2. Memory portion 21 is comprised of memory planes 69, 70, 71, and 72 each of which has a plurality of memory cells located at intersecting rows and columns. Likewise, portion 22 is comprised of memory planes 73, 74, 75, and 76 each of which has memory cells located at intersecting rows and columns. Planes 69-76 provide signal  $L_0 - L_3$  and  $R_0 - R_3$ , respectively. When signal  $A_p$  is a logic high, planes 69-72 are precharged. A cell from each plane 69-72 is then selected. Signals  $L_0 - L_3$  are provided as representative of the logic state of the selected memory cells. With signal  $A_p$  at a logic high, signals  $L_0 - L_3$  are coupled to amplifier 47-50 which in turn provide output bits  $Q_0 - Q_3$  at the logic state indicated by signal  $L_0 - L_3$ . When signal  $A_p$  is a logic low and  $\bar{A}_p$  is a logic high, planes 73-76 are precharged. A cell from each plane 73-76 is selected. Signals  $R_0 - R_3$

are provided as representative of the logic state of the selected memory cells. With signal  $\bar{A}_p$  at a logic high, signals  $R_0 - R_3$  are coupled to amplifiers 47-50 which in turn provide output bits  $Q_0 - Q_3$  at the logic state indicated by signals  $R_0 - R_3$ . Thus it is shown that only four amplifiers, amplifiers 47-50, are needed for the left half 17 of the array 12. The same structure as shown in FIG. 3 for left half 17 is also provided for right half 18. As is shown in FIG. 1 and 3 there is no required decoding between amplifiers 47-50 and pads 28-31. With the same structure for amplifier-driver 14 as is shown for amplifier-driver 13 shown in FIG. 3, there is also no required decoding between amplifier-driver 14 and pads 32-35. Also the conductive paths between amplifier-drivers 13-14 and pads 28-35 do not cross each other. Accordingly, the conductive paths between amplifier-drivers 13-14 and pads 28-35 are uninterrupted. Consequently, the highest conductivity interconnect, for example, metal, is used.

FIG. 3 further shows that conductor pairs 69-72 are uninterrupted between couplers 46 and 51. Conductor pairs 69-72 can thus be made from the highest conductivity material, for example metal, available for making interconnect for memory circuit 10. Connections between transistors 52-59 and conductors 69-72 can be made by conventional metal to diffusion contacts. Transistor diffusion can be made to extend under conductors 69-72 by conventional fabrication techniques. Diffusions are also relatively low resistance so that outputs of memory cells which provide signals  $L_0 - L_3$  and  $R_0 - R_3$  face very little resistance prior to reaching amplifiers 47-50.

### Claims

1. An integrated circuit random access memory (10) for providing a predetermined number of data bits as an output ( $Q_0-Q_7$ ) in a read mode and for receiving the predetermined number of data bits in a write mode, comprising:
  - a left array (17) comprised of a first plurality of adjacent left subarrays (21, 22) on a left side of the memory; and
  - a right array (18) comprised of a second plurality of adjacent right subarrays (24, 25) on a right side of the memory;
 characterized by further comprising:
  - a first amplifier (13), coupled to the left array, for providing as a first portion of the output of the memory (10) a first half of the predetermined number of data bits received from a selected one of the adjacent left subarrays (21, 22); and
  - a second amplifier (14) coupled to the right array, for providing as a second portion of



signal  $L_3$ , transistors 60 and 61 with signal  $R_0$ , transistors 62 and 63 with signal  $R_1$ , transistors 64 and 65 with signal  $R_2$ , transistors 66 and 67 with signal  $R_3$ . Each amplifier 47-50 is coupled to a pair of transistors of both couplers 46 and 51 by a pair of conductors 69, 70, 71 and 72, respectively. Conductor pair 69 connects transistor pair 52-53 and transistor pair 60-61 to  $Q_0$  amplifier 47. Conductor pair 70 connects transistor pair 54-55 and transistor pair 62-63 to  $Q_1$  amplifier 48. Conductor pair 71 connects transistor pair 56-57 and transistor pair 64-65 to  $Q_2$  amplifier 49. Conductor pair 72 connects transistor pair 58-59 and transistor pair 66-67 to  $Q_3$  amplifier 50. Each signal  $L_0 - L_3$  and  $R_0 - R_3$  has a true and complementary representation. When a logic high is received on the gates of the transistors of a transistor pair, that transistor pair couples the true and complementary representation of the signal, one of  $L_0 - L_3$  and  $R_0 - R_3$ , with which it is associated to the conductor pair, one of 69-72, to which it is connected. Accordingly, when signal  $A_p$  is a logic high, transistor pair 52-53 couples signal  $L_0$  to  $Q_0$  amplifier 47 via conductor pair 69, transistor pair 54-55 couples signal  $L_1$  to  $Q_1$  amplifier 48 via conductor pair 70, transistor pair 56-57 couples signal  $L_2$  to  $Q_2$  amplifier 49 via conductor pair 71, and transistor pair 58-59 couples signal  $L_3$  to  $Q_3$  amplifier 50 via conductor pair 72. With signal  $A_p$  at a logic high, signal  $\bar{A}_p$  is a logic low which turns off transistors 60-67 to prevent interference with signals  $L_0 - L_3$  which are carried on conductors 69-72. In the same way when signal  $A_p$  is a logic low and  $\bar{A}_p$  is a logic high, transistor pairs 60-61, 62-63, 64-65, and 66-67 couple signals  $R_0 - R_3$ , respectively, to amplifiers 47-50, respectively, and transistors 52-59 are turned off. Amplifiers 47-50 sense and amplify the logic state of the received signal to provide output bits  $Q_0 - Q_3$ .

Each signal  $L_0 - L_3$  and  $R_0 - R_3$  is representative of a logic state of a memory cell such as memory cell 36 of FIG. 2. Memory portion 21 is comprised of memory planes 69, 70, 71, and 72 each of which has a plurality of memory cells located at intersecting rows and columns. Likewise, portion 22 is comprised of memory planes 73, 74, 75, and 76 each of which has memory cells located at intersecting rows and columns. Planes 69-76 provide signal  $L_0 - L_3$  and  $R_0 - R_3$ , respectively. When signal  $A_p$  is a logic high, planes 69-72 are precharged. A cell from each plane 69-72 is then selected. Signals  $L_0 - L_3$  are provided as representative of the logic state of the selected memory cells. With signal  $A_p$  at a logic high, signals  $L_0 - L_3$  are coupled to amplifier 47-50 which in turn provide output bits  $Q_0 - Q_3$  at the logic state indicated by signal  $L_0 - L_3$ . When signal  $A_p$  is a logic low and  $\bar{A}_p$  is a logic high, planes 73-76 are precharged. A cell from each plane 73-76 is selected. Signals  $R_0 - R_3$

are provided as representative of the logic state of the selected memory cells. With signal  $\bar{A}_p$  at a logic high, signals  $R_0 - R_3$  are coupled to amplifiers 47-50 which in turn provide output bits  $Q_0 - Q_3$  at the logic state indicated by signals  $R_0 - R_3$ . Thus it is shown that only four amplifiers, amplifiers 47-50, are needed for the left half 17 of the array 12. The same structure as shown in FIG. 3 for left half 17 is also provided for right half 18. As is shown in FIG. 1 and 3 there is no required decoding between amplifiers 47-50 and pads 28-31. With the same structure for amplifier-driver 14 as is shown for amplifier-driver 13 shown in FIG. 3, there is also no required decoding between amplifier-driver 14 and pads 32-35. Also the conductive paths between amplifier-drivers 13-14 and pads 28-35 do not cross each other. Accordingly, the conductive paths between amplifier-drivers 13-14 and pads 28-35 are uninterrupted. Consequently, the highest conductivity interconnect, for example, metal, is used.

FIG. 3 further shows that conductor pairs 69-72 are uninterrupted between couplers 46 and 51. Conductor pairs 69-72 can thus be made from the highest conductivity material, for example metal, available for making interconnect for memory circuit 10. Connections between transistors 52-59 and conductors 69-72 can be made by conventional metal to diffusion contacts. Transistor diffusion can be made to extend under conductors 69-72 by conventional fabrication techniques. Diffusions are also relatively low resistance so that outputs of memory cells which provide signals  $L_0 - L_3$  and  $R_0 - R_3$  face very little resistance prior to reaching amplifiers 47-50.

### Claims

1. An integrated circuit random access memory (10) for providing a predetermined number of data bits as an output ( $Q_0-Q_7$ ) in a read mode and for receiving the predetermined number of data bits in a write mode, comprising:
  - a left array (17) comprised of a first plurality of adjacent left subarrays (21, 22) on a left side of the memory; and
  - a right array (18) comprised of a second plurality of adjacent right subarrays (24, 25) on a right side of the memory;
 characterized by further comprising:
  - a first amplifier (13), coupled to the left array, for providing as a first portion of the output of the memory (10) a first half of the predetermined number of data bits received from a selected one of the adjacent left subarrays (21, 22); and
  - a second amplifier (14) coupled to the right array, for providing as a second portion of



the output of the memory (10) a second half of the predetermined number of data bits received from a selected one of the adjacent right subarrays (24, 25);

the selected one of said left subarrays (21, 22) providing, in parallel, the first half of the predetermined number of said data bits; and

the selected one of said right subarrays (24, 25) providing, in a parallel, the second half of the predetermined number of said data bits and further characterized in that only the selected one of said left subarrays (21, 22) and the selected one of said right subarrays (24, 25) are precharged in response to an equalization pulse.

2. The integrated circuit (10) of claim 1 or 2 further comprising uninterrupted metal lines (69-72) connecting output pads (28-35), which receive the predetermined number of said data bits from the first and second amplifiers, to the first and second amplifiers.

#### Patentansprüche

1. Integrierter Speicherschaltkreis (10) mit wahlfreiem Zugriff zum Bereitstellen einer vorgegebenen Anzahl von Datenbits als Ausgabe (Q0-Q7) in einem Lesemodus und zum Empfangen einer vorgegebenen Anzahl von Datenbits in einem Schreibmodus mit:

einer linken Anordnung (17), die aus einer ersten Mehrzahl von benachbarten linken Unteranordnungen (21, 22) auf der linken Seite des Speichers besteht; und

einer rechten Anordnung (18), die aus einer ersten Mehrzahl von benachbarten rechten Unteranordnungen (24, 25) auf der rechten Seite des Speichers besteht;

dadurch gekennzeichnet, daß er außerdem umfaßt:

einen ersten Verstärker (13), der mit der linken Anordnung verbunden ist, um als ersten Teil der Ausgabe des Speichers (10) eine erste Hälfte der vorgegebenen Anzahl von Datenbits, die von einer ausgewählten der benachbarten linken Unteranordnungen (21, 22) erhalten werden, bereitzustellen; und

einen zweiten Verstärker (14), der mit der rechten Anordnung verbunden ist, um als zweiten Teil der Ausgabe des Speichers (10) eine zweite Hälfte der vorgegebenen Anzahl von Datenbits, die von einer ausgewählten der benachbarten rechten Unteranordnungen (24, 25) erhalten werden, bereitzustellen;

wobei die ausgewählte der linken Unteranordnungen (21, 22) parallel die erste Hälfte der vorgegebenen Anzahl der Datenbits bereitstellt;

und

wobei die ausgewählte der rechten Unteranordnungen (24, 25) parallel die zweite Hälfte der vorgegebenen Anzahl der Datenbits bereitstellt,

und außerdem dadurch gekennzeichnet, daß nur die ausgewählte der linken Unteranordnungen (21, 22) und die ausgewählte der rechten Unteranordnungen (24, 25) in Abhängigkeit von einem Ausgleichsimpuls vorgeladen werden.

2. Integrierter Schaltkreis (10) nach Anspruch 1, der außerdem nicht unterbrochene Metallleitungen (69-72) umfaßt, die die vorgegebene Anzahl der Datenbits von den ersten und zweiten Verstärkern erhalten, mit den ersten und zweiten Verstärkern verbinden.

#### Revendications

1. Une mémoire vive à circuit intégré (10) destinée à fournir un nombre prédéterminé de bits de données à titre d'information de sortie (Q0-Q7) dans un mode de lecture, et à recevoir le nombre prédéterminé de bits de données dans un mode d'écriture, comprenant :

un réseau gauche (17) constitué par un premier ensemble de sous-réseaux gauches adjacents (21, 22) d'un côté gauche de la mémoire; et

un réseau droit (18) constitué par un second ensemble de sous-réseaux droits adjacents (24, 25) d'un côté droit de la mémoire;

caractérisée en ce qu'elle comprend en outre: un premier amplificateur (13), connecté au réseau gauche, pour fournir à titre de première partie de l'information de sortie de la mémoire (10), une première moitié du nombre prédéterminé de bits de données qui sont reçus à partir d'un sous-réseau sélectionné parmi les sous-réseaux gauches adjacents (21, 22); et

un second amplificateur (14) connecté au réseau droit, pour fournir à titre de seconde partie de l'information de sortie de la mémoire (10), une seconde moitié du nombre prédéterminé de bits de données qui sont reçus à partir d'un sous-réseau sélectionné parmi les sous-réseaux droits adjacents (24, 25);

le sous-réseau sélectionné parmi les sous-réseaux gauches (21, 22) fournissant, en parallèle, la première moitié du nombre prédéterminé de bits de données; et

le sous-réseau sélectionné parmi les sous-réseaux droits (24, 25) fournissant, en parallèle, la seconde moitié du nombre prédéterminé de



bits de données, et

caractérisée en outre en ce que seuls le sous-réseau sélectionné parmi les sous-réseaux gauches (21, 22) et le sous-réseau sélectionné parmi les sous-réseaux droits (24, 25) sont préchargés sous l'effet d'une impulsion d'égalisation.

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2. Le circuit intégré (10) de la revendication 1, comprenant en outre des conducteurs métalliques ininterrompus (69-72) connectant aux premier et second amplificateurs des plots de sortie (28-35) qui reçoivent le nombre prédéterminé de bits de données à partir des premier et second amplificateurs.

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