Description

This invention relates to a raster scanning type ..splay system, and more particularly to a cathode ray tube graphic display system which facilitates the addressing of a refresh memory and also permits scrolling.

The graphic display system using a raster scanning type cathode ray tube (hereinafter referred to as CRT) normally uses a bit mapped refresh buffer memory which assigns a data bit to each display dot or picture element. Fig. 1 shows a prior art configuration of such graphic display systems. A refresh memory 50 stores video dot data which one to one correspond to dots of a graphic pattern such as characters and diagrams displayed on the CRT 80. The refresh memory 50 is addressed by a microprocessor (MPU) 10 or a CRT controller (CRTC) 20. The address from the CRTC 20 are selectively supplied to the refresh memory 50 through a multiplexer 40. The output of an oscillator (OSC) 30 is input to a clock circuit 32, and the clock circuit 32 outputs a clock signal CLK to the CRTC 20. The MPU 10 supplies addresses to the address bus for reading from and writing into the refresh memory 50 through a data bus. The CRTC 20 supplies display addresses to the refresh memory 50 during display operation to read the video dot data sequentially. The video dot data read by the CRTC 20 is serialized by a parallel/serial converter (P/S) 60, and then supplied to the CRT 80 through a video control circuit 70. The CRTC 20 provides a horizontal synchronizing signal (HS) and a vertical synchronizing signal (VS) to the video control circuit 70.

In such a graphic display, the number of dots displayed may vary depending on the size of the CRT. For example, a 15-inch CRT displays 1,024 dots in the X (horizontal) direction and 768 dots in the Y (vertical) direction and a 12-inch CRT displays 720 dots in the X direction and 512 dots in the Y direction. Therefore, in case of the 15-inch CRT, the refresh memory stores 1,024×768 bits of video dot data, and in case of the 12-inch CRT, the refresh memory stores 720×512 bits of video dot data.

When a 16-bit microprocessor is used as the MPU 10, it is advantageous to divide the storage area of the refresh memory 50 into memory blocks of 1×16 bits and to address on block by block basis. In case of the 15-inch CRT, since each horizontal scanning line of 1,024 dots is divided into 64 line segments or display information units each containing 16 dots, 64 memory blocks must be read from the refresh memory in each horizontal scanning line. In case of the 12-inch CRT, each horizontal line of 720 dots is divided into 45 line segments each containing 16 dots, and therefore, 45 memory blocks must be read from the refresh memory in each horizontal scanning line.

Such a graphic display, however, involves the problem that when sequential addresses are assigned to the memory blocks, the address calculation is very complicated unless the number of line segments per scanning line or the number of memory blocks to be read for each scanning line is represented by a power of 2. This problem will be described referring to Figs. 2 and 3.

Figs. 2 and 3 show refresh memories for a 15-inch CRT and a 12-inch CRT, respectively. The storage area of each refresh memory is divided into memory blocks of 1×16 bits, and is addressed on block by block basis. The memory blocks are assigned to sequential addresses as shown by 0, 1, . . ., and read sequentially in the order of the addresses by the CRTC during display operation.

Suppose the case where memory blocks A, B, C and D are addressed from the microprocessor to set the specified bits of the memory blocks A, B, C and D to 1 as shown by reference number 90. In this case, it is necessary to access the memory blocks A, B, C and D sequentially for writing the data. Since the addresses of memory blocks are sequential, the address of the memory block B is given by the address of the memory block A plus the number of memory blocks per scanning line, and so forth.

In case of Fig. 2, the number of line segments or the number of memory blocks per scanning line, is $64=2^6$, the sixth power of 2.

Therefore, the addresses of the memory blocks B, C and D can be obtained easily by adding a binary number 1000000 to the addresses of the memory blocks A, B and C, respectively. The address of any selected memory block can also be obtained easily. For example, if the memory block A is in Xth in Yth memory block row, the binary address of the storage block A can be obtained by $Y \cdot 2^6+X$ easily.

In case of Fig. 3, on the other hand, the number of memory blocks is 45 (101101 in binary), and is not represented by any power of 2. To obtain the addresses of memory blocks B, C and D, the binary number 101101 must be added to the addresses of memory blocks A, B and C, respectively, making the address calculation complicated. Of course, a complicated calculation is also required to obtain the binary address of any selected memory block. Since the method of address calculation for a 15-inch CRT differs from that of a 12-inch CRT, separate programs must be prepared depending on the size of CRTs.

Furthermore, when a refresh memory of a bit capacity corresponding to the number of display dots of a CRT screen is used as in Figs. 2 and 3, scrolling cannot be accomplished unless the data of the refresh memory is rewritten. Since rewriting increases the burden of the program, it is desirable that scrolling is accomplished easily with hardware.

The invention as claimed is intended to remedy these drawbacks. It solves the problem of how to provide a technique for facilitating the addressing of memory blocks of a refresh memory in a graphic display in which the number of line segments per scanning line is not represented by any power of 2.

Another object of this invention is to facilitate the addressing of memory blocks of a refresh

memory in a graphic display in which the number of line segments per scanning line is not represented by any power of 2, and to accomplish scrolling.

According to this invention, letting M (M is an integer larger than 1, not represented by any power of 2) be the number of line segments per scanning line, a refresh memory having N memory blocks per scanning line (N is an integer larger than M, represented by a predetermined power of 2) is used, and M memory blocks are accessed during the display time and (N—M) memory blocks are accessed during the non-display time. The memory blocks are assigned to sequential addresses. According to this invention, scrolling can also be accomplished by changing the display start address of the refresh memory.

One way of carrying out the invention is described in detail below with reference to the drawings 4 to 7 which illustrate only a preferred embodiment, in which:

Fig. 4 is a memory configuration of a refresh memory in accordance with the invention;

Fig. 5 is a block diagram of a graphic display system in accordance with the invention;

Fig. 6 is the timing control circuit used in the graphic display system in accordance with the invention;

Fig. 7 illustrates the operational waveforms of the timing control circuit of Fig. 6.

The memory configuration of the refresh memory (Fig. 4) is designed for use with a 12-inch CRT which displays 720×512 dots. The storage area of the refresh memory 100 is divided into memory blocks of 1×16 bits, and each memory block is assigned a sequential address. In this embodiment, the number of line segments or memory blocks actually used for display in each scanning line period, M, is 45 not being any power of 2, and the number of memory blocks per scanning line, N, is 64 being the sixth power of 2. When the start address is 0, therefore, the area 110 is displayed on the CRT screen.

The CRT controller (CRTC) accesses M memory blocks during the display time in each horizontal scanning line period, and (N—M) memory blocks during the non-display time. This permits the use of the same addressing as described in connection with Fig. 2 even when the number of line segments in each scanning line is not any power of 2. The refresh memory configuration in Fig. 4 is also suitable for a 15-inch CRT without changing the program if 64×768 memory blocks are used. In Fig. 4, 64 memory blocks are shown in the X direction, and 1,024 memory blocks, in the Y direction, but the number of memory blocks in the Y direction is not necessarily a power of 2 and has only to be equal to or greater than the number of horizontal scanning lines.

The major difference between Fig. 1 and the graphic display system in accordance with the invention as shown in Fig. 5 is the use of a refresh memory 130 having a configuration as shown in Fig. 4 and a timing control circuit 120 which switches the frequency of the basic clock CLK to the CRTC 20 another system using a change of clock frequency, at the end of a frame, is disclosed by document number US—A—3916402.

The microprocessor (MPU) 10 is, for example, Intel iAPX-86, and the CRTC 20 is, for example, Hitachi HD46505SP-2. The CRTC 20 can be initialized by the MPU 10 for various operational conditions for making display on the CRT 80, such as horizontal period, the number of horizontal scanning lines, the number of memory blocks to be accessed for each scanning line. In the configuration of Fig. 4, the number of memory blocks accessed for each scanning line is set to 64.

In this case, however, there arises a problem that timing error occurs between the horizontal period of the CRT 80 and the refresh memory access time for each scanning line. That is, under the operational condition suitable for displaying 720×512 dots on the 12-inch CRT 80, the horizontal period T_H is, for example, 45.6 µs. On the other hand, since it takes 800 ns for accessing a memory block for each line segment and displaying it, the access time of 45 memory blocks to be actually displayed is

$$800\ \text{ns} \times 45 = 36\ \mu\text{s},$$

and the remaining time,

$$45.6 - 36 = 9.6\ \mu\text{s},$$

is insufficient for accessing the remaining 19 memory blocks. In other words, letting T_D and T_B be the display time and the non-display time of each horizontal period, respectively,

$$[T_D/M] > [T_B/(N-M)],$$

and if the refresh memory access rate of the CRTC 20 is fixed, 64 memory blocks cannot be accessed in each horizontal scanning line.

According to this invention, the frequency of the basic clock CLK to the CRTC 20 is switched between the display time T_D and the non-display time T_B by means of the timing control circuit 120. In this example, the clock CLK to the CRTC 20 runs at a period of 800 ns (frequency: 1.25 MHz) during the time T_D and at a period of 400 ns (frequency: 2.5 MHz) during the time T_B. Since the CRTC 20 accesses a memory block in one cycle of the clock signal CLK, the memory blocks are accessed on the non-display time at a rate twice that in the display time. In the non-display time T_B, therefore, 19 memory blocks are accessed in

$$400\ \text{ns} \times 19 = 7.6\ \mu\text{s}.$$

Consequently, the CRTC 20 accesses 64 memory blocks in

$$36\ \mu\text{s} + 7.6\ \mu\text{s} = 43.6\ \mu\text{s}$$

in each horizontal scanning. The CRTC 20 judges the number of the accessed memory blocks by the number of clock pulses CLK. The remaining time,

45.6 μs−43.6 μs=2 μs,

used for synchronization.

Fig. 6 shows the timing control circuit 120, and Fig. 7 shows the operational waveforms thereof. An oscillator (OSC) 30 generates a 20 MHz signal which is converted to clock signals of 400 ns and 800 ns periods by frequency dividers 140 and 150, respectively. The 800 ns clock is shown as waveform A in Fig. 7, and the 400 ns clock, as waveform B. The number of 800 ns clock pulses required for accessing 45 memory blocks during the display time T_D, 45, is preset in a register 160, and this value is loaded into the counter 170 by a load pulse from a load pulse generator 180 prior to each display time T_D. The load pulse generator 180 receives the horizontal synchronizing signal HS (waveform C) from the CRTC 20 and the 400 ns clock, and as shown in waveform D, generates a low level of 800 ns duration, 800 ns after the fall of the horizontal synchronizing signal HS, providing the load pulses. T_H in waveform C shows the length of a horizontal period.

The count value loaded into the counter 170 is counted down by the 800 ns clock. The counter 170 generates a high level when the count value is loaded, and generates a low level when the count value is counted down to 0 (waveform E). The counter output is applied to an AND circuit A1 through an inverter circuit I1, and also applied to an AND circuit A2. The AND circuits A1 and A2 receive the 400 ns and 800 ns clocks as another input, respectively. Therefore, the 800 ns clock is gated to the CRTC 20 through an OR circuit when the counter output is high, and the 400 ns clock is gated to the CRTC 20 when the counter output is low. Thus, the clock signal CLK as in waveform F is applied to the CRTC 20.

Consequently, 45 memory blocks to be displayed in each scanning line are read by the 800 ns clock, and the remaining 19 memory blocks are read by the 400 ns clock. The output of the counter 170 is inverted by an inverter I2, and supplied to the video control circuit as a blanking signal (waveform G). Therefore, during the time T_D (36 μs) when 45 memory blocks are read, display is permitted, and during the remaining time T_B (9.6 μs), display is inhibited.

The CRTC 20 has a display start address register DSAR (Fig. 5) in which the addresses of a memory block to be first accessed in the first horizontal scan are set from the MPU 10. The CRTC 20 addresses sequentially the memory blocks starting with the address in the register DSAR. In this example, the CRTC 20 addresses 64×512 memory blocks sequentially. With the refresh memory of 64×1,024 memory blocks with 45×512 memory blocks thereof displayed as shown in Fig. 4, redundant memory spaces are available in both X and Y directions, and therefore, scrolling can easily be accomplished in both X and Y directions by changing the start address of the register DSAR. Since 64 memory blocks in the X direction can be addressed by 6 bits and 1,024 lines in the Y direction, by 10 bits, any memory block can be addressed by 16 bits with 6 bits for X placed at lower order part and 10 bits for Y placed at higher order part. When the start address bits are all 0, the area 110 in Fig. 4 is displayed; when higher 10 bits are all 0 and lower bits are changed, the display is scrolled in the X direction; when lower 6 bits are all 0 and higher bits are changed, the display is scrolled in the Y direction; and when both higher and lower bits are changed, the display is scrolled diagonally.

Claims

1. A graphic display system comprising:

a raster scanning cathode ray tube (80);

a refresh buffer memory (50) storing video dot data;

a CRT controller (20) selectively supplying display addresses to said refresh buffer memory (50) through a multiplexer (40), and providing a horizontal synchronizing signal (HS) as well as a vertical synchronizing signal (VS) to a video control circuit (70) also receiving video dot data read by said CRT controller (20);

a microprocessor (10) supplying addresses via an address but to said multiplexer (40) for reading data from, and writing data into said refresh memory buffer (50) via a data bus; and

timing control means (32) connected to said CRT controller (20) characterized in that

said raster scanning display device displays M line segments for each scanning line, where M is an integer greater than 1, not represented by any power of 2;

said refresh memory (130) has N memory blocks for each scanning line of said display device, where N is an integer greater than M, represented by a predetermined power of 2, said memory blocks being assigned to sequential addresses and each storing video data for one of said line segments;

said CRT controller (20) accesses M memory blocks during the display time of each scanning line period and (N—M) memory blocks during the remaining time of each scanning line period, and

said timing control means (120) includes counter means (170) for detecting the completion of accessing M memory blocks during each scanning line period and being responsive to said detection to inhibit displaying of said display device while (N—M) memory blocks are accessed.

2. A graphic display system of Claim 1, characterized by:

$$[T_D/M]>[T_B/(N—M)]$$

where T_D is the display time and T_B is the remaining time of each scanning line period, and

where said timing control means (120) increases the clock frequency to said CRT controller (20) in response to said counter means (170) so that accessing of (N—M) memory blocks is completed during the time T_B.

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a microprocessor (10) supplying addresses via an address but to said multiplexer (40) for reading data from, and writing data into said refresh memory buffer (50) via a data bus; and

timing control means (32) connected to said CRT controller (20) characterized in that

said raster scanning display device displays M line segments for each scanning line, where M is an integer greater than 1, not represented by any power of 2;

said refresh memory (130) has N memory blocks for each scanning line of said display device, where N is an integer greater than M, represented by a predetermined power of 2, said memory blocks being assigned to sequential addresses and each storing video data for one of said line segments;

said CRT controller (20) accesses M memory blocks during the display time of each scanning line period and (N—M) memory blocks during the remaining time of each scanning line period, and

said timing control means (120) includes counter means (170) for detecting the completion of accessing M memory blocks during each scanning line period and being responsive to said detection to inhibit displaying of said display device while (N—M) memory blocks are accessed.

2. A graphic display system of Claim 1, characterized by:

$$[T_D/M]>[T_B/(N—M)]$$

where T_D is the display time and T_B is the remaining time of each scanning line period, and

where said timing control means (120) increases the clock frequency to said CRT controller (20) in response to said counter means (170) so that accessing of (N—M) memory blocks is completed during the time T_B.

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Patentansprüche

1. Graphisches Anzeigesystem, folgendes enthaltend:

eine zeilenweise arbeitende Kathodenstrahlröhre (80);

einen Wiederauffrischungs-Pufferspeicher (50) zum Speichern von Bildpunktdaten;

eine Kathodenstrahlröhren-Steuereinheit (20), welche selektiv Anzeigeadressen an den Wiederauffrischungs-Pufferspeicher (50) durch einen Multiplexor (40) sendet und ein horizontales Synchronisiersignal (HS) sowie ein vertikales Synchronisiersignal (VS) an eine Bildsteuerschaltung (70) sendet, welche ebenfalls Bildpunktdaten empfängt, die von der Kathodenstrahlröhren-Steuereinheit (20) gelesen wurden;

einen Mikroprozessor (10), welche Adressen über einen Adressenbus an den Multiplexor (40) liefert, um über einen Datenbus Daten aus dem Wiederauffrischungs-Pufferspeicher zu lesen und in denselben zu schreiben; und

mit der Kathodenstrahlröhren-Steuereinheit (20) verbundene Zeitsteuermittel (32), dadurch gekennzeichnet, daß

die zeilenweise arbeitende Anzeigevorrichtung M Zeilensegmente für jede Abtastzeile anzeigt, wobei M eine ganze Zahl größer als 1 ist, die durch keine Zweierpotenz wiedergegeben wird;

der Wiederauffrischungsspeicher (130) N Speicherblöcke für jede Abtastzeile der Anzeigevorrichtung hat, wo N eine ganze Zahl größer als M ist, die durch eine bestimmte Zweierpotenz widergegeben wird, wobei die Speicherblöcke sequentiellen Adressen zugeordnet sind und jeweils Bilddaten für eines der Zeilensegmente speichern;

die Kathodenstrahlröhren-Steuereinheit (20) auf M Speicherblöcke während der Anzeigezeit jeder Abtastzeilenperiode und auf (N—M) Speicherblöcke während der verbleibenden Zeit jeder Abtastzeilenperiode zugreift, und

die Zeitsteuermittel (120) einen Zähler (170) enthalten, welcher das Ende des Zugriffs auf M Speicherblöcke während jeder Abtastzeilenperiode feststellt und nach dieser Feststellung das Anzeigen dieser Anzeigevorrichtung verhindert, während auf (N—M) Speicherblöcke Zugriff genommen wird.

2. Anzeigesystem nach Anspruch 1, gekennzeichnet durch:

$$[T_D/M]>[T_B/(N—M)]$$

wo T_D die Anzeigezeit und T_B die verbleibende Zeit jeder Abtastzeilenperiode ist, und

wo die Zeitsteuermittel (120) die Taktfrequenz zur Kathodenstrahlröhren-Steuereinheit (20) erhöhen als Antwort auf den Zähler (170), sodaß der Zugriff zu (N—M) Speicherblöcken während der Zeit T_B abgeschlossen wird.

Revendications

1. Dispositif d'affichage graphique comprenant:

un tube à rayons cathodiques à balayage de trame (80);

une mémoire tampon à rafraîchissement (50) mémorisant des points de données vidéo;

un contrôleur de TRC (20) fournissant sélectivement des adresses d'affichage à la mémoire tampon à rafraîchissement (50) par l'intermédiaire d'un multiplexeur (40), et fournissant un signal de synchronisation horizontale (HS) ainsi qu'un signal de synchronisation verticale (VS) à un circuit de commande vidéo (70) recevant aussi des points de données vidéo lus par le contrôleur de TRC (20);

un microprocesseur (10) fournissant des adresses par l'intermédiaire d'un bus d'adresse au multiplexeur (40) pour lire et écrire les données dans la mémoire tampon à rafraîchissement (50) par l'intermédiaire d'un bus de données; et

des moyens de commande de synchronisation (32) connectés au contrôleur de TRC (20) caractérisé en ce que

le dispositif d'affichage à balayage de trame affiche M segments de ligne pour chaque ligne de balayage, où M est un entier supérieur à 1, non représenté par une quelconque puissance de 2;

la mémoire à rafraîchissement (130) possède N blocs de mémoire pour chaque ligne de balayage du dispositif d'affichage, où N est un entier supérieur à M, représenté par une puissance de 2 prédéterminée, ces blocs de mémoire étant affectés à des adresses séquentielles et chacun mémorisant des données vidéo pour l'un des segments de ligne;

le contrôleur de TRC (20) accède à M blocs de mémoire pendant la durée d'affichage de chaque période de ligne de balayage et à (N—M) blocs de mémoire pendant la durée restante de chaque période de ligne de balayage, et

le moyen de commande de synchronisation (120) comprend un compteur (170) pour détecter la fin de l'accès aux M blocs de mémoire pendant chaque période de ligne de balayage et agir en réponse à cette détection pour empêcher un affichage de ce dispositif d'affichage pendant que l'on accède aux (N—M) blocs de mémoire.

2. Dispositif d'affichage graphique selon la revendication 1, caractérisé par:

$$[T_D/M]>[T_B/(N—M)]$$

où T_D est la durée d'affichage et T_B est la durée restante de chaque période de ligne de balayage, et

où le moyen de commande de synchronisation (120) augmente la fréquence d'horloge vers le contrôleur de TRC (20) en réponse au compteur (170) de sorte que l'accès (N—M) blocs de mémoire est achevé pendant la durée T_B.

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