WHAT IS CLAIMED IS:

1. An interface circuit of a memory device including a plurality of memory dies, comprising:

a plurality of registers corresponding to the plurality of memory dies, respectively, the plurality of registers each configured to store command information related to a data operation command;

a demultiplexer circuit configured to provide input command information to a selected register from among the plurality of registers according to at least one of a first address or a first chip selection signal, the input command information being received from outside the interface circuit; and

a multiplexer circuit configured to receive output command information from the selected register from among the plurality of registers and output the output command information according to at least one of a second address or a second chip selection signal,

wherein the interface circuit further comprises a way selection circuit configured to generate a demultiplexer control signal for controlling a first register selection of the demultiplexer circuit and a multiplexer control signal for controlling a second register selection of the multiplexer circuit, based on the at least one of the first address or the first chip selection signal.

2. The interface circuit of claim 1, wherein the way selection circuit is further configured to,

compare the first address with a lookup table stored therein,

select a memory die among the plurality of memory dies based on a result of the comparison, and

generate the demultiplexer control signal and the multiplexer control signal such that the demultiplexer circuit and the multiplexer circuit select a register corresponding to the selected memory die from among the plurality of registers.

3. The interface circuit of claim 1, wherein the way selection circuit is further configured to,

select a memory die corresponding to the first chip selection signal from among the plurality of memory dies, and

generate the demultiplexer control signal and the multiplexer control signal such that the demultiplexer circuit and the multiplexer circuit select one register, from among the plurality of registers, corresponding to the selected memory die.

4. The interface circuit of any one of claims 1 to 3, wherein

the plurality of memory dies include a first memory die and a second memory die,

the plurality of registers include a first register storing command information corresponding to the first memory die and a second register storing command information corresponding to the second memory die, and

the demultiplexer circuit is configured to provide the first register with first command information in response to input of a first data operation command for the first memory die, the first command information being related to the first data operation command.

5. The interface circuit of claim 4, wherein,

the interface circuit is configured to cause a first data operation on the first memory die to stop and resume according to the first data operation command in response to a second data operation on the second memory die, and

the multiplexer circuit is configured to select and output the first command information in response to input of at least one of an address or a chip selection signal, each indicating selection of the first memory die, the first command information being stored in the first register.

6. The interface circuit of claim 4 or claim 5, wherein the first command information includes at least one of the first data operation command or data operation control signals generated based on the first data operation command.

7. A method of operating a memory device including a first memory die and a second memory die, the method comprising:

performing a first data operation on the first memory die in response to a first input of a first command;

storing first command information related to the first command in a first register corresponding to the first memory die;

stopping the first data operation;

performing a second data operation on the second memory die in response to a second input of a second command; and

performing a remaining data operation on the first memory die based on the first command information stored in the first register, without receiving an additional resume command, the remaining data operation having not been performed during the first data operation,

wherein the memory device further includes an interface circuit including:

a plurality of registers, the plurality of registers each storing command information corresponding to a corresponding one of a plurality of memory dies, the plurality of memory dies including the first memory die and the second memory die;

a demultiplexer circuit configured to provide input command information to a selected register from among the plurality of registers according to at least one of a first address or a first chip selection signal, the input command information received from outside the memory device;

a multiplexer circuit configured to receive output command information from the selected register from among the plurality of registers and output the output command information according to at least one of a second address or a second chip selection signal; and

a way selection circuit configured to generate a demultiplexer control signal for controlling a first register selection of the demultiplexer circuit based on the at least one of the first address or the first chip selection signal, and generate a multiplexer control signal for controlling a second register selection of the multiplexer circuit based on the at least one of the second address or the second chip selection signal.

8. The method of claim 7, wherein the storing first command information includes storing the first command information in the first register corresponding to the first memory die from among the plurality of registers.

9. The method of claim 7 or claim 8, wherein the performing a remaining data operation includes performing the remaining data operation of the first data operation in response to a third input of at least one of an address or a chip selection signal, each indicating selection of the first memory die.

10. The method of any one of claims 7 to 9, wherein the first command information includes at least one of the first command or a first data operation control signal generated based on the first command.

11. The method of any one of claims 7 to 10, wherein

the storing first command information includes storing the first command, and

the performing a remaining data operation includes,

generating second data operation control signals based on the first command that has been stored, the second data operation control signals being related to the first command, and

performing the remaining data operation of the first data operation using the second data operation control signals.

12. The method of claim 10, wherein

the storing of the first command information includes,

generating the first data operation control signal based on the first command, and

storing the first data operation control signal, and

the performing a remaining data operation includes performing the remaining data operation of the first data operation using the first data operation control signal that have been stored.

13. A memory device comprising:

a plurality of memory dies including a first memory die and a second memory die;

an interface circuit configured to store plural pieces of command information, the plural pieces of command information corresponding to the plurality of memory dies, respectively, the interface circuit configured to selectively output at least one of the plural pieces of command information; and

a control logic configured to,

perform a first data operation according to a first selection signal and a first command,

stop the first data operation on the first memory die in response to an input

of a second selection signal and a second command for the second memory die during performing the first data operation,

control the memory device to perform a second data operation corresponding to the second command on the second memory die, and

control the memory device to perform a remaining data operation of the first data operation on the first memory die based on first piece of the plural pieces of command information in response to a re-input of the first selection signal, the first piece of the plural pieces of command information related to the first command received from the interface circuit.

14. The memory device of claim 13, wherein the interface circuit includes:

a plurality of registers storing the plural pieces of command information, respectively, the plural pieces of command information corresponding to the plurality of memory dies, respectively;

a demultiplexer circuit configured to provide input command information to a selected register from among the plurality of registers according to at least one of a first address or a first chip selection signal, the input command information received from outside the memory device; and

a multiplexer circuit configured to receive output command information from the selected register from among the plurality of registers and output the output command information according to at least one of a second address or a second chip selection signal.

15. The memory device of claim 14, wherein the interface circuit further includes a way selection circuit, the way selection circuit configured to,

generate a demultiplexer control signal for controlling a first register selection of the demultiplexer circuit based on the at least one of the first address or the first chip selection signal, and

generate a multiplexer control signal for controlling a second register selection of the multiplexer circuit based on the at least one of the second address or the second chip selection signal.

16. The memory device of any one of claims 13 to 15, wherein

the interface circuit is configured to store a plurality of data operation commands,

the plurality of data operation commands corresponding to the plurality of memory dies, respectively, and

the control logic is configured to,

generate data operation control signals based on the first command, and

control the memory device to perform the remaining data operation of the first data operation based on the data operation control signals.

17. The memory device of claim 16, wherein the control logic is further configured to,

select one command of the first command or a third command, a third command input from outside the memory device, and

generate the data operation control signals based on the selected one command.

18. The memory device of any one of claims 13 to 15, wherein

the interface circuit stores data operation control signals generated based on a data operation command corresponding to each of the plurality of memory dies, and

the control logic is configured to control the memory device to perform the remaining data operation of the first data operation on the first memory die based on first data operation control signals corresponding to the first command in response to completion of the second data operation.