

图 1

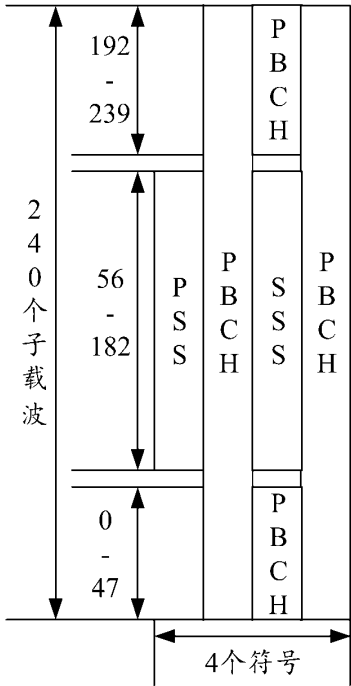


图 2

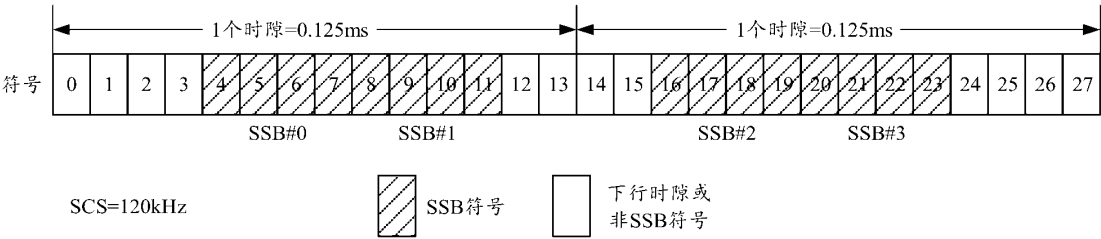


图 3

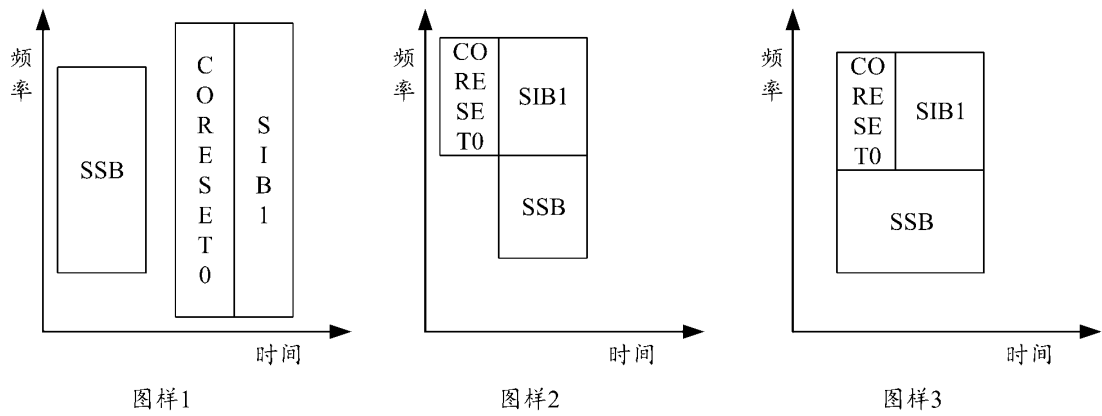


图 4

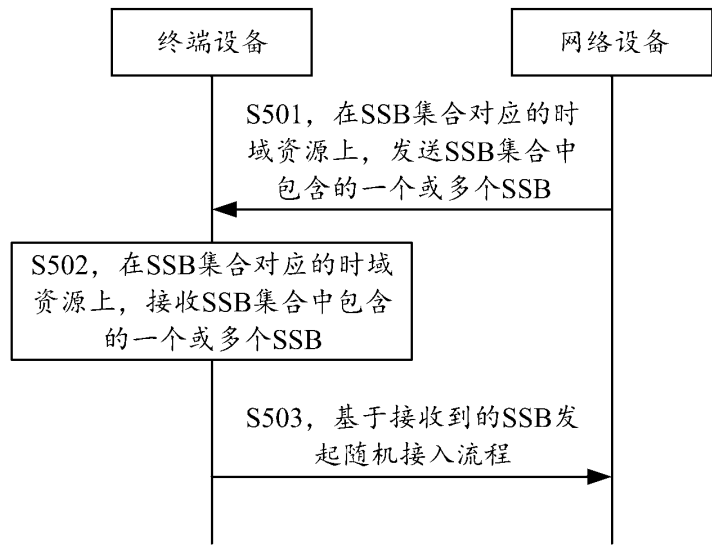


图 5

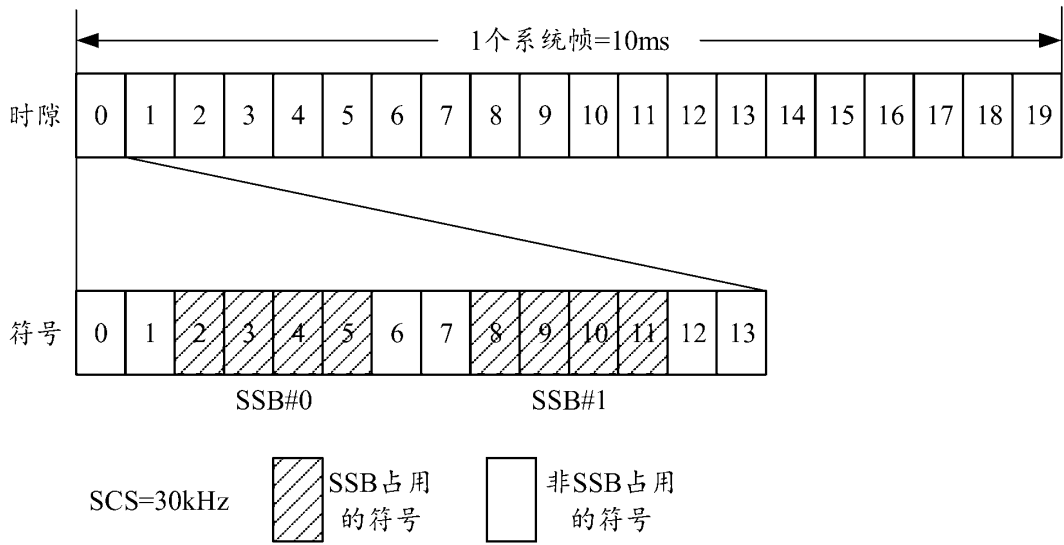


图 6

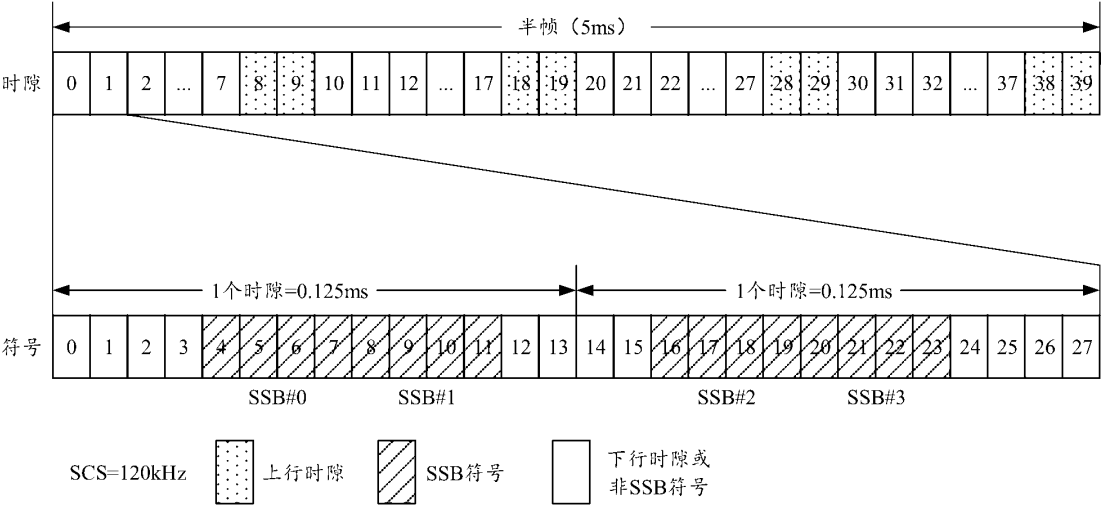


图 7

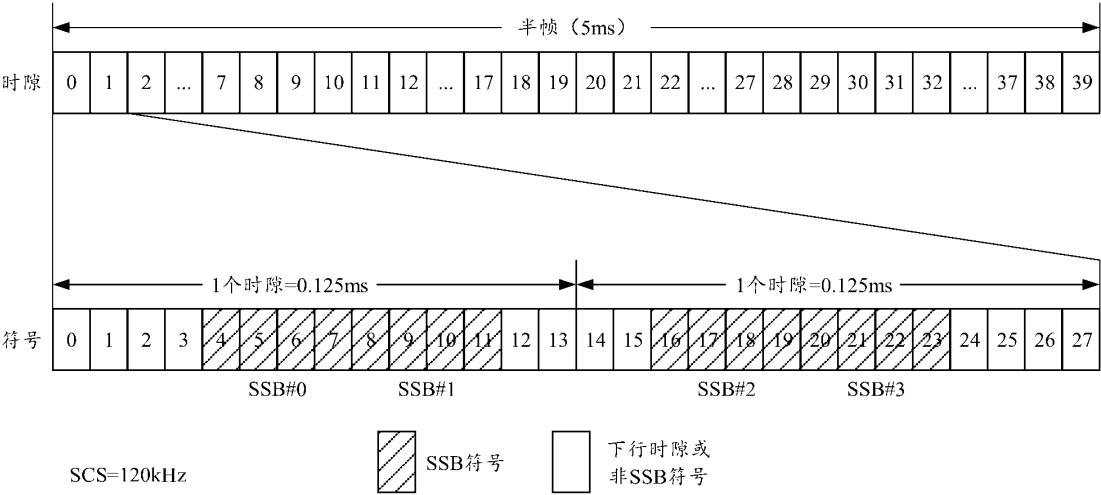


图 8

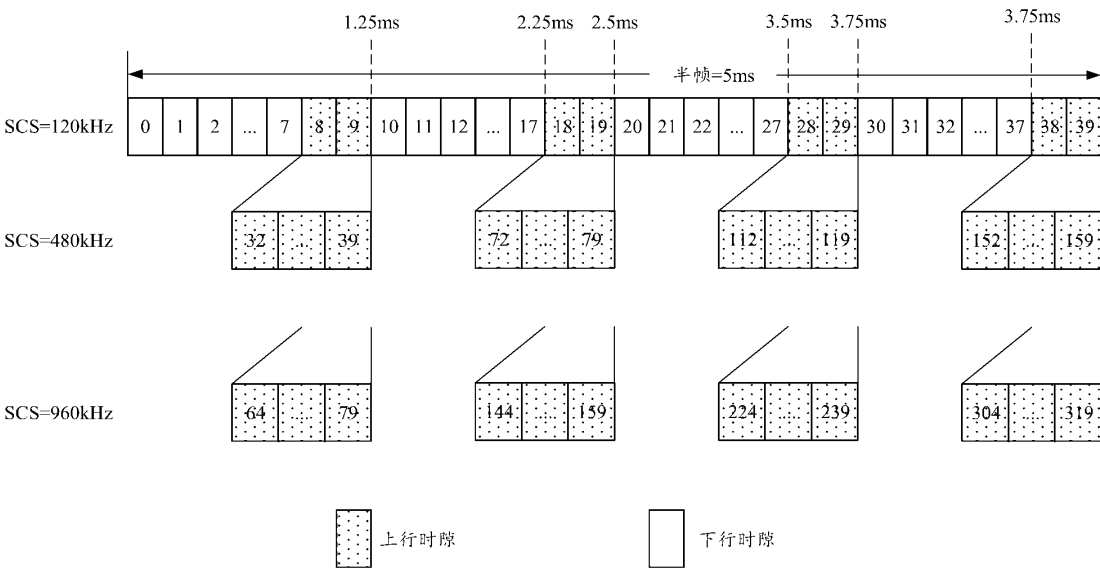


图 9

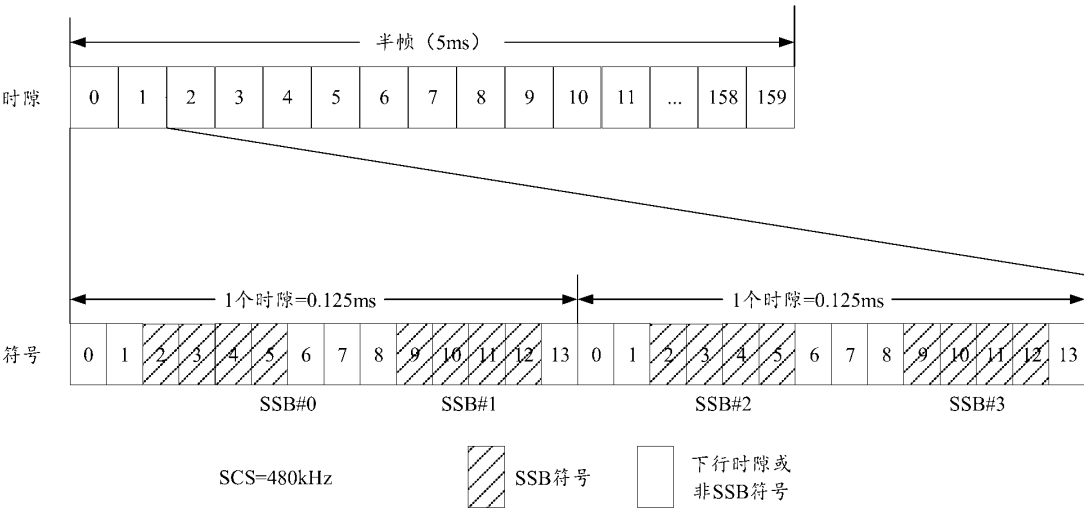
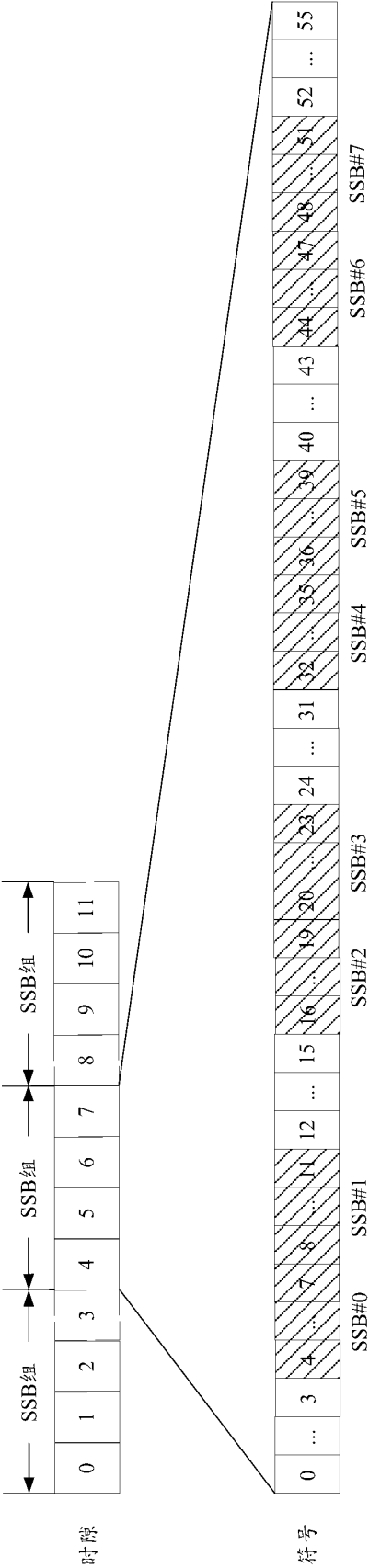


图 10



SCS=240kHz

图 11

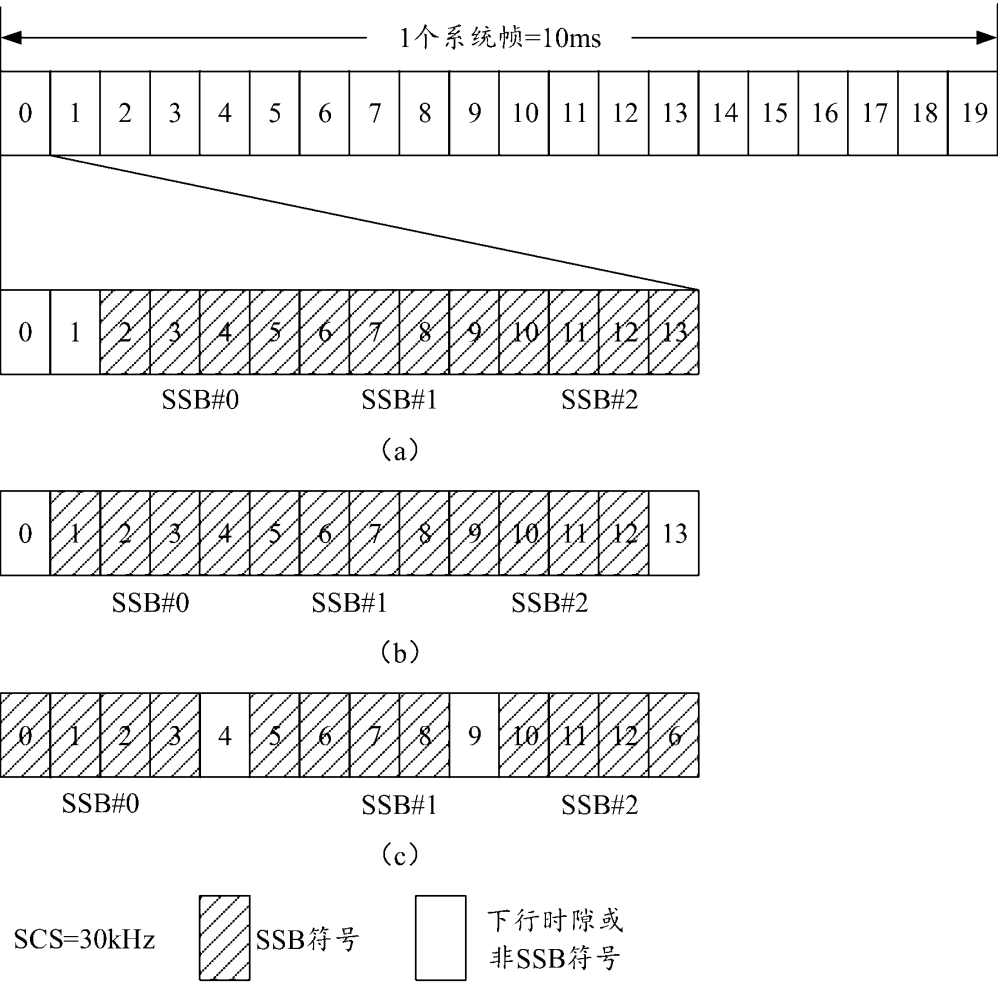


图 12

		SSB#0 对应的 CORE SET0		SSB#0 对应的 SIB1		SSB#1 对应的 CORE SET0		SSB#1 对应的 SIB1		SSB#2 对应的 CORE SET0		SSB#2 对应的 SIB1	
0	1	2	3	4	5	6	7	8	9	10	11	12	13
		SSB#0				SSB#1				SSB#2			

(a)

		SSB#0 对应的 CORE SET0		SSB#0 对应的 SIB1		SSB#1 对应的 CORE SET0		SSB#1 对应的 SIB1		SSB#2 对应的 CORE SET0		SSB#2 对应的 SIB1	
0	1	2	3	4	5	6	7	8	9	10	11	12	13
		SSB#0				SSB#1				SSB#2			

(b)

SSB#0 对应的 CORE SET0		SSB#0 对应的 SIB1			SSB#1 对应的 CORE SET0		SSB#1 对应的 SIB1			SSB#2 对应的 CORE SET0		SSB#2 对应的 SIB1	
0	1	2	3	4	5	6	7	8	9	10	11	12	6
SSB#0					SSB#1					SSB#2			

(c)

图 13

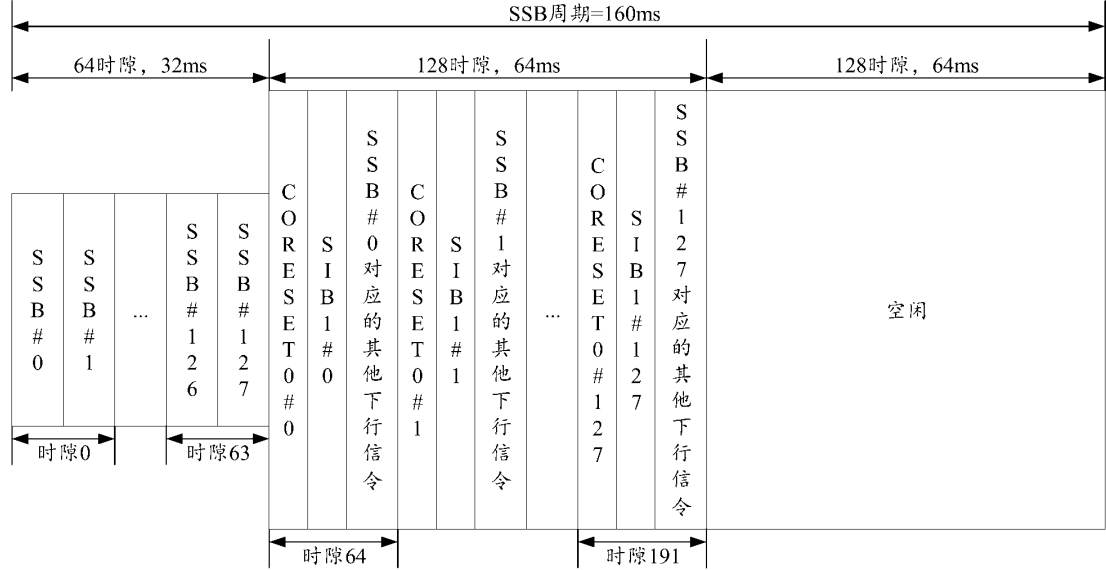


图 14

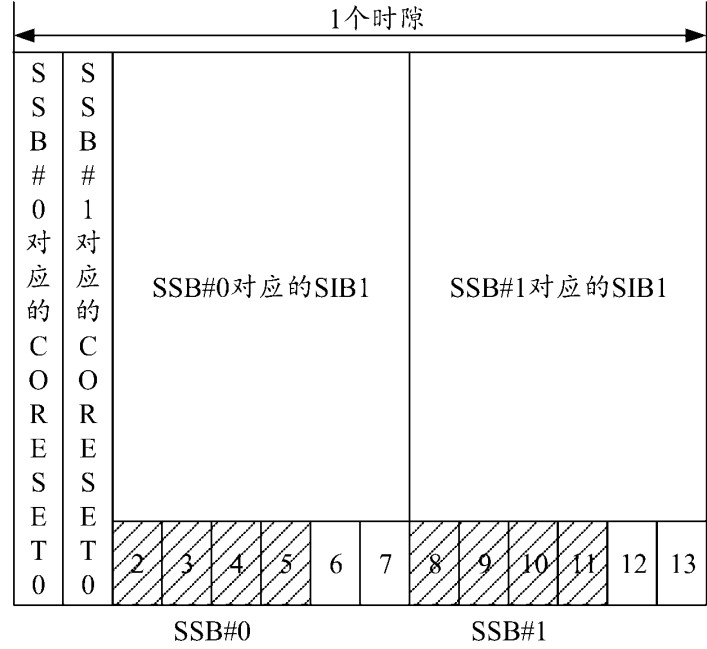


图 15

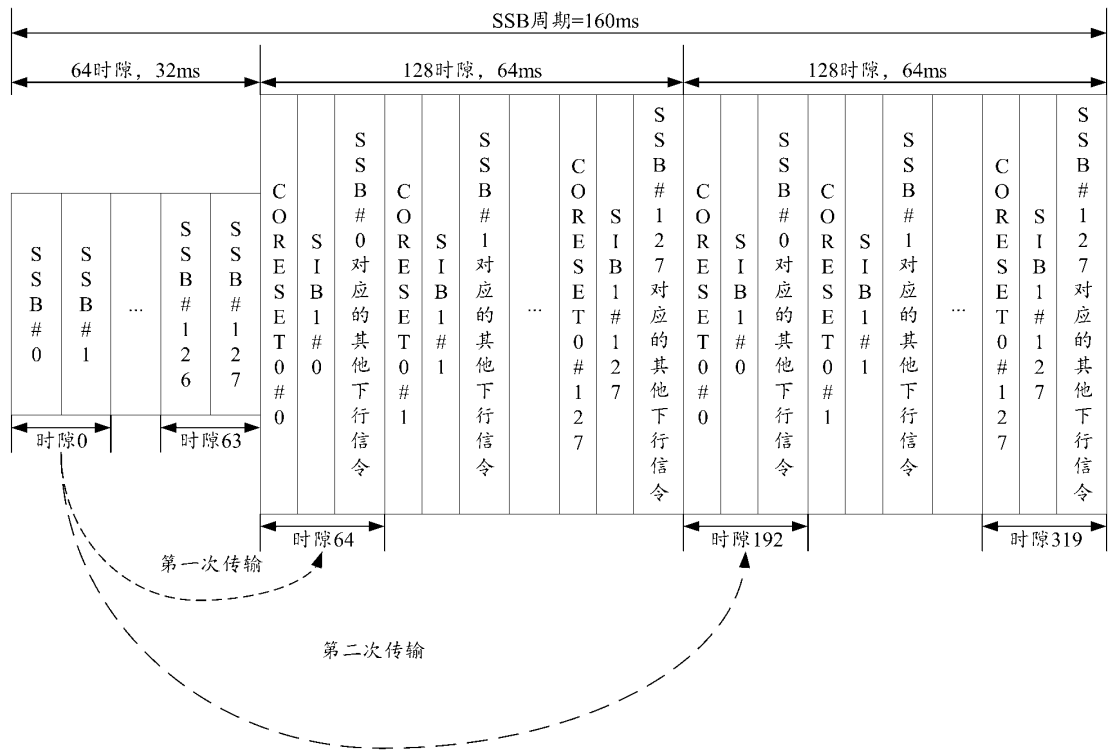


图 16

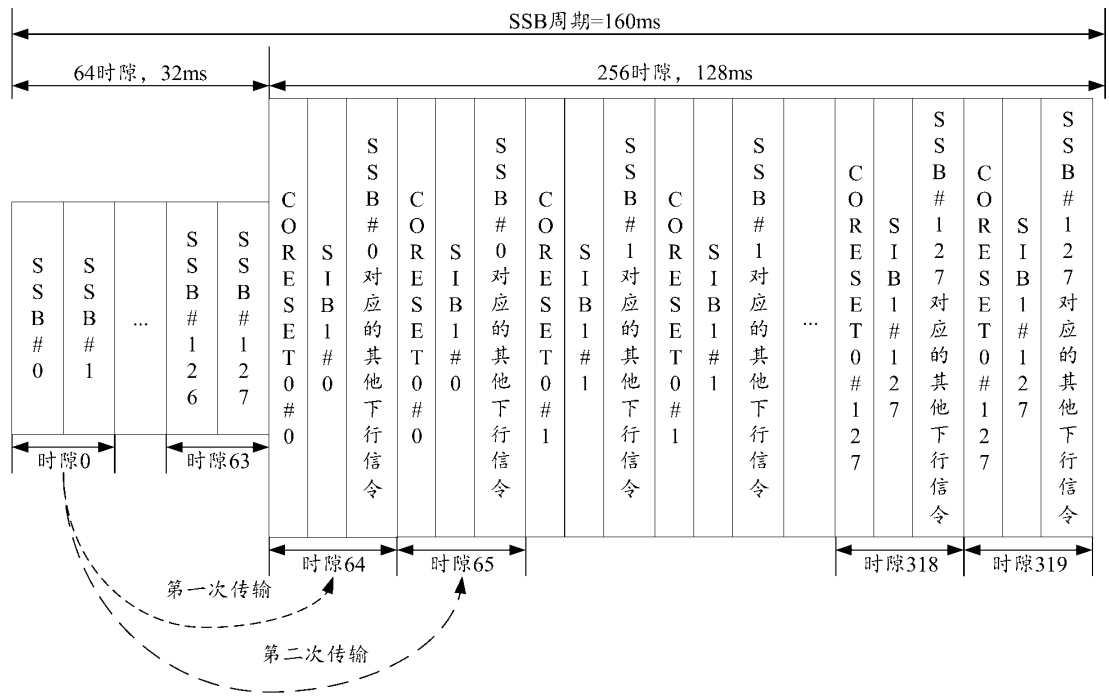
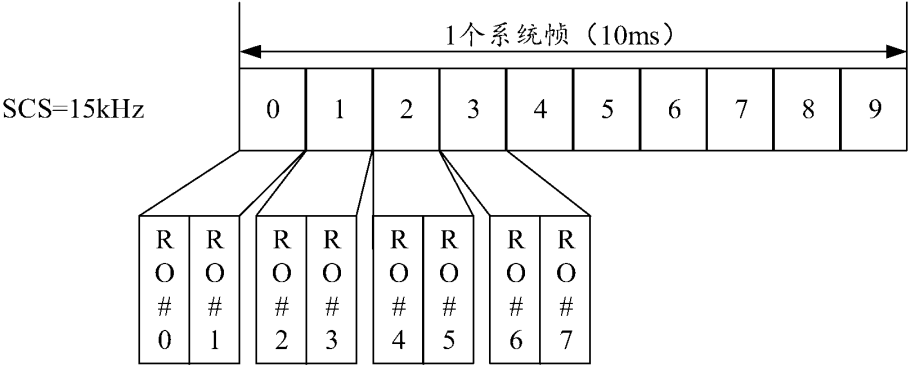
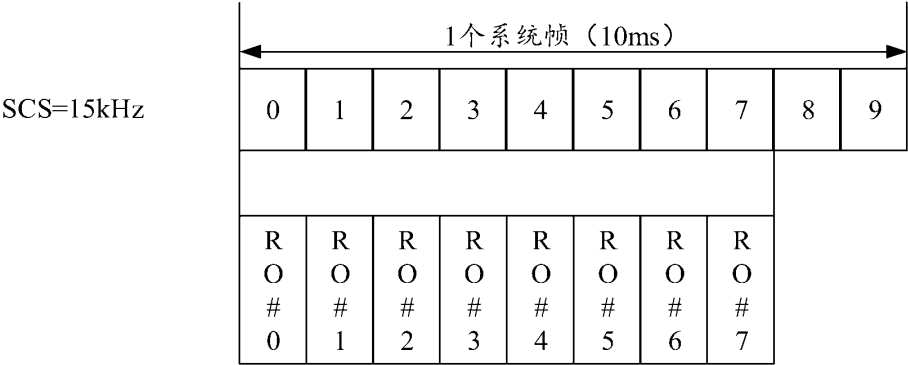


图 17



(a)



(b)

图 18

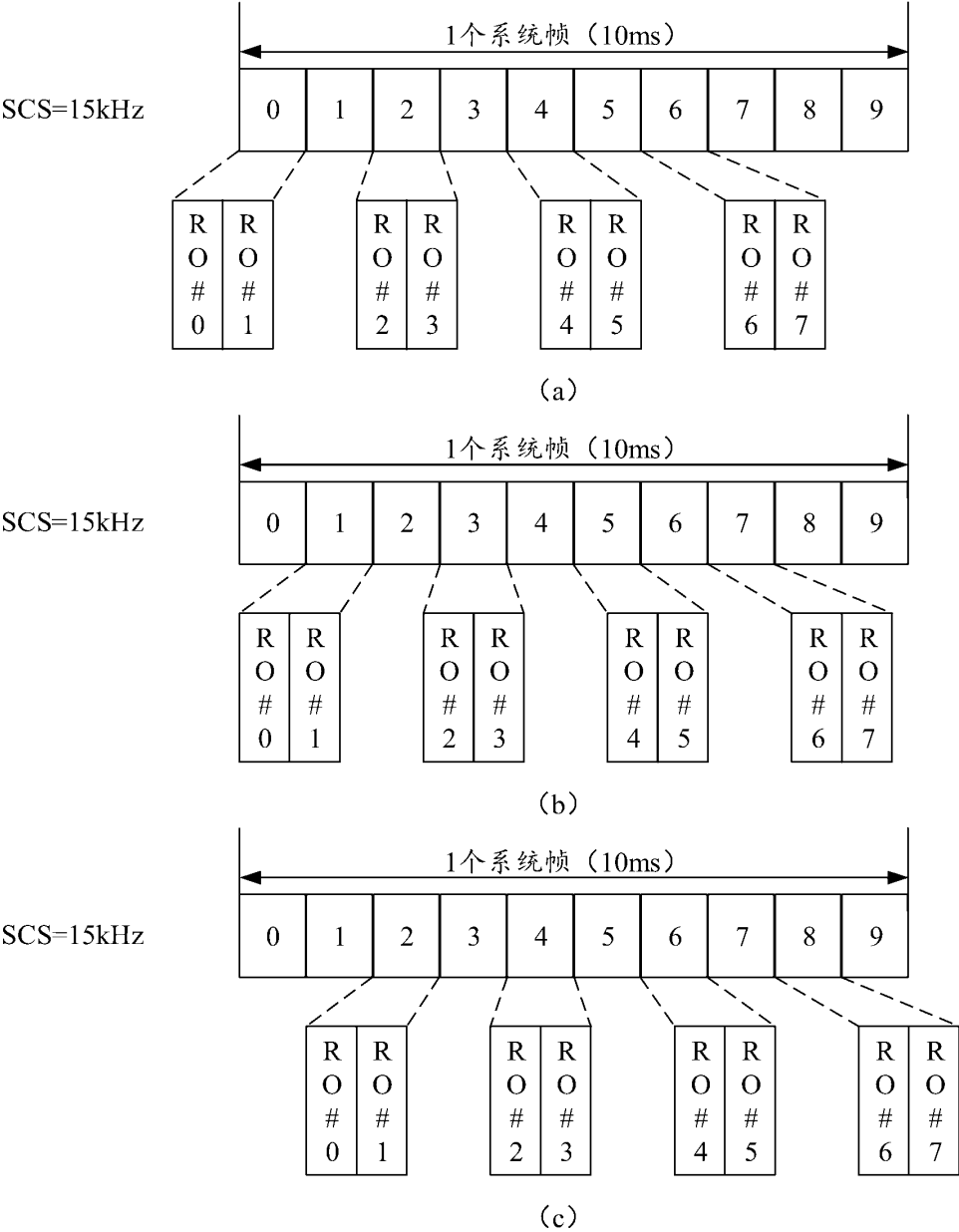


图 19



图 20

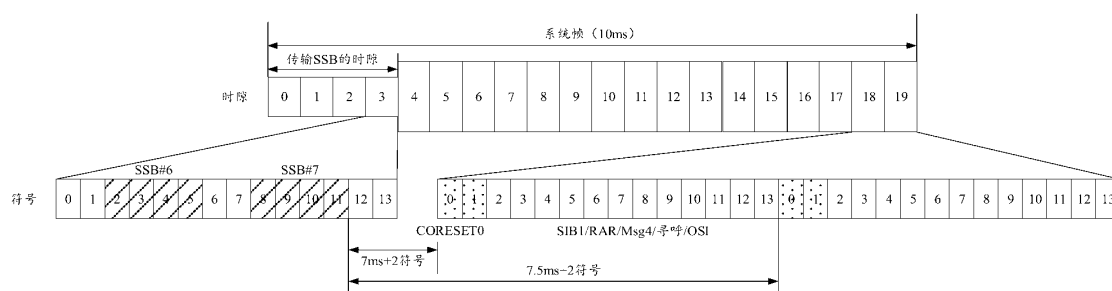


图 21

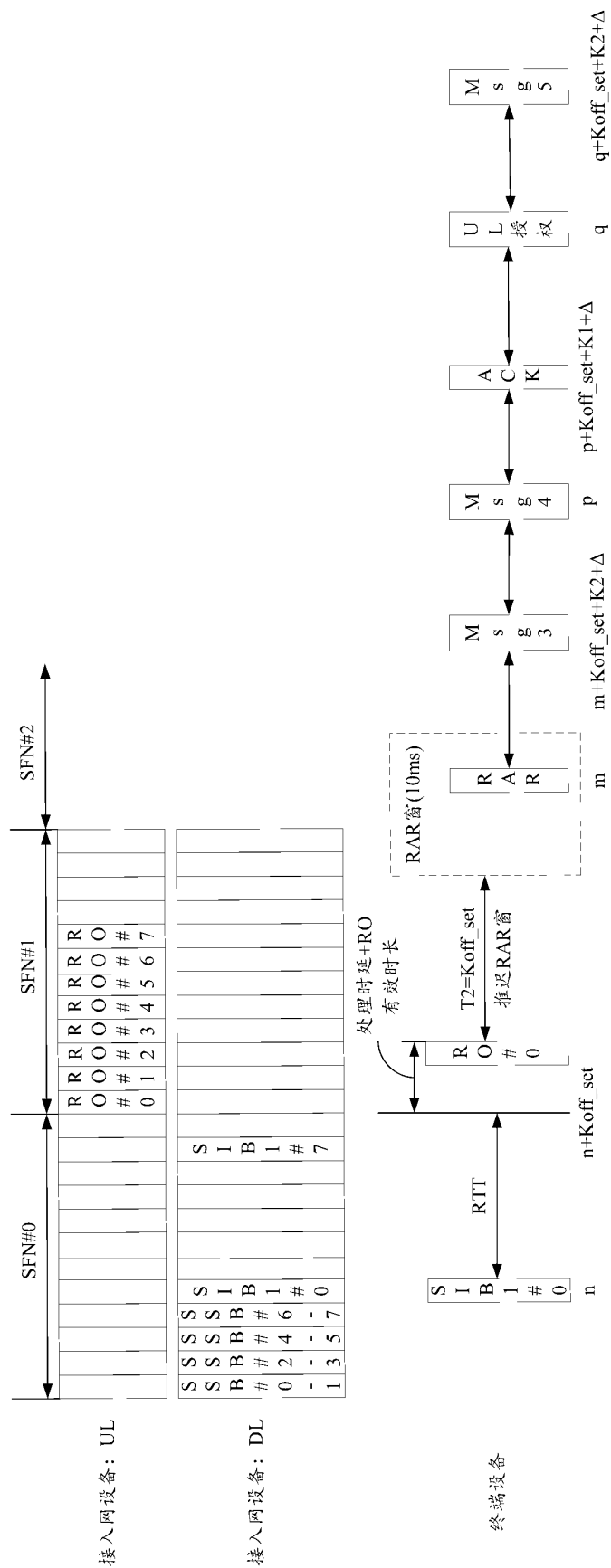


图 22

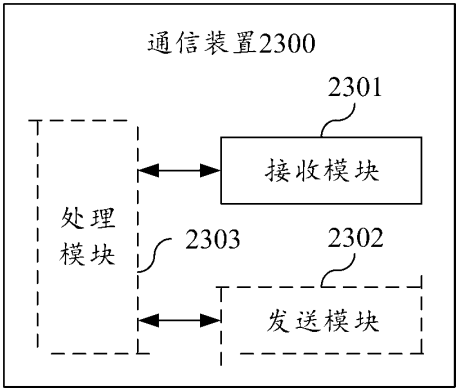


图 23

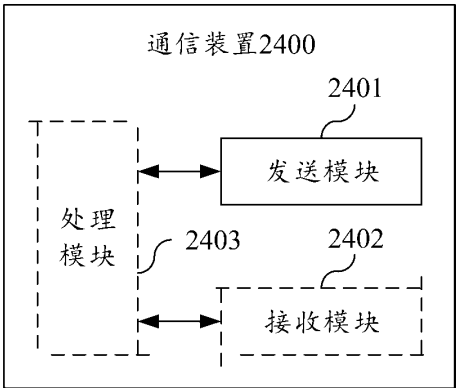


图 24

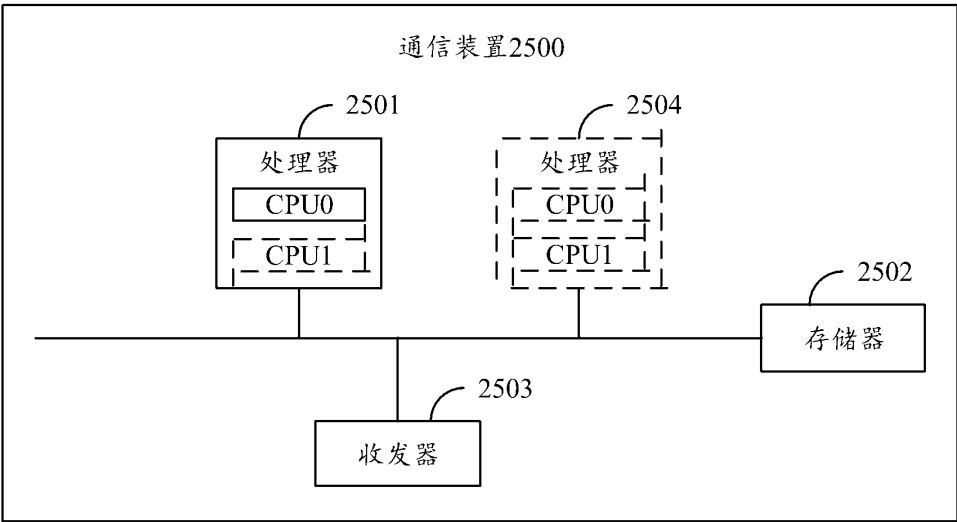


图 25