INTERCONNECTS FOR PACKAGED SEMICONDUCTOR DEVICES AND METHODS FOR MANUFACTURING SUCH DEVICES

TECHNICAL FIELD

[0001] The present invention relates to interconnects for packaged semiconductor assemblies, stacked semiconductor assemblies, and methods for manufacturing such assemblies.

BACKGROUND

[0002] Semiconductor products require packaged semiconductor assemblies with a high density of devices in a relatively small space. For example, the space available for memory devices, processors, displays and other microfeature devices is continually decreasing in cell phones, personal digital assistants, laptop computers and many other products. One technique to increase the density of semiconductor devices within a given footprint is to stack semiconductor devices and assemblies, and many stacked semiconductor assemblies require adequate electrical interconnects within and between the packages.

[0003] Conventional interconnects electrically connect the integrated circuitry of a semiconductor device (such as a die) with other devices or stacked packages. These interconnects can be formed by creating a via in the packaging material and then filling or plugging the via with conductive material. Figure 1 illustrates an earlier interconnect 100 including a plugged via 110. The via 110 is formed by drilling or etching a hole through an interposer substrate 112. The interconnect is then formed by plating a conductive material 114 into the via 110, and patterning the conductive material 114 so that it is electrically isolated. The remaining void in the via 110 is filled with a conductive material 116 that plugs the via 110. The conductive material 114 electrically connects a pad 117 at a first side of the package with a solder ball 118 (or other conductive feature) at a second side of the package.

[0004] One challenge associated with the interconnect 100 in Figure 1 is the difficulty of achieving uniform metallization in the vias. Non-uniform plating within the vias decreases the

quality and integrity of the interconnect. For example, vias having a high aspect ratio (i.e., ratio of the depth to the size of the opening) are especially difficult to consistently plate and fill. Moreover, in certain circumstances the filling process can trap air in the via that can cause the interconnect or assembly to crack as the fill material and the assembly harden. Such non-uniformities in the vias provide inconsistent electrical connections and compromise the integrity of the metallization of the interconnects.

[0005] Other challenges associated with existing interconnects are the cost, time and complexity of forming, plating and filling the vias. Forming the vias by an ablation or drilling process typically requires forming individual vias in a sequential manner: this increases the processing time to form the vias. Simultaneously forming the vias by an etching process can be much faster, but etching can result in inconsistent sizes of the vias. It can also be difficult to achieve a dense distribution of the vias with an etching process. Moreover, the plating and filling processing steps following the via formation require additional processing time.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 is a side cross-sectional view of a portion of an interconnect in an interposer substrate in accordance with the prior art.

[0007] Figure 2 is a side cross-sectional view of a stacked semiconductor assembly in accordance with an embodiment of the invention.

[0008] Figures 3-8 are side cross-sectional views illustrating various stages in a method of forming interconnects in a packaged semiconductor assembly in accordance with embodiments of the invention.

[0009] Figure 9 is flow diagram of a process of forming a semiconductor assembly in accordance with still another embodiment of the invention.

[0010] Figures 10A and 10B are side cross-sectional views illustrating various stages in a method of forming interconnects in a packaged semiconductor assembly in accordance with still another embodiment of the invention.

[0011] Figures 11A-11C are side cross-sectional views illustrating various stages in a method of forming interconnects in a packaged semiconductor assembly in accordance with still another embodiment of the invention.

[0012] Figure 12 is a flow diagram of a process of forming an interconnect in a packaged assembly in accordance with still another embodiment of the invention.

[0013] Figure 13 is a schematic view of a system that incorporates packaged assemblies with interconnects in accordance with embodiments of the invention.

DETAILED DESCRIPTION

[0014] Several embodiments of the present invention are directed toward packaged semiconductor devices with interconnects and methods of forming interconnects in packaged semiconductor devices. Many specific details of the invention are described below with reference to methods of forming the interconnects. The term "semiconductor assembly" is used throughout to include a variety of articles of manufacture including, for example, semiconductor wafers having active components, individual integrated circuit dies, packaged dies, and two or more semiconductor devices or assemblies in a stacked configuration. Many specific details of certain embodiments of the invention are set forth in Figures 2-13 and the following text to provide a thorough understanding of these embodiments. Several other embodiments of the invention can have different configurations, components or processes than those described in this section. A person skilled in the art, therefore, will appreciate that the invention may have additional embodiments or that the invention may be practiced without several details of the embodiments shown in Figures 2-13.

[0015] Figure 2 is a side cross-sectional view of a stacked semiconductor assembly 200 in accordance with one embodiment of the invention. The assembly 200 includes two or more packaged semiconductor assemblies 210 in a stacked configuration. In this embodiment, each assembly 210 includes a microelectronic die 220 attached to a support layer 230, and a plurality of interconnects 240 retained in and projecting from the support layer 230 in a predetermined configuration. The interconnects 240 can comprise a plurality of preformed pin-like members or other pre-formed conductive structures. Individual assemblies 210 also include an encapsulant 250

molded over the die 220 and between the interconnects 240. In the illustrated embodiment, each assembly 210 can further include optional first and second redistribution structures 260 and 270 at opposite sides of the package, and a plurality of conductive members 280 attached to the first redistribution layer 260. As explained in more detail below, the interconnects 240 can (a) provide high quality through package interconnections, (b) be formed relatively quickly, and (c) simplify the processing steps.

[0016] In the embodiment shown in Figure 2, individual interconnects 240 are preformed pins or pin-like members extending from a first side 211 of the package to a second side 212 of the package. The pre-formed pins provide a uniform electrical connection through the package 210 without requiring the complex processes of forming, plating and filling vias through a package as in conventional interconnects. Instead of forming and filling vias, the interconnects 240 are pre-formed in a separate process and then retained in a desired configuration before encapsulating the die 220 with the encapsulant 250. In certain embodiments, the interconnects 240 can be composed of a conductive material such as copper, nickel, gold and/or silver, or any other suitable conductive material(s). Individual interconnects 240 can also have a generally cylindrical shape and are all approximately the same size. In certain embodiments however, the interconnects 240 may differ in size or shape according to the needs and application of the packaged assembly. The interconnects 240 typically have a diameter of 100 μm or more, although in certain embodiments the diameter may be less. As explained in more detail below, the interconnects 240 are inserted into the support layer 230, a plate (not shown), or another type of support member in a predetermined configuration or array. Thereafter, the support layer 230 (or plate) retains the interconnects 240 in the desired configuration while the encapsulant 250 is molded around the interconnects 240 and the die 220. As such, the interconnects 240 provide a continuous and uniform conductive structure through the encapsulation 250 and avoid some of the complexities associated with forming, plating and filling vias of conventional interconnects described above.

[0017] Figures 3-8 illustrate various stages in a method of forming a plurality of discrete arrays of the interconnects 240 of Figure 2 in accordance with one embodiment of the invention. Figure 3, more specifically, illustrates a stage in which a plurality of discrete arrays of interconnects 240 have been mounted to a support plate 214 in a desired configuration. The interconnects 240 can

be mounted to the support plate 214 by loading the preformed interconnects 240 into a socket 208 that releasably retains second portions 244 of the interconnects 240 (shown in broken lines). In operation, the socket 208 moves towards the plate 214 (arrows 209) to insert first portions 242 of individual interconnects 240 into corresponding recesses 216 in the plate 214. The second portions 244 of the interconnects 240 are free-standing without a solid material between the second portions 244 at this stage. In this manner, the plurality of interconnects 240 are at least substantially simultaneously mounted to the plate 214. In certain embodiments, the interconnects 240 can be mounted to the plate 214 individually. The recesses 216 can be precision machined holes arranged in a predetermined array corresponding to an interconnect array at a die site of the semiconductor assembly. Such precision machining can enable the recesses 216 to be arranged in a dense array. The first portions 242 can optionally have a beveled or pointed portion 243 to facilitate inserting the interconnects 240 in the recesses 216. The lower portion of the plate 214 is sufficiently thick so that the recesses 216 have a sufficient depth to retain the interconnects 240 in a desired configuration during subsequent processing steps. In certain embodiments, the interconnects 240 can be ultrasonically welded or otherwise adhered to the plate 214, and therefore the plate 214 in such embodiments does not need to have the recesses 216.

[0018] The plate 214 can be composed of a metal or a synthetic material, such as an epoxy. In the case of an epoxy plate, it can include the recesses 216 or the epoxy can be partially cured to provide a "self-embedding" plate such that the interconnects 240 can be inserted into the plate 214 without any preformed holes. Once the interconnects 240 are in place, the epoxy plate 214 can be further cured or hardened. This type of self-embedding epoxy plate may mitigate errors caused by misalignment between the interconnects 240 and the recesses 216 in a rigid plate.

[0019] The procedure illustrated in Figure 3 can be performed in a short period of time because the plurality of interconnects 240 can be formed and arranged off-line and then simultaneously mounted to the plate 214 in a single step. This reduces the number of processing steps and thus the processing time. The socket 208 can be a device similar to a test socket or test probe, as is known in the art for electrical testing of packaged assemblies, and used to simultaneously insert multiple interconnects 240 into the plate 214. Moreover, the insertion process can be automated using existing technologies.

[0020] After mounting the interconnects 240 to the plate 214, Figure 4 illustrates a stage in which a dielectric support layer 230 is formed or otherwise disposed in a cavity 215 of the plate 214 and around the interconnects 240. The support layer 230 in Figure 4 has a first surface 232 contacting the plate 214, and a second surface 234 spaced apart from the first surface 232. In certain embodiments, the support layer 230 can be a polymer disposed in the cavity 215 to surround each of the interconnects 240. Accordingly, the thickness of the support layer 230 can vary according to the depth of the cavity 215 or how much the cavity 215 is filled with the support layer 230.

[0021] The support layer 230 provides a dielectric material between the conductive interconnects 240, and the support layer 230 can also retain the first portions 242 of the interconnects 240 in the desired configuration. For example, the support layer 230 can be at least partially cured or hardened to hold the interconnects 240 in a desired configuration during subsequent molding and material removal steps. In certain embodiments, the support layer 230 can be disposed in the cavity 215 before the interconnects 240 are inserted into the plate 214. In this embodiment, the interconnects 240 are inserted through the support layer 230 and into the individual recesses 216 in the plate 214 before curing the support layer 230.

[0022] The support layer 230 can also provide a surface to which a plurality of dies can be mounted. For example, the support layer 230 can be a polymeric material in which the second surface 234 becomes tacky in a partially or fully cured state, or a separate adhesive layer can be applied to the second surface 234. Accordingly, individual dies can be securely attached to the second surface 234 of the support layer 230. Moreover, in certain embodiments the support layer 230 can also be a photoimageable polymer that can be patterned to open bond-sites or conductive features on the die.

[0023] Figure 5 illustrates a stage in which a plurality of semiconductor dies 220 have been attached to the second surface 234 of the support layer 230. In this embodiment, the active surfaces of individual dies 220 are adhered to the second surface 234 of the support layer 230. The support layer 230 also provides a passivation or protective layer on the active surfaces of the dies 220. The support layer 230 can be deformable at this state so that optional conductive members 228 can project from bond-sites 222 of the dies 220 into the support layer 230. In certain embodiments, the conductive member 228 can be a stud bump formed on the die 220 before the die 220 is attached to

the support layer 230. One skilled in the art will appreciate that the die 220 can include other bond-sites or electrically connective features, or that the backside of the die 220 can be attached to the support layer 230.

[0024] Figure 6 illustrates a stage in which the encapsulation 250 has been disposed around the components of the sub-assemblies 210 to form a semiconductor workpiece 213. The encapsulant 250 can be composed of a different materials, such as thermosets, thermoplastics, hybridized versions of thermosets and thermoplastics, or any other suitable encapsulating material. In one embodiment, the subassembly of the plate 214, interconnects 240 and dies 220 is positioned in a mold (not shown), and the encapsulant 250 is then molded between the interconnects 240 and over the dies 220 such that the encapsulant 250 at least partially covers each of the dies 220. The mold can be shaped like a conventional semiconductor wafer so that subsequent processes can be performed in wafer processing equipment. The plate 214 and support layer 230 support and retain the interconnects 240 in the predetermined array during the molding process. The encapsulant also protects the dies 220 from contamination (e.g., moisture, particulates, etc.) and electrically isolates the interconnects 240. The thickness of the encapsulant 250 can vary with respect to the length of the interconnects 240. For example, in certain embodiments, the surface of the encapsulant 250 can be co-planar with the second portions 244 of the interconnects 240 after molding as indicated by the portion 252 of the encapsulant 250. In other embodiments, the second portions 244 of the interconnects 240 can be completely over-molded with the encapsulant 250 as indicated by the broken line and the portion 254 of the encapsulant 250. Material removal steps explained below are also used to adjust the thickness of the encapsulant 250 and surface characteristics of the workpiece 213.

[0025] Figure 7 illustrates a stage in which material has been removed from opposite surfaces of the workpiece 213. In one embodiment, the workpiece 213 is ground, planarized and/or etched to remove the material from a first surface 290 of the workpiece 213. The first surface 290, for example, can be formed by removing the material portions of the plate 214 and the support layer 230 to expose the first portions 242 of the interconnects 240. A portion 217 of the plate 214 can remain with the workpiece 213 even though the lower portion of the plate 214 has been removed. A portion of the support layer 230 can also remain to provide a dielectric passivation layer at the

surface of the die 220. In the embodiments where the dies 220 include conductive members 228, material can be removed from the workpiece 213 until the conductive members 228 are also exposed. In an optional embodiment, a second surface 292 of the workpiece 213 can be ground, planarized and/or etched to remove a portion of the encapsulant 250 from the workpiece 213. This process can remove a portion of the second portions 244 of the interconnects 240 and expose or clean the second portions 244 of the pins. Accordingly, the thickness 256 of the workpiece 213 can be controlled by accurately forming the first and second surfaces 290 and 292.

[0026] Figure 8 is cross-sectional view of the assembly 210 after a first redistribution structure 260 has been formed at the first side 290 of the workpiece 213, and a second redistribution structure 270 has been formed at the second side 292 of the workpiece 213. The first and second redistribution structures 260 and 270 can be configured to electrically connect the bond-sites 222 of the dies 220 to one or more of the interconnects 240. In embodiments without conductive members 228 projecting from the die 220, the support layer 230 is patterned to expose the bond-sites 222, and then bumps, balls, wire bonds or other conductive members are attached to the bond-sites 222. For example, a support layer 230 composed of a photoimageable polymer can be patterned to expose the bond-sites 222. In embodiments where conductive members 228 project from the die 220 and are exposed by the material removal processes, the first redistribution structure 260 electrically connects the conductive members 228 to one or more of the interconnects 240.

[0027] Several embodiments of the assemblies 210 with interconnects 240 can provide consistent electrical properties. For example, the preformed interconnects 240 can be formed off-line apart from the packaging process such that they are consistently solid and void-free. Additionally, molding over the pre-inserted interconnects 240 can be a fast and relatively cost effective method of forming the interconnects through the encapsulant 250 because the foregoing process eliminates the patterning, etching, plating and filling processing steps used in conventional processes for forming interconnects.

[0028] One skilled in the art will appreciate that individual dies 220 can have additional bond-sites or active surfaces proximate to the second surface 292 of the package 210. Accordingly, in certain embodiments, the second redistribution structure 270 can also electrically connect to the die 220 to the second surface 292 of the package 210. A plurality of conductive features, such as the

solder balls illustrated in Figure 2, may also be attached to and project from the first and second redistribution structures 260 and 270. After forming the redistribution structures 260 and 270, the sub-assemblies 210 can be singulated from the workpiece 213. In certain embodiments, for example, the sub-assemblies can be singulated with a wafer saw or other singulating devices that are known in the art.

[0029] Figure 9 is a flow diagram of an embodiment of a method or process 900 for forming a semiconductor assembly. In this embodiment, the process 900 includes mounting preformed interconnect structures to a plate in a predetermined array of interconnects for the assembly (block 905). In one embodiment, a socket holding a plurality of the interconnect structures can simultaneously mount or insert the interconnect structures in apertures or recesses in the plate. Once the interconnect structures have been mounted, the socket can release the interconnect structures and move away from the plate. The plate can be made of a metallic or synthetic material, and the apertures or recesses can extend through the plate or to a predetermined depth of the plate. The process also includes forming a dielectric support layer on the plate and around the interconnect structures (block 910) and positioning a die on the support layer (920).

[0030] The process further includes encasing at least a portion of the plate, support layer, die and interconnect structures in an encapsulant (block 920). In certain embodiments encasing the components of the assembly can include forming a generally coplanar exterior surface of the encapsulant with second portions of the interconnect structures spaced apart from the support layer. In other embodiments, the second portions can be completely over-molded. The process also includes exposing portions of the interconnect structures (block 925). In certain embodiments, exposing these portions can include planarizing first and second sides of the assembly to expose the interconnect structures. As such, the plate can be a sacrificial layer and at least partially removed during the planarization. Exposing these portions in other embodiments can also include forming a generally coplanar first and second surfaces of the assembly with first and second portions of the interconnect structures.

[0031] The process illustrated in Figure 9 can be accomplished in a short period of time because individual vias do not have to be formed, plated and filled to create the interconnect

structures. Rather, the encapsulant encases the interconnects or pins after the pins have been retained in the predetermined array.

[0032] Figures 10A and 10B illustrate various stages in a method for forming interconnects in a semiconductor assembly in accordance with another embodiment of the invention. Figure 10A, more specifically, is a side cross-sectional view of an embodiment of the invention having a plate 314 similar to the plate described above, except that the plate 314 can be removed from the sub-assembly or workpiece. The plate 314 releasably receives the plurality of the interconnects 240 in a plurality of recesses 316 arranged in a predetermined interconnect array. Individual recesses 316, however, do not extend all the way through the plate 314. Accordingly, when the first portion 242 of a pin 240 is inserted in the recess 316, the pin 240 does not extend to a lower surface 317 of the plate 314. In certain embodiments, the first portions 242 of the pins 240 can be configured to have a semi-blunt end portion, such as a dowel-like first portion 242 illustrated in Figures 10A and 10B. The plate 314 also includes a cavity 315 for receiving the support layer 230. After forming the support layer 330 in the cavity 315, processing can continue as described above with respect to Figures 5 and 6, including attaching a plurality of dies 220 to the support layer 330 and disposing the encapsulant 250 around the interconnects 240 and dies 220.

[0033] Figure 10B illustrates a stage in which an encapsulant 250 has been disposed around the interconnects 240 and dies 220, and the plate 314 has been removed from the support layer 330 and interconnects 240. After the plate 314 is removed, processing can continue as described above with respect to Figures 7-8, including removing material and forming redistribution structures. The removable plate 314 illustrated in Figures 10A and 10B can save material cost and processing time because the material removal steps (e.g., planarizing) will not have to remove the plate 314 with the other package materials. The removable plate 314 can also be reused for other semiconductor assemblies having the same interconnect configuration.

[0034] Figures 11A-11C illustrate various stages in a method for forming interconnects in a semiconductor assembly according to still another embodiment of the invention. The manufacturing process and interconnects illustrated in Figures 11A-11C have similar features to the embodiments described above, however the first portions 242 of the interconnects 240 are retained solely by a support layer 430 and not inserted into a separate support plate. Figures 11A and 11B,

for example, illustrate a stage in which the interconnects 240 are temporarily retained by a socket 402 and inserted into the support layer 430. The support layer 430 can be a polymer, and at the stage shown in Figures 11A and 11B the support layer is in a state in which the interconnects can penetrate the support layer 430. In certain embodiments, the first portions 242 of the interconnects 240 can have different configurations, such as the beveled or pointed first portions 243, flat portions 245 (shown at the right of Figure 11A), or other configurations suitable for embedding and retaining the interconnects 240 in a stable manner. While the socket 402 holds the interconnects 240 in a desired configuration, the support layer 430 can be at least partially cured or otherwise processed to retain the interconnects 240 in the desired configuration. The socket 402 subsequently releases the second portions 244 of the interconnects (Figure 11C) and the support layer 430 holds the interconnects 240 in place. At this stage, the second portions 244 of the interconnects 240 (e.g., pins) are free-standing without a solid material between the second portions 244. The support layer 430 can also provide an adhesive surface 434 to which a die (not shown) can be attached as described above.

[0035] The embodiment illustrated in Figures 11A-11C retains the interconnects 240 in a desired configuration in the support layer 430 without inserting the first portions 242 of the interconnects 240 into holes in a separate plate. Accordingly, this embodiment may mitigate the need to align the interconnects 240 with holes or recesses in a separate support plate.

[0036] Figure 12 is a flow diagram of an embodiment of a method or process 1200 for forming an interconnect. The process 1200 includes inserting a plurality of preformed pins in a support member (block 1205). The support member can at least partially retain the pins in a predetermined array. The pins can include a first portion in the support member and a second portion opposite the first portion. Moreover, the plurality of pins can be simultaneously inserted in the support member. In one example, a socket holds the second portions of the pins, inserts the first portions of the pins in the support member in the predetermined array, and releases the second portions after the first portions are inserted and retained in the support member. The process also includes positioning a die on a first surface of the support member (block 1210). In certain embodiments, the process can include at least partially curing the support member prior to positioning the die on the support layer. The process further includes encasing at least a portion of

the die and pins with an encapsulant (block 1215) and at least partially exposing the pins (block 1220).

[0037] Any one of the semiconductor assemblies having the interconnects described above with reference to Figures 1-12 can be incorporated into any of a myriad of larger and/or more complex systems, a representative example of which is system 1300 shown schematically in Figure 13. The system 1300 can include a processor 1302, a memory 1304 (e.g., SRAM, DRAM, flash and/or other memory devices), input/output devices 1306 and/or other subsystems or components 1308. The semiconductor assemblies having interconnects described above with reference to Figures 1-12 may be included in any of the components shown in Figure 13. The resulting system 1300 can perform any of a wide variety of computing, processing, storage, sensing, imaging and/or other functions. Accordingly, the representative systems 1300 include, without limitation, computers and/or other data processors, for example, desktop computers, laptop computers, Internet appliances, hand-held devices (e.g., palm-top computers, wearable computers, cellular or mobile phones, personal digital assistants, music players, etc.), multi-processor systems, processor–based or programmable consumer electronics, network computers and minicomputers. Other representative systems 1300 may be housed in a single unit or distributed over multiple interconnected units (e.g., through a communication network). The components of the system 1300 can accordingly include local and/or remote memory storage devices, and any of a wide variety of computer readable media.

[0038] From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but well-known structures and functions have not been shown or described in detail to avoid unnecessarily obscuring the description of the embodiments of the invention. For example, the backside of the dies 220 can be mounted to the support layer 230 such that the bond-sites 222 face away from the support layer 220. The bond-sites 222 can be protected during the molding procedure such that they are not covered by the encapsulant 250, and then the bond-sites 222 can be electrically connected to corresponding interconnects (e.g., via wire bonding or redistribution structure). Where the context permits, singular or plural terms may also include the plural or singular term, respectively. Moreover, unless the word "or" is expressly limited to mean only a single item exclusive from the other items in reference to a list of two or more items, then the use of "or" in such a list is to be interpreted as

including (a) any single item in the list, (b) all of the items in the list, or (c) any combination of the items in the list. Additionally, the term "comprising" is used throughout to mean including at least the recited feature(s) such that any greater number of the same feature and/or additional types of features are not precluded.

[0039] Various modifications may be made without deviating from the embodiments of the invention. For example, features described in the context of particular embodiments may be combined or eliminated in other embodiments. Further, while advantages associated with certain embodiments of the invention have been described in the context of those embodiments, other embodiments may also exhibit such advantages, and not all embodiments need necessarily exhibit such advantages to fall within the scope of the invention. For example, the interconnect structures (e.g., pins) can be retained by another type of support member before molding the encapsulant around the die and interconnects. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

We claim:

[c1] 1. A semiconductor assembly, comprising:

a semiconductor die having a plurality of bond-sites;

a dielectric support layer having a first side and a second side, wherein the die is attached to the second side of the support layer;

a plurality of preformed conductive interconnects, wherein individual interconnects have a first portion in the support layer and a second portion spaced apart from the support layer; and

a dielectric encapsulant between the interconnects and around at least a portion of the die.

[c2] 2. The assembly of claim 1 wherein the support layer is a photoimageable polymer.

[c3] 3. The assembly of claim 1 wherein the support layer is a polymer that adheres to the die.

[c4] 4. The assembly of claim 1 wherein the interconnects are arranged in a predetermined pattern outside of a footprint of the die, and the dielectric encapsulant is in a flowable state.

[c5] 5. The assembly of claim 1 wherein the die has a first height and the interconnects have a second height greater than the first height.

[c6] 6. The assembly of claim 1 wherein the interconnects comprise a plurality of preformed pins, and wherein the first portions of the pins have a beveled portion.

[c7] 7. The assembly of claim 1, further comprising at least a portion of a plate at least partially surrounding the support layer.

[c8] 8. The assembly of claim 1 wherein the semiconductor assembly is a first semiconductor assembly and wherein a second semiconductor assembly generally similar to the first semiconductor assembly is stacked on the first semiconductor assembly.

[c9] 9. A plurality of through package interconnects in a semiconductor assembly including a die, a dielectric support layer, and an encapsulant, the interconnects comprising:

a plurality of preformed electrically conductive pins projecting from the support layer in a predetermined array outside of a footprint of the die, wherein the pins are arranged in the predetermined array apart from the encapsulant.

[c10] 10. An intermediate article of manufacture of a semiconductor assembly, comprising:

a dielectric support layer;

a plurality of semiconductor dies attached to the support layer such that individual dies are at die sites across the support layer; and

a plurality of preformed conductive pins having first portions retained in the support layer and second portions projecting from the support layer, wherein the pins are arranged in a plurality of discrete pin arrays, and wherein the second portions of the pins are free-standing without a solid material therebetween.

[c11] 11. The article of claim 10, further comprising a plate having a cavity, wherein:

the support layer is formed in the cavity; and

the pins are mounted to and project from the plate.

[c12] 12. The article of claim 11 wherein the plate is configured to be removable from the article.

[c13] 13. A system, comprising:

at least one of a processor, a memory device and an input or output device, wherein at least one of the processor, memory device and input or output device includes a semiconductor assembly comprising-

a die having a plurality of bond-sites;

a dielectric support layer, wherein the die is attached to the support layer;

a plurality of preformed conductive interconnects projecting from the support layer, wherein individual interconnects have a first portion in the support layer; and

a dielectric encapsulant molded between the interconnects and around at least a portion of the die.

[c14] 14. A method of forming a semiconductor assembly comprising:

retaining an array of preformed interconnects in a support member before disposing an encapsulant between the interconnects;

positioning a die relative to the array of interconnects; and

disposing an encapsulant between the interconnects and over at least a portion of the die after positioning the die relative to the interconnects.

[c15] 15. The method of claim 14 wherein the support member comprises a plate, and wherein retaining the preformed interconnects comprises mounting the preformed interconnects to the plate.

[c16] 16. The method of claim 15, further comprising forming a support layer on the plate, wherein the plate and the support member retain the preformed interconnects.

[c17] 17. The method of claim 15 wherein mounting preformed interconnects to the plate comprises inserting the interconnects into corresponding recesses in the plate.

[c18] 18. The method of claim 17, further comprising inserting the plurality of interconnects into the plate simultaneously.

[c19] 19. The method of claim 15 wherein mounting preformed interconnects to the plate comprises:

retaining the interconnects in a socket;

moving the socket toward the support plate; and

releasing the interconnects from the socket after the interconnects are inserted into the plate.

[c20] 20. The method of claim 15, further comprising removing the plate after disposing the encapsulant between the interconnects.

[c21] 21. The method of claim 14 wherein the support member comprises a dielectric support layer, and wherein positioning the die comprises mounting the die to the support layer.

[c22] 22. The method of claim 21 wherein retaining the preformed interconnects comprises inserting the preformed interconnects into the support layer and subsequently hardening the support layer.

[c23] 23. The method of claim 14 wherein the support member comprises a plate and a dielectric support layer on the plate.

[c24] 24. The method of claim 14, further comprising exposing portions of the interconnects.

[c25] 25. The method of claim 24 wherein exposing portions of the interconnects includes planarizing a first side and/or a second side of the assembly.

[c26] 26. The method of claim 24 wherein exposing portions of the interconnects includes removing at least a portion of a support layer that retains the interconnects until a desired thickness of the assembly is reached.

[c27] 27. The method of claim 24 wherein exposing portions of the interconnects includes forming an approximately coplanar surface of a support layer that retains first portions of the interconnects and forming an approximately coplanar surface of an encapsulant at second portions of the interconnects opposite from the first portions.

[c28] 28. The method of claim 14 wherein disposing the encapsulant between the interconnects, further comprises forming an exterior surface of the encapsulant to be at least generally coplanar with second portions of the interconnects.

[c29] 29. The method of claim 14, further comprising at least partially curing the support member.

[c30] 30. The method of claim 24 wherein the semiconductor assembly is a first semiconductor assembly and the method further comprises forming a second semiconductor assembly generally similar to the first assembly and singulating the first and second semiconductor assemblies.

[c31] 31. A method of forming packaged assembly, comprising:

inserting a plurality of preformed pins in a support layer, wherein individual pins have a first portion in the support layer and a second portion opposite the first portion, wherein the support layer at least partially retains the pins in a predetermined array;

positioning a die on a first surface of the support layer;

encasing at least a portion of the die and the pins in an encapsulant; and

exposing the first and second portions of the pins.

[c32] 32. The method of claim 31, further comprising at least partially curing the support layer before positioning the die on the first surface of the support layer.

[c33] 33. The method of claim 31 wherein the pins are inserted simultaneously into the support layer.

[c34] 34. The method of claim 31 wherein inserting the plurality of preformed pins in the support layer comprises:

retaining the second portions of the pins in a socket;

moving the socket in a first direction toward the support layer; and

releasing the second portions of pins from the socket after the pins are inserted in the support layer.