CLAIMS

What is claimed is:

1. A phase change memory (PCM) device comprising:

a bottom electrode;

a bottom heater over the bottom electrode;

a bottom buffer layer over the bottom heater;

a PCM region over the bottom buffer layer;

a top buffer layer over the PCM region;

a top heater over the top buffer layer; and

a top electrode over the top heater.

2. The PCM device according to claim 1, wherein the bottom buffer layer comprises a material selected from the group consisting of: C, TiN, TaN, TiC, TaC, TiAlN, TaAlN, TiAlC, TaAlC, HfN, and WN.

3. The PCM device according to claim 1 wherein the bottom heater comprises titanium nitride or tantalum nitride.

4. The PCM device according to claim 1 wherein the PCM region comprises a material selected from the group consisting of: Sb(x)Te(y), Ge(x)Sb(y)Te(z), and In(x)Se(y), wherein x, y, and z are integers.

5. The PCM device according to claim 1, wherein the PCM region comprises a thickness of less than about 100 nm.

6. The PCM device according to claim 1, wherein the PCM region comprises a thickness of less than about 20 nm.

7. The PCM device according to claim 1, wherein:

the PCM region comprises a thickness of between about 1 and about 100 nm; and

the PCM region comprises a material selected from the group consisting of: Sb(x)Te(y), Ge(x)Sb(y)Te(z), and In(x)Se(y), wherein x, y, and z are integers.

8. A method of fabricating a semiconductor device, the method comprising:

forming a bottom electrode upon a substrate;

forming a bottom heater over the bottom electrode;

forming a bottom buffer layer over the bottom heater;

forming a PCM region over the bottom buffer layer;

forming a top buffer layer over the PCM region;

forming a top heater over the top buffer layer; and

forming a top electrode over the top heater.

9. The method according to claim 8, wherein the bottom buffer layer comprises a material selected from the group consisting of: C, TiN, TaN, TiC, TaC, TiAlN, TaAlN, TiAlC, TaAlC, HfN, and WN.

10. The method according to claim 8, wherein the buffer layer comprises germanium telluride.

11. The method according to claim 8, wherein the bottom heater comprises tantalum nitride.

12. The method according to claim 8, wherein the PCM region comprises a material selected from the group consisting of: Sb(x)Te(y), Ge(x)Sb(y)Te(z), and In(x)Se(y), wherein x, y, and z are integers.

13. The method according to claim 8, wherein the PCM region has a thickness of less than about 100 nm.

14. The method according to claim 8, wherein the PCM region has a thickness of less than about 20 nm.

15. A method for utilizing a phase change memory (PCM) semiconductor logic circuit, the circuit comprising a PCM cell disposed in series between a first node and a second node, wherein the first node is configured to receive a first write pulse, the second node is configured to receive a second write pulse, and the circuit is configured to receive a read pulse across the first node and the second node, the method comprising:

concurrently applying the first write pulse and the second write pulse to the PCM cell prior to a logical write operation, wherein a voltage amplitude of the first write pulse and a voltage amplitude of the second write pulse combine to exceed a reset voltage amplitude of the PCM cell;

concurrently writing a first logical state of the first node to the PCM cell and ~~and~~ writing a second logical state of the second node to the non-volatile memory;

applying a read pulse across the first node and the second node; and

interpreting a logical state of the circuit according to a current associated with the read pulse.

16. The method according to claim 15, wherein a voltage amplitude of the second write pulse exceeds a set voltage of the PCM cell and is less than a reset voltage of the PCM cell.

17. The method according to claim 15, wherein the first write pulse and the second write pulse have opposite polarities.

18. The method according to claim 15, wherein a voltage amplitude of the first write pulse exceeds a set threshold of the PCM cell and is less than a reset voltage of the PCM cell.

19. The method according to claim 15, wherein a voltage amplitude of the read pulse is less than a set threshold of the PCM cell.

20. The method according to claim 15, wherein the circuit comprises an XOR logic circuit.