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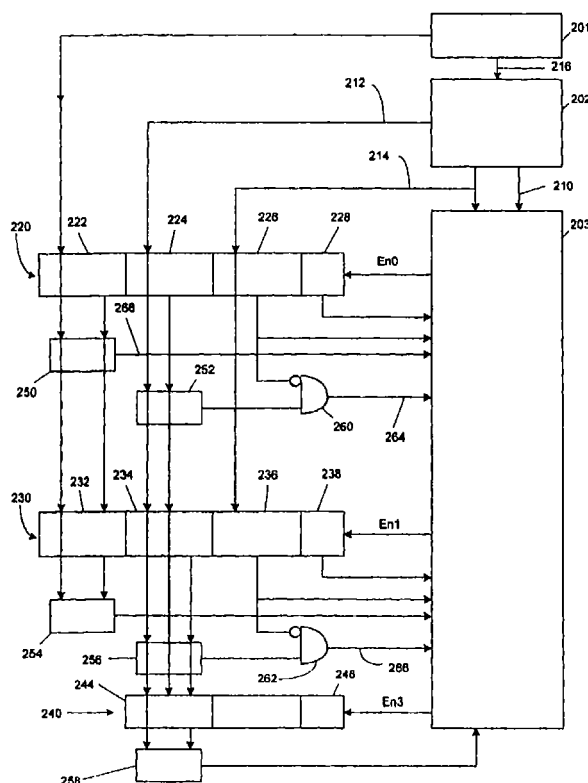
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(54) Title: METHOD AND APPARATUS FOR BUILT-IN SELF-REPAIR OF MEMORY STORAGE ARRAYS



(57) Abstract: An integrated circuit device includes a memory array (10) having a plurality of memory cells arranged in a plurality of rows (12) and a plurality of columns (23). First and second redundant rows (17) of memory cells and a first redundant column (18) of memory cells are provided. A test circuit (201) is coupled to the memory array (10) and is adapted to test a plurality of memory cells coupled to each of the plurality of rows (21). A control circuit (203) is coupled to the test circuit (201) and is adapted to receive test results from the test circuit (201), the control circuit (203) being adapted to respond to a detection of a defective memory cell to determine an assignment of at least one of the first and second redundant rows (17) and first redundant column (18). A first register (220) is coupled to the control circuit (203) and adapted to receive an assignment of the first redundant row (17) in response to a determination by the control circuit (203), a second register (240) is coupled to the control circuit (203) and adapted to receive an assignment of the first redundant column (18) in response to a determination by the control circuit (203), and a third register (230) is coupled to the control circuit (203) and adapted to receive an assignment of the second redundant row (17) in response to a determination by the control circuit (203).

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