

(12) 按照专利合作条约所公布的国际申请

(19) 世界知识产权组织
国际局

(43) 国际公布日
2026 年 2 月 19 日 (19.02.2026)



(10) 国际公布号
WO 2026/036829 A1

(51) 国际专利分类号:
H01L 23/552 (2006.01)

(21) 国际申请号: PCT/CN2025/096162

(22) 国际申请日: 2025 年 5 月 21 日 (21.05.2025)

(25) 申请语言: 中文

(26) 公布语言: 中文

(30) 优先权:
202411133716.9 2024 年 8 月 16 日 (16.08.2024) CN

(71) 申请人: 长鑫科技集团股份有限公司 (CXMT CORPORATION) [CN/CN]; 中国安徽省合肥市经济技术开发区空港工业园兴业大道 388 号 230601 (CN)。

(72) 发明人: 梁智玮 (LIANG, Zhiwei); 中国安徽省合肥市经济技术开发区空港工业园兴业大道 388 号 230601 (CN)。

(81) 指定国(除另有指明, 要求每一种可提供的国家保护): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU,

CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UY, UZ, VC, VN, WS, ZA, ZM, ZW。

(84) 指定国(除另有指明, 要求每一种可提供的地区保护): ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), 欧亚 (AM, AZ, BY, KG, KZ, RU, TJ, TM), 欧洲 (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG)。

本国际公布:
— 包括国际检索报告(条约第 21 条(3))。

(54) Title: SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREFOR

(54) 发明名称: 半导体结构及其制作方法

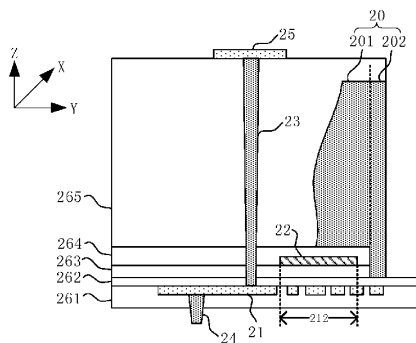


图 1

(57) Abstract: The present disclosure provides a semiconductor structure and a manufacturing method therefor. The semiconductor structure at least comprises: a bottom conductive layer and a blocking part, wherein the plane where the blocking part is located is located above the plane where the bottom conductive layer is located, and the projections of the blocking part and the bottom conductive layer in a vertical direction have an overlapping region; a three-dimensional structure, wherein the three-dimensional structure comprises a first part and a second part, the top surface of the blocking part is higher than the bottom surface of the second part and lower than or flush with the bottom surface of the first part, and the first part is at least partially located directly above the overlapping region; contact holes and a first conductive layer, wherein the plane where the first conductive layer is located is higher than the top surface of the three-dimensional structure, the contact holes are directly connected to the first conductive layer, the bottom conductive layer is electrically connected to the first conductive layer by means of the contact holes, and the contact holes are located at the side of the first part away from the second part; and a first isolation layer, wherein the first isolation layer is used for filling the region between each contact hole and the three-dimensional structure, and filling the region between different contact holes.

[见续页]

(57) 摘要: 本公开提供一种半导体结构及其制作方法, 半导体结构至少包括: 底层导电层和格挡部, 格挡部所在平面位于底层导电层所在平面上方, 格挡部与底层导电层在竖直方向上的投影具有重叠区域; 立体结构, 立体结构包括第一部和第二部, 格挡部的顶面高于第二部的底面且低于或平齐于第一部的底面, 第一部至少部分位于重叠区域的正上方; 接触孔和第一导电层, 第一导电层所在平面高于立体结构的顶面, 接触孔与第一导电层直接连接, 底层导电层通过接触孔电连接第一导电层, 接触孔位于第一部远离第二部的一侧; 第一隔离层, 第一隔离层用于填充接触孔与立体结构之间的区域以及填充不同接触孔之间的区域。