FREQUENCY SEARCHER AND FREQUENCY-LOCKED DATA DEMODULATOR USING A PROGRAMMABLE ROTATOR

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0001] The present invention relates generally to communication systems. Particularly, the present invention relates to reverse link signal acquisition in a CDMA environment.

DESCRIPTION OF THE RELATED ART

[0002] The radio frequency (RF) spectrum is a limited commodity. Only a small portion of the spectrum can be assigned to each communications industry. The assigned spectrum, therefore, must be used efficiently in order to allow as many frequency users as possible to have access to the spectrum.

[0003] Multiple access modulation techniques are some of the most efficient techniques for utilizing the RF spectrum. Examples of such modulation techniques include time division multiple access (TDMA), frequency division multiple access (FDMA), and code division multiple access (CDMA).

[0004] CDMA modulation employs a spectrum technique for the transmission of information. The spread spectrum system uses a modulation technique that spreads the transmitted signal over a wide frequency band. This frequency band is typically substantially wider than the minimum bandwidth required to transmit the signal. A signal having a bandwidth of only a few kilohertz can be spread over a bandwidth of more than a megahertz.

[0005] CDMA communications systems typically use directional antennas located in the center of a cell and broadcasting into sectors of the cell. The cells are located in major metropolitan areas, along highways, and along train tracks to allow consumers to communicate both at home and while traveling.

[0006] All of the mobile telephones communicating in the CDMA system transmit on the same frequency. Therefore, in order for the base station to identify each mobile, each mobile is assigned a unique pseudorandom (PN) spreading code that identifies that particular mobile to the system.

[0007] The mobile begins the registration process with a CDMA system by sending out a preamble signal that is comprised of chips. A base station searches for the preamble to determine if a mobile station is trying to communicate with the system. The base station may have to integrate over thousands of chips to find the mobile's preamble signal. This is typically not a problem if the preamble signal is at the proper frequency being searched by the base station.

[0008] Due to the Doppler effect, the critical cells are the cells located near highways or railway tracks. If a mobile is approaching a base station, the Doppler effect increases the signal's frequency as observed by the base station. If the mobile is moving away from the base station, the base station observes a signal having a frequency that is less than the frequency transmitted by the mobile. The amount of frequency shift is a function of the speed of the mobile.

[0009] The frequency of a signal transmitted by the mobile is aligned with the local oscillator in the mobile. The base station's frequency is synchronized with the Global Positioning System. When the mobile acquires a signal from the base station, that signal's frequency will be off. The mobile uses this shifted frequency to adjust its local oscillator in order to transmit back on the same frequency it has received. The base station then receives a signal that is shifted again by the Doppler effect. The base station is therefore receiving a signal that has double the frequency error. The two-way Doppler offsets may be in the range from 420 Hz for highway traffic to 1200 Hz for high-speed trains.

[0010] A typical frequency searcher experiences difficulty finding the signals transmitted by mobile telephones due to the double Doppler effect. The double Doppler effect may reduce a mobile's signal as much as 24db below the threshold used by the searcher to find mobile signals. There is a resulting need for a frequency searcher that is capable of acquiring mobile signals that are affected by Doppler shift.

SUMMARY OF THE INVENTION

[0011] The present invention encompasses a searcher that finds and tracks the frequency of a received signal. The received signal typically is experiencing a phase error from the phase that for which the searcher is looking. The searcher comprises a frequency locked loop that generates a phase increment signal in response to the detected phase error of the incoming signal. This phase error is used to generate a phase increment signal. An accumulator is coupled to the frequency locked loop to accumulate the phase increments. After the accumulator has accumulated a predetermined phase increment, the accumulator generates a control signal to a

programmable rotator. The programmable rotator performs a phase rotation function in response to the control signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. 1 shows a block diagram of the Frequency Locked Loop with the programmable rotator of the present invention.

[0013] FIG. 2 shows a flowchart of a programmable rotator process of the present invention.

[0014] FIG. 3 shows a table of segment lengths (in PN chips) and phase increments for different frequency bins.

[0015] FIG. 4 shows a plot of the probability of pilot signal detection versus the frequency deviation in accordance with the programmable rotator of the present invention.

[0016] FIG. 5 shows a block diagram of a base station incorporating the searcher with the programmable rotator of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0017] The searcher of the present invention incorporating a Frequency Locked Loop (FLL) with a programmable rotator eliminates the searcher coherent loss resulting from the Doppler effect. The present invention provides a significant improvement of the searcher sensitivity by replacing a periodic 90° rotation with a programmable rotation of multiples of 45°. The searcher's performance is substantially equivalent to the searching technique known in the art as frequency binning.

[0018] In frequency binning, the intermediate frequency (IF) of the local oscillator adjusts the offset frequency control logic so that the baseband signal is already corrected by the amount required. The amount of correction or offset by the local oscillator represents the bin spacing.

[0019] However, in order to perform frequency binning, the hardware needs to introduce the frequency offset into the received signal. This cannot be done on a per mobile basis since all the mobiles are received together as a CDMA signal. Additionally, in cases when the frequency bin offset is introduced into the baseband signal, multiplication is generally required and the bit width of the datapath must increase. This increases the hardware complexity in a non-linear fashion.

[0020] The searcher process of the present invention replaces the frequency binning process by phase compensation or rotation that is applied to the baseband I/Q samples. In the preferred embodiment, the rotation is limited to multiples of 45° steps. Alternate embodiments use other rotation limits, such as 90° phase rotations.

[0021] The block diagram of FIG. 1 represents the searcher of the present invention, a FLL with hardware $\pi/4$ rotator. In the subsequent discussion of the present invention, each slot is divided into four 512-chip intervals, subsequently referred to as "segments". Each segment is further divided into 8 "sub-segments" each having a length of 64 chips. The pilot channel filtering is based on first accumulating the de-spread, hardware-rotated pilot chips over each segment and then suitably combining the result over four segments, spanning an interval of length 2048 chips.

[0022] Referring to FIG. 1, the preferred embodiment of the present invention is comprised of a rotator portion (101) together with a FLL portion (102). In the preferred embodiment, the rotator portion (101) is implemented in hardware while the FLL portion (102) is implemented in a digital signal processor (DSP).

[0023] In general, the FLL rotates each segment-sum and inputs it to a sliding window accumulator that sums its input over four segments. The output of the sliding window accumulator is then de-rotated to generate an output of the pilot filter that is valid for a given segment. The rotation of segment sums is used to align the phase of the pilot accumulated over each segment relative to one another. The de-rotation step is performed in order to align the phase of the pilot filter output with the phase of the signal at the midpoint of the segment over which the pilot filter output is used for demodulation.

[0024] Referring to FIG. 1, the first step in pilot filtering is to decover the pilot channel from the hardware rotator output and accumulate the result over each segment of 512 chips (105). The decovering operation is performed by the multiplier (126) that has the phase of the input signal, $e^{j2\pi f_e T_c}$, as one input. The phase signal is multiplied by the angle of rotation, $e^{-j\theta_R}$, from the hardware rotator (110). The generation of the angle of rotation is discussed subsequently.

[0025] The output of the multiplier (126) is the decovered pilot signal that is input to a summer (105) for accumulation over 512 chips. The accumulated signal is multiplied with the local estimate of the frequency error, $e^{-j\theta_L}$. The multiplier (130) output, $e^{-j\theta_e[m]}$, is then input to a discriminator (110) to determine the cross product. The FLL is driven by the output of the cross product between successive 512 chip accumulations of the pilot signal. The output of the discriminator (110) can be expressed as $G\sin(\delta\theta_e)$.

[0026] The output of the discriminator (110) is scaled by the "G" term to achieve the desired time constant/jitter variance. The cross product is applied to a loop filter (accumulator) (115) that is updated once every 512 chips. The output of the loop filter (115) provides the estimate, $\hat{f}_m$, of the frequency offset.

[0027] The FLL also keeps track of the phase relationship between different segments by associating each segment with an average phase. This is accomplished by multiplying the estimate of the frequency offset by $512T_C$ (116). At high frequency offsets, the instantaneous phase of the signal may vary considerably within each segment. The frequency estimate generated by the loop filter defines the phase shift between one segment and the next. It also defines the difference in the instantaneous phase of the signal from the beginning of the segment to the end.

[0028] The estimate of the average phase of the segment is used by the rotation and de-rotation of the pilot within the DSP portion (102). The hardware rotator (110) uses the estimated phase difference to rotate the signal within each segment so as to compensate for the change in instantaneous signal phase over the segment.

[0029] The rotator (110) operates under the hypothesis that the difference between the instantaneous phase of the signal and the average phase of the signal over the given segment varies linearly with time. It starts with an initial value, δ radians, at the beginning of the segment and ends with a final value of $-\delta$ radians at the end of the segment. With this assumption, the rotator (110) computes the average phase over each sub-segment (64-chip interval), quantized to the nearest multiple of $\pi/4$ radians. The resulting rotation is applied to each sub-segment of the received signal, over the given segment. As a result, the instantaneous phase of the signal at the output of the hardware rotator (110) remains nearly constant over each segment. The output of the hardware rotator (110) is used by the tracking loops, pilot filtering, and demodulation of a communications device.

[0030] The average phase of the signal over the segment is the same with or without the hardware rotator (110) of the present invention. Therefore, the hardware rotation process is transparent to pilot filtering and demodulation. The hardware rotator (110), however, provides coherence gain by reducing the variance of the instantaneous phase within each segment. If the frequency offset is small, then the hardware rotator (110) provides no rotation, and the system degenerates to the prior art implementation of a FLL.

[0031] In implementation, referring again to FIG. 1, the output of the multiplier (116) is input to an accumulator (117) that is updated every 512 chips. The output of the accumulator (117) is the angle of rotation, $\theta_L[m]$, that is input to the DSP rotator (120) to generate the local estimate of the frequency error, $e^{-j\theta_L}$.

[0032] The outputs of the FLL can be expressed in x (initial phase) and y (phase increment) terms as follows:

[0033]
$$x = \left\{-\hat{f}_m * \left(N/2 - 32\right)T_C + \pi/8\right\} \bmod 2\pi$$
$$y = \hat{f}_m * 64T_C$$

[0034] where N is the coherent accumulation length that is 512 chips for FLL and demodulation. The x term is approximately equal to a negative of half of the phase shift suffered by the received signal over the length of the segment. The "32" term is used to center the initial phase to the first sub-segment of length 64 chips. The additional $\pi/8$ term is used so that the hardware needs to truncate, rather than round off, the value of its state variable in order to determine the actual phase rotation. In the 8-bit scaling used to represent x, $\pi/8$ radians corresponds to the number 16.

[0035] The phase increment, y, represents the phase shift of the signal over a sub-segment (64-chip interval). The same phase parameters may be used for the demodulation of all RAKE receiver fingers, in a communications device, associated with a given user.

[0036] During a frequency search, the above expressions for x and y are modified slightly by replacing the frequency offset estimate, $\hat{f}_m$, from the FLL with the frequency hypothesis, f_H, and by setting N equal to the number of chips of coherent accumulation used to compute the search energies. This results in x and y being expressed as:

$$x = \left\{-f_H * \left(N/2 - 32\right)T_C + \pi/8\right\} \bmod 2\pi$$
$$y = f_H * 64T_C.$$

[0037] During a search for frequencies of mobile communication devices that are already being tracked, the search, in an alternate embodiment, may be restricted to the single frequency hypothesis. This is the frequency offset estimate that is closest to that estimated by the FLL for that particular mobile.

[0038] The hardware rotator (110) of the present invention maintains an 8-bit state variable whose value represents the phase angle at a high resolution of radians. In the preferred embodiment, this resolution is $\pi/128$ radians. During a demodulation or search dispatch, the DSP portion (102) of the present invention programs the hardware rotator (110) with a 16-bit word that contains the two 8-bit parameters, x and y.

[0039] Referring again to FIG. 1, the 16-bit programming word is generated by the combination (150) of x that has been left shifted 8 bits to truncate the 8-LSBs, and y. This combination is expressed as:

$z = (x << 8) | y$.

[0040] The higher significant byte of the 16-bit word contains the initial value of the state variable, which determines the phase of the rotator over the first sub-segment (64-chip interval). The lower significant byte of the 16-bit word contains the phase increment, which determines the amount by which the state variable is incremented from one sub-segment to the next. The phase accumulation is performed modulo 256, which corresponds to a full rotation of 2π radians. The actual phase rotation for a given sub-segment is obtained by truncating the 5 LSBs of the state variable, and multiplying the 3-bit result by $\pi/4$ radians.

[0041] During demodulation dispatches, the initial phase and phase increment are computed from an the estimated of the frequency offset provided by the FLL, and the length of the segment (N = 512 chips).

[0042] The x and y outputs of the FLL are input to the rotator portion (101) of the present invention. The rotator portion (101) is initialized by the initial phase (x) from the FLL. The phase increment (y) is input to a modulo 256 accumulator (140) that is updated at a 64-chip rate. Both the x and y inputs are 8 bits in width.

[0043] The output of the 8-bit accumulator (140) is input to a shift register (125) or other shifting device that shifts the accumulated signal by five places to the right. This generates a three remaining bit signal ($R=R_2R_1R_0$) that is input to the hardware rotator (110) of the present invention. These are the bits that are applied to the hardware rotator (110) that instruct the rotator to perform the phase rotation a predetermined amount. For example, in one embodiment, R = 001 ($R_2 = 0, R_1 = 0, R_0 = 1$) would instruct the rotator to rotate by $\pi/4$.

[0044] The hardware rotator (110) in the rotator portion (101) minimizes the coherence loss in the presence of large frequency offsets between the reverse link signal, received by the base station, and the local oscillator. This is achieved by phase shifting the signal by a (possibly)

different amount during each 64-chip sub-segment. In this way, the instantaneous phase of the signal remains close to the average phase of the signal over each segment.

[0045] The hardware rotator (110) applies phase shifts to the despread signal (112), $e^{j2\pi f_e T_c}$, at the chip rate, prior to pilot filtering and demodulation that is performed by the DSP portion (102). The angle of rotation, in the preferred embodiment, is a multiple of 45° and the angle is kept constant over each sub-segment (64 chips).

[0046] FIG. 2 illustrates a flowchart of a searcher process in accordance with the programmable rotator of the present invention. The process begins by centering the searcher on the expected frequency bins (step 201). The expected frequency bin is different for different applications and locations of base stations that incorporate the searcher of the present invention. For example, if the base station is located on a highway, the searcher may be centered on frequency bins +400 Hz and –400 Hz. If the base station is located on a railway, the frequency bins may be +1200 Hz and –1200 Hz, depending on the expected speeds of the trains.

[0047] The base station receives the pilot signal and decovers it (step 205). The decovering process is well known in the art and is not discussed further.

[0048] The FLL of the present invention then determines the phase error present in the signal (step 210). This error is determined after a 64-chip interval as described above. Alternate embodiments use other intervals of chip lengths.

[0049] The phase error is accumulated until it has reached a predetermined accumulated error (step 215). In the preferred embodiment, the predetermined accumulated error threshold is 45. For example, if after every 64-chip interval the error is 6°, this error is accumulated until the total error reaches 45°. If the accumulated error has reached the predetermined accumulated error threshold (step 220), the rotation is performed (step 225) as described above. If the threshold has not been reached (step 220), the process goes back to receiving and accumulating the phase errors (steps 205 – 220) until the threshold is reached.

[0050] After the rotation is performed (step 225), the accumulated phase error is reset to zero (step 230). The process then continues the tracking by returning to the receiving step (step 205) and repeating.

[0051] In an alternate embodiment, the same 8-PSK rotator can be used for both the FLL and the searcher. The rotator control in the searcher needs to be separated from the phase estimate output by the FLL. Instead, the value of the phase needs to be overwritten by the DSP and has to be interfaced to a higher layer of the software that implements the searcher process.

[0052] By supplying the phase increment, the DSP controls the point at which the rotator phase actually switches. The phase update is enabled every 64-chips.

[0053] The DSP of the preferred embodiment is limited to an 8-bit phase representation. Thus, the desired phase increments need to be quantized to be represented by an 8-bit integer number. This computation only concerns a 45° rotator since it is the preferred embodiment. The computations for a QPSK rotator would be different.

[0054] There is a tradeoff between optimal bin placement and hardware simplification and optimization. The general rule in choosing the phase rotator segment in chips, denoted as L, was minimizing the Mean loss function and Max loss function over the specified Doppler range. For a specified searcher mode (e.g., 3-Bin 45°), the L is a function of range. For example, L = 464 is optimal for the F_d=+/-400 Hz range, but L = 272 is optimal for the range of +/-800 Hz. The definition of range is arbitrary and does not have to be strict. One can assume that L = 448 will be an optimal L value for some range just above +/-400 Hz and well below +/-800 Hz.

[0055] Using this approach, we can derive phase increment values to generate a value close to an appropriate L. The procedure for computing integer Phase increment (θ) is expressed as:

$$(L/64)_\theta = 256/8,$$

[0056] where 256 is the 8-bit representation of a full 360° phase, and 256/8 is the representation of 45°. Thus, $\theta = 256*8/L$ can be used to compute θ increments for the DSP. FIG. 3 illustrates the phase increments in LSBs and the corresponding L, in PN chips, using this alternate embodiment approach.

[0057] In the embodiment where the FLL and searcher share the rotator design, the knowledge of frequency can be shared between these two blocks. During the initial acquisition, if the searcher signal is found in one of the frequency bins, this bin center can be used to initialize the FLL. Similarly, when performing set maintenance searches, the searcher can be programmed to search only one frequency bin corresponding to the offset value in the FLL accumulator.

[0058] FIG. 4 illustrates a plot of the probability of pilot signal detection versus the frequency deviation of the pilot signal. This plot shows a comparison between the probability of detecting the pilot signal using a searcher without a rotator and a searcher using the programmable rotator of the present invention.

[0059] Both plots assume that EcNt = -18dB, number of chips (Nc) = 1024, and the number of non-coherent accumulations (Nn) = 6. Additionally, the rotator used in the plot is a 2-bin, 45° rotator.

[0060] Referring to FIG. 4, it can be seen that the probability of a searcher without a rotator (401) detecting the pilot is substantially less than a searcher with the rotator (402) of the present invention. This is especially true when the pilot is experiencing a $\pm$400 Hz or more of a Doppler shift.

[0061] FIG. 5 illustrates a block diagram of a base station incorporating the searcher of the present invention. The base station is comprised of a transmitter (501) that modulates and transmits signals over an air channel using the antenna (502). The transmitter gets its signals to be modulated and transmitted from the network that is coupled to the base station. This network can be a cellular infrastructure network, the public switched telephone network, or any other network requiring connection to a wireless base station.

[0062] The antenna (502) also receives signals from mobile communication devices. These signals are coupled to the receiver (505) of the base station for demodulation and transmission to the network. The receiver (505) comprises the searcher incorporating the FLL and programmable rotator of the present invention.

[0063] The base station is further comprised of a base station controller (510). The controller (510) is responsible for control of the base station's transmitter, receiver, and other components not shown but are well known in the art.

[0064] In summary, the searcher of the present invention can specify an arbitrary number of frequency bins and perform frequency as well as code space searching. By using a programmable rotator, the searcher is able to find and track a signal that has a large frequency error, such as those experiencing a Doppler effect caused by movement away from and towards the base station.

WE CLAIM:

CLAIMS

1. A searcher method for finding a signal having a frequency deviation from an expected frequency, the method comprising the steps of:

initialising the searcher on predetermined frequency bins;

determining a phase error in the signal;

generating a phase increment in response to the phase error;

accumulating the phase increments to generate a total phase increment; and

when the total phase increment has reached a predetermined total phase increment threshold, performing a phase rotation function that is substantially equivalent to the total phase increment.

2. The method of claim 1, and further including the step of resetting the accumulated phase increments after performing the phase rotation function.

3. The method of claim 1, wherein the phase rotation function is a Quadrature Phase Shift Keying function.

4. The method of claim 1, wherein the phase rotation function is an 8-Phase Shift Keying function.

5. The method of claim 1, wherein the total phase increment threshold is substantially equivalent to $\pi/4$ radians.

6. The method of claim 1, wherein the total phase increment threshold is substantially equivalent to $\pi/2$ radians.

7. A wireless communication device for finding a signal having a frequency deviation from an expected frequency, the device comprising:

means for initialising the searcher on predetermined frequency bins;

means for determining a phase error in the signal;

means for generating a phase increment in response to the phase error;

means for accumulating the phase increments to generate a total phase increment; and

means for performing a phase rotation function that is substantially equivalent to the total phase increment when the total phase increment has reached a predetermined total phase increment threshold.

8. The device of claim 7, further comprising means for resetting the accumulated phase increments after performing the phase rotation function.

9. The device of claim 7, wherein the phase rotation function is a Quadrature Phase Shift Keying function.

10. The device of claim 7, wherein the phase rotation function is an 8-Phase Shift Keying function.

11. The device of claim 7, wherein the total phase increment threshold is substantially equivalent to $\pi/4$ radians.

12. The device of claim 7, wherein the total phase increment threshold is substantially equivalent to $\pi/2$ radians.