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CMOS INVERTERS CONFIGURED USING MULTIPLE-GATE TRANSISTORS

Field of the Invention

0001 The present invention generally relates to the field of silicon-on-insulator (SOI) circuits, and more particularly, to an inverter formed of multiple-gate metal oxide semiconductor field effect transistors (MOSFETs).

Background of the Invention

0002 The dominant semiconductor technology used for the manufacture of ultra-large scale integrated (ULSI) circuits is the metal-oxide-semiconductor field effect transistor (MOSFET) technology. Reduction in the size of MOSFETs has provided continued improvement in speed performance, circuit density, and cost per unit function over the past few decades. As the gate length of the conventional bulk MOSFET is reduced, the source and drain increasingly interact with the channel and gain influence on the channel potential. Consequently, a transistor with a short gate length suffers from problems related to the inability of the gate to substantially control the on and off states of the channel. Phenomena such as reduced gate control associated with transistors

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with short channel lengths are termed short-channel effects. Increased body doping concentration, reduced gate oxide thickness, and ultra-shallow source/drain (S/D) junctions are ways to suppress short-channel effects. However, for device scaling well into the sub-50 nm regime, the requirements for body-doping concentration, gate oxide thickness, and source/drain doping profiles become increasingly difficult to meet when conventional device structures, based on bulk silicon (Si) substrates, are employed. Innovations in front-end process technologies or the introduction of alternative device structures are required to sustain the historical pace of device scaling.

0003 For device scaling well into the sub-30 nm regime, a promising approach to controlling short-channel effects is to use an alternative device structure with multiple-gate electrodes. Examples of multiple-gate structures include the double-gate structure, triple-gate structure, omega-FET structure, and the surround-gate or wrap-around gate structure. A multiple-gate transistor structure is expected to extend the scalability of CMOS technology beyond the limitations of the conventional bulk MOSFET and realize the ultimate limit of silicon MOSFETs. The introduction of additional gates improves the capacitance coupling

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between the gates and the channel, increases the control of the channel potential by the gate, helps suppress short channel effects, and prolongs the scalability of the MOS transistor.

0004 A simple example of a multiple-gate device is the double-gate MOSFET structure, where there are two gate electrodes on the opposing sides of the channel or silicon body. A one way to fabricate a double-gate MOSFET is described by U.S. Patent No. 6,413,802B1, issued to Hu et al, for FinFET transistor structures having a double gate channel extending vertically from a substrate and methods of manufacture. In U.S. Patent No. 6,413,802B1, the device channel comprises a thin silicon fin formed on an insulative substrate (e.g. silicon oxide) and defined by using an etchant mask. Gate oxidation is performed, followed by gate deposition and gate patterning to form a double-gate structure overlying the sides of the fin. Both the source-to-drain direction and the gate-to-gate direction are in the plane of the substrate surface. The specific device structure, the cross-section of which is illustrated in Figure 1A, is widely recognized to be one of the most manufacturable double-gate structures. A plane view of the double-gate structure 10 is shown in Figure 1B. The etchant mask 12 of U.S. Patent No. 6,413,802B1 is retained on the fin 20 in the

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channel region through the process. The device width of a single fin is defined to be twice the fin height h . Multiple device widths may be achieved on the same substrate 14 by placing multiple fins 22,24 in parallel, as illustrated in device 30 in Figure 2. An inverter circuit may be formed using N-channel and P-channel MOSFETs comprising such multiple fins. In another embodiment of U.S. Patent No. 6,413,802B1, an inverter circuit 40 is implemented using N-channel and P-channel MOSFETs 42,44 that are vertically aligned and separated by a dielectric layer 46, as illustrated in Figure 3.

0005 Another example of the multiple-gate transistor is the triple-gate transistor 50. The cross-section of the triple-gate transistor structure 50 is illustrated in Figure 4A. The plane view of the triple-gate structure 50 is shown in Figure 4C. The triple-gate transistor structure 50 has three gates: one gate on the top surface 52 of the silicone body/fin, and two gates on the sidewalls 54,56 of the silicon body/fin. The triple-gate device achieves better gate control than the double-gate device because it has one more gate on the top surface 52 of the silicon fin.

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0006 While there is some work on the design and fabrication of multiple-gate devices such as the double-gate and triple-gate devices, there is little work on circuits, such as inverter circuits, configured using such devices. The relentless pursuit of high-performance has pushed logic and circuit designers to utilize every delay and area optimization technique at their disposal. However, the optimization of circuits, such as inverter circuits, incorporating multiple-gate transistors has not been addressed. Traditionally, in logic synthesis, delay optimization techniques have heavily relied on gate sizing algorithms which vary drive strengths of gates to optimize circuit delay. Since the delay in CMOS logic circuits not only depends on the drive strengths of each stage, but also on the width ratio of the P-channel and N-channel devices (P/N width ratio), it is crucial to make available a simple method to provide optimal P/N width ratios for inverters incorporating multiple-gate transistors.

0007 Referring back to Figures 1A and 1B, a double-gate MOSFET structure 10 is shown. Figure 1A shows the cross-sectional view of the double-gate MOSFET 10 through its channel region where the semiconductor fin 20 forms the channel and a gate electrode 16 straddles over the semiconductor fin 20, forming two gates 26,28,

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one on each of the two sidewalls 36,38 of the semiconductor fin 20. The plane view of the double-gate MOSFET structure 10 is shown in Figure 1B. The width of a double-gate MOSFET formed using a single semiconductor fin is two times the fin height h , that is, the width of the double-gate MOSFET is equal to $2h$. Varying the fin width for the double-gate MOSFET has no effect on the device width. Multiple device widths may be achieved on the same substrate by placing multiple fins in parallel. Figure 2A shows the cross-sectional view of two double-gate MOSFETs connected in parallel. The width of the resulting parallel connection of two double-gate MOSFETs $4h$.

0008 Figure 4A shows the cross-sectional view of a triple-gate transistor 50 through the channel region. The triple-gate transistor is similar to the double-gate transistor except for the absence of the mask on the top surface 52 of the semiconductor fin 20. The gate dielectric 58 wraps around the semiconductor fin 20 on three sides, and the gate electrode 48 straddles over the fin 20. The gate electrode 48 forms three gates: a gate 62 on the top surface 52 of the semiconductor fin 20 and a gate 64,66 on each of the two sidewalls 54,56 of the fin. The device width of the triple-gate MOSFET 50 is given by the sum of the fin width and

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twice the fin height, e.g. $(2h + w)$. Note that in this device structure, a variation of the fin width w changes the device width. The value of fin width w may be varied by altering the layout as schematically illustrated in Figure 4C. A three-dimensional perspective of the triple-gate MOSFET 50 is shown in Figure 5A.

0009 Triple-gate transistors may have a recessed insulator layer for improved gate control, as illustrated in Figure 4B. Such a structure is also known as the Omega field-effect transistor (FET), or simply omega-FET, since the gate electrode has an omega-shape in its cross-sectional view. The encroachment of the gate electrode under the semiconductor fin or body forms an omega-shaped gate structure. It closely resembles the gate-all-around (GAA) transistors for excellent scalability, and uses a manufacturable process similar to that of the double-gate or triple-gate transistor. The omega-FET has a top gate 62, two sidewall gates 64, 66, and special gate extensions or encroachments 68 under the semiconductor body. The omega-FET is therefore a field effect transistor with a gate that almost wraps around the body. In fact, the longer the gate extension, e.g. the greater the extent of the encroachment E , the more the structure approaches or resembles the gate-all-around structure. A three-dimensional perspective of the

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triple-gate transistor 50 with recessed insulator, or omega-FET, is schematically illustrated in Figures 5B. The encroachment of the gate electrode 48 under the silicon body helps to shield the channel from electric field lines from the drain and improves gate-to-channel controllability, thus alleviating the drain-induced barrier lowering effect and improving short-channel performance. The encroachment 68 of the gate electrode under the silicon body relies on an undercut 88 of the insulator layer 18 on the substrate 14, thus forming an undercut 88 in the substrate 14 at the base of the silicon body. It should be noted that the device width of the omega-FET is given by the sum of the fin width w , twice the fin height h , and twice the encroachment E . Therefore, the device width is given by $(w + 2h + 2E)$. A variation of the fin width for the omega-FET changes the device width.

0010 The plane view showing the triple-gate transistor of Figure 4A, or the omega-FET of Figure 4B, is shown in Figure 4C. Both cross-sections in Figures 4A and 4B are drawn along line A-A'.

0011 It is therefore an object of the present invention to provide an inverter formed of multiple-gate metal oxide semiconductor field effect transistors.

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0012 It is another object of the present invention to provide a method for fabricating an inverter by multiple-gate metal oxide semiconductor field effect transistors.

Summary of the Invention

0013 In accordance with the present invention, an inverter formed of multiple-gate metal oxide semiconductor field effect transistors and a method for such fabrication are provided.

0014 In a preferred embodiment, an inverter is provided which includes a first multiple-gate transistor including a source connected to a power supply, a drain connected to an output terminal and a gate electrode; a second multiple-gate transistor including a source connected to a ground, a drain connected to the output terminal, and a gate electrode; and an input terminal connected to the gate electrodes of the first and second multiple-gate transistors.

0015 In the present invention inverter, the first and second multiple-gate transistors may be triple-gate transistors, or may be omega field-effect transistors. Each of the first and second multiple-gate transistors may further include a substrate that has

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an insulating layer on top and source, drain regions formed therein; a semiconductor fin formed vertically on the substrate, the semiconductor fin has two fin sidewalls and a fin top; a gate dielectric layer overlying the semiconductor fin; and a gate electrode that wraps around the semiconductor fin separating the source and drain regions. The semiconductor fin may be formed of silicon, or may be formed of silicon and germanium. The semiconductor fin may have a non-uniform fin width. A first semiconductor fin width for the first multiple-gate transistor may be different from a second semiconductor fin width for the second multiple-gate transistor. The first multiple-gate transistor and the second multiple-gate transistor may be formed on the same semiconductor fin, or may be formed on different semiconductor fins.

0016 In the present invention inverter, the insulating layer includes a dielectric material, or includes silicon oxide. The insulating layer may have a thickness between 20 Angstroms and 1000 Angstroms. The gate dielectric layer may include silicon oxide, or may include silicon oxynitride, or may include a high permittivity material selected from the group consisting of La_2O_3 , Al_2O_3 , HfO_2 , HfON and ZrO_2 . The gate dielectric layer may be formed of a high

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permittivity material that has a relative permittivity of at least 5. The gate dielectric layer may have a thickness between 3 Angstroms and 100 Angstroms, or may have a thickness on the fin sidewall different than a thickness on the fin top, or may have a thickness on the fin top smaller than a gate dielectric thickness on the fin sidewall, or may have a thickness on the fin top of the semiconductor fin less than 20 Angstroms. The gate electrode may be formed of poly-crystalline silicon, or may be formed of polycrystalline silicon germanium, or may be formed of a metal. The source and drain regions of the first and second multiple-gate transistors may be strapped by a conductive material selected from the group consisting of metals and silicides. An electrical contact between the conductive material and the source and drain regions may be made on at least one of the fin sidewalls and fin top of the semiconductor fin.

0017 The present invention is further directed to an inverter that includes a first plurality of P-channel multiple-gate transistors each including a source connected to a power supply, a drain connected to an output terminal, and a gate electrode; a second plurality of N-channel multiple-gate transistors each including a source connected to ground, a drain connected to the

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output terminal, and a gate electrode; and an input terminal connected to the gate electrodes of the first plurality of P-channel and the second plurality of N-channel multiple-gate transistors.

0018 In the present invention inverter, the first plurality of P-channel and the second plurality of N-channel multiple-gate transistors may be triple-gate transistors, or may be omega field-effect transistors. Each of the first plurality of P-channel and the second plurality of N-channel multiple-gate transistors may include a substrate that has an insulating layer formed on a top surface; source and drain regions formed in the substrate; a semiconductor fin vertically formed on the insulating layer, the fin has a fin top and two fin sidewalls; a gate dielectric layer overlying the semiconductor fin; and a gate electrode wrapping around the semiconductor fin separating the source and drain regions. The semiconductor fin may include silicon, or may include silicon and germanium. The semiconductor fin may have a non-uniform fin width. A first fin width for the first plurality of P-channel multiple-gate transistors may be different from a second fin width for the second plurality of N-channel multiple-gate transistors. The first plurality of P-channel multiple-gate

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transistors and the second plurality of N-channel multiple-gate transistors may be formed on the same semiconductor fin, or may be formed on different semiconductor fins.

0019 In the present invention inverter, the insulating layer may include a dielectric material, or may include a silicon oxide. The insulating layer may have a thickness between 20 Angstroms and 1000 Angstroms. The gate dielectric layer may include silicon oxide, or may include silicon oxynitride, or may include a high permittivity material selected from the group consisting of La_2O_3 , Al_2O_3 , HfO_2 , HfON and ZrO_2 . The gate dielectric layer may include a high permittivity material that has a relative permittivity of at least 5. The gate dielectric layer may have a thickness between 3 Angstroms and 100 Angstroms, or may have a different thickness on the fin sidewall than on the fin top, or may have a smaller thickness on the fin top than on the fin sidewall, or may have a thickness on the fin top of less than 20 Angstroms. The gate electrode may include poly-crystalline silicon, or poly-crystalline silicon germanium, or a metal. The source and drain regions may be strapped by a conductive material selected from the group consisting of metals and silicides. An electrical contact between the conductive material and the source and drain regions may be

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made on at least one of the fin sidewalls and fin top of the semiconductor fin.

0020 The present invention is still further directed to a method for fabricating an inverter by multiple-gate transistors which can be carried out by the operating steps of providing a substrate that includes a semi-conducting layer overlying an insulating layer; forming a semiconductor fin in the semi-conducting layer, the fin has two sidewalls and a top; depositing a layer of a dielectric material overlying the semiconductor fin; depositing a layer of a conductive material overlying the layer of dielectric material; patterning the layer of conductive material forming gate electrode straddling across the two sidewalls and the top of the semiconductor fin; and forming a source and a drain region in the semiconducting layer.

0021 In the method for fabricating an inverter by multiple-gate transistors, the semi-conducting layer may include silicon, or may include silicon and germanium. The insulating layer may include silicon oxide. The semiconductor fin forming process may further include a fin surface smoothing step. The surface smoothing step may further include sacrificial oxidation and high

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temperature annealing in a hydrogen ambient. The dielectric material layer may include silicon oxide, or may include silicon oxynitride, or may include a high permittivity material of La_2O_3 , Al_2O_3 , HfO_2 , HfON or ZrO_2 . The high permittivity material may have a relative permittivity of at least 5. The dielectric material layer may have a thickness between 3 Angstroms and 100 Angstroms, or may have a thickness on the fin sidewalls different than a thickness on the fin top, or may have a smaller thickness on the fin top compared to a thickness on the fin sidewall, or may have a thickness on the fin top of less than 20 Angstroms. The dielectric material may include poly-crystalline silicon, or poly-crystalline silicon germanium. The conductive material layer may be formed on the source region and the drain region. The conductive material layer may be selected from the group consisting of metals, metallic silicides and metallic nitrides.

Brief Description of the Drawings

0022 These and other objects, features and advantages of the present invention will become apparent from the following detailed description and the appended drawings in which:

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0023 Figures 1A and 1B are enlarged, cross-sectional view and plane view, respectively, for a conventional double-gate device structure.

0024 Figures 2A and 2B are enlarged, cross-sectional view and plane view, respectively, for two double-gate devices connected in parallel.

0025 Figure 3 is an enlarged, perspective view of a conventional CMOS inverter utilizing stacked P-channel and N-channel MOSFETs.

0026 Figures 4A, 4B and 4C are enlarged, cross-sectional views and plane view, respectively, for a triple-gate device structure with recessed insulator.

0027 Figures 5A and 5B are enlarged, perspective views for a present invention triple-gate transistor without and with recessed insulator, respectively.

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0028 Figure 6 is an enlarged, perspective view of a present invention CMOS inverter formed by triple-gate N-channel and P-channel MOSFETs.

0029 Figure 7 is a layout diagram for the present invention CMOS inverter of Figure 6.

0030 Figure 8 is a schematic representation for a present invention inverter configured using multiple-gate transistors.

0031 Figures 9A and 9B are layout diagrams for a present invention CMOS inverter including triple-gate N-channel and P-channel MOSFETs with multiple fins.

0032 Figure 10 is a layout diagram for a present invention CMOS inverter, in an alternate embodiment, formed by triple-gate N-channel and P-channel MOSFETs with multiple fins.

0033 Figures 11A, 11B, 11C and 11D are enlarged, cross-sectional views illustrating the present invention process flow for the formation of a triple-gate transistor.

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0034 Figures 12A and 12B are enlarged, cross-sectional views illustrating the present invention process flow for the formation of omega-FET.

0035 Figure 13 is an enlarged, plane view of a completed present invention triple-gate transistor or omega-FET.

Detailed Description of the Preferred and Alternate Embodiments

0036 In accordance with the present invention, an inverter circuit may be formed using N-channel and P-channel MOSFETs comprising of a single fin or multiple fins. An inverter circuit comprises a complementary pair of transistors. The complementary pair includes a P-channel transistor and an N-channel transistor. The ratio of the width of the P-channel MOSFET to the width of the N-channel MOSFET is termed the P/N width ratio. It is advantageous to have the freedom of selecting an appropriate P/N width ratio to optimize circuit performance or circuit delay time. It should be noted that the double-gate MOSFET as shown in Figures 1 and 2 are not able to offer a continuous range of P/N width ratio if the P-channel and the N-channel MOSFETs have the same fin height, or are formed from the same semiconductor film. If two fins are used for

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the P-channel MOSFET and one fin is used for the N-channel MOSFET in an inverter circuit, the P/N width ratio is 2. If three fins are used for the P-channel MOSFET and two fins are used for the N-channel MOSFET in an inverter circuit, the P/N width ratio is $3/2$ or 1.5. The P/N width ratio must be a number given by a quotient of two integers. It cannot be continuously varied. It is not straightforward to realize a P/N width ratio of 1.35 using the double-gate MOSFET as shown in Figures 1 and 2.

0037 One way to vary the P/N ratio of the double-gate MOSFET continuously is to use a stacked structure comprising of P-channel and N-channel MOSFETs vertically aligned and separated by a dielectric layer, as shown in Figure 3. This structure is described in U.S. Patent No. 6,413,802B1. The PMOS layer has a thickness t_{PMOS} and the NMOS layer has a thickness t_{NMOS} . The ratio of the thickness of the PMOS layer to the NMOS layer, e.g. t_{PMOS}/t_{NMOS} , is the P/N width ratio and may be varied over a wide range. The stacked structure, as shown in Figure 3, is not easily fabricated. It requires the formation of a crystalline PMOS layer overlying the dielectric layer, by methods such as solid phase epitaxy and lateral epitaxial overgrowth, which are expensive and have low throughput.

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0038 In the present invention, the problems of prior art are solved by configuring an inverter circuit using multiple-gate transistors with a gate on the top surface of the semiconductor fin. Multiple-gate transistors with a gate on the top surface of the semiconductor fin include the triple-gate MOSFET and the omega-FET.

0039 An inverter circuit incorporating multiple-gate transistors such as triple-gate MOSFET and omega-FET is provided in the present invention. In one embodiment of the present invention, the inverter circuit is provided with the triple-gate transistors of Figure 4A. In another embodiment, the inverter circuit is provided with triple-gate transistors with a recessed insulator layer, also known as omega-FETs, of Figure 4B. An illustration of the inverter structure 70 incorporating triple-gate transistors 72,74 are shown in Figure 6. In Figure 6, the inverter structure 70 is comprised of a single semiconductor fin 76. The semiconductor fin 76 constitutes the inverter which may have a non-uniform width. The fin width is w_{NMOS} in the portion where an N-channel MOSFET 74 is formed and w_{PMOS} in the portion where a P-channel MOSFET 72 is formed. The fin height is h for both N-channel and P-channel MOSFETs 72,74 in the preferred embodiment.

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Nevertheless, the fin height does not have to be uniform, and can be different in different regions of the semiconductor 76. In the preferred embodiment, the semiconductor fin 76 is comprised of silicon. In general, the semiconductor fin 76 may be comprised of any elemental semiconductor such as germanium, any alloy semiconductor such as silicon-germanium, or any compound semiconductor such as indium phosphide and gallium arsenide.

0040 The inverter structure 70 of Figure 6 is formed from a complementary pair of transistors, an N-channel triple-gate transistor 74 comprising N-type source and drain regions 84,86 separated by a gate electrode 78, and a P-channel triple-gate transistor 72 comprising P-type source and drain regions 92,94 separated by a gate electrode 82. In the preferred embodiment, the gate electrode 78,82 is poly-crystalline silicon (poly-Si) and is doped N-type in the N-channel MOSFET 74 and doped P-type in the P-channel MOSFET 72. In general, the gate electrodes 78,82 may be comprised of a material such as poly-crystalline silicon (poly-Si), poly-crystalline silicon-germanium (poly-SiGe), a refractory metal such as molybdenum and tungsten, compounds such as titanium nitride, or other conducting materials.

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0041 The layout of the inverter structure 70 of Figure 6 is shown in Figure 7. The gate electrodes 78,82 of the N-channel multiple-gate transistor 74 and the P-channel multiple-gate transistor 96 are connected together. The inverter also includes a gate contact 96. The gate contact 96 connects the gate electrode to a metal line 98, which provides an input to the inverter. Further, the inverter includes an electrical contact between the drain regions 86,94 of the N-channel and P-channel multiple-gate transistors 74,72 to provide an output for the inverter 70. The source 84 of the N-channel multiple-gate transistor 74 is connected to ground 100, and the source 92 of the P-channel multiple-gate transistor 72 is connected to the power supply 102. The circuit diagram for the inverter structure 70 of Figure 6 is shown in Figure 8.

0042 According to another embodiment of the invention, an inverter may also be configured using multiple semiconductor fins with non-uniform widths. An inverter 110, comprising two semiconductor fins 112,114 with non-uniform widths is illustrated in Figure 9A. The first semiconductor fin 114 comprises two regions 116,118, one region 116 where a first N-channel multiple-gate transistor is formed, and another region 118 where a first P-

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channel multiple-gate transistor is formed. The second semiconductor fin 112 comprises two regions 120,122, one region 120 where a second N-channel multiple-gate transistor is formed, and another region 122 where a second P-channel multiple-gate transistor is formed. In general, the fin widths w_{NMOS1} , w_{NMOS2} , w_{PMOS1} , and w_{PMOS2} are not the same. The drain regions of all the transistors 116, 118, 120, 122 in Figure 9 are connected to the output terminal 124. The electrodes 128,130 of the N-channel and P-channel transistors are connected to the input terminal. The source regions of the P-channel transistors are connected to the power supply 132, and the source regions of the N-channel transistors are connected to ground 134.

0043 The N-type metal-oxide semiconductor (NMOS) and P-type metal-oxide-semiconductor (PMOS) devices need not be on the same semiconductor fin. In Figure 10, structure 150 of yet another embodiment of the invention where the N-channel multiple-gate transistor and the P-channel multiple-gate transistor are formed using different semiconductor fins 152,154 with different fin widths.

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0044 The preceding explanation details the structural description of the inverter configured using multiple-gate transistors. Various variations of this invention may be implemented. As an illustration, semiconductor fin with non-uniform width may comprise of a plurality of multiple-gate transistors of the same type, e.g. two P-channel transistors.

0045 A method for the formation of the present invention structure is now described by a process flow for fabricating a triple-gate transistor or an omega-FET.

0046 The fabrication process for the triple-gate transistor, the preferred embodiment of his invention, is schematically described in Figures 11A-11D. Figures 11A-11D show the device cross-sections at the various process steps, as observed along line A-A' of the plane view of the completed device 170 shown in Figure 13. The starting substrate 14 is a silicon-on-insulator substrate, as shown in Figure 11A. The starting substrate comprises a silicon film 32 overlying an insulator layer 18. The insulator layer 18 has a thickness of between 20 Angstroms and 1000 Angstroms. The

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first insulator layer 18 can be made of any dielectric material such as silicon oxide. In the preferred embodiment, the first dielectric material is silicon oxide.

0047 The silicon fins 20 are patterned using an etchant mask 12, as shown in Figure 11B. The etchant mask may comprise a material commonly used for masking an etch process, such as photoresist, silicon oxide, silicon nitride, etc. In the preferred embodiment, the etchant mask is silicon oxide. In the present invention, an optional fin surface smoothing step is used to improve or reduce the surface roughness of the fin sidewalls 36,38. If the etchant mask used for fin definition is silicon oxide, as in the preferred embodiment, it may be removed before or after the fin smoothing process. The removal of the etchant mask 12 on the silicon fin 20 prior to gate dielectric formation allows the device to have a triple-gate structure since the gate electrode 16 will finally be formed on each of the two sidewalls 36,38 as well as the top surface of the fin, as shown in Figure 11C. If the etchant mask 12 used for fin definition is a photoresist, it has to be removed before the fin surface smoothing step to avoid the high temperatures used in the fin smoothing process. The fin surface smoothing is performed by subjecting the fin 20 to a sacrificial

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oxidation and/or silicon sidewall treatment (e.g. high temperature anneal at 1000°C in H₂ ambient). The surface smoothing of the fin sidewalls contributes to the achievement of good carrier mobilities. Depending on whether the silicon oxide etchant mask is removed prior to the fin smoothing process step, the shape of the fin may be square-like or rounded at the top. If the etchant mask may be retained on the fin throughout the process, the final device structure will be a double-gate device structure.

0048 The process is followed by gate dielectric formation. The gate dielectric may be formed by thermal oxidation, chemical vapor deposition, sputtering, etc. In general, the thickness of the gate dielectric may be different on the sidewall of the fin and on the top of the fin. Depending on the technique of gate dielectric formation, the gate dielectric thickness on the top of the fin may be thinner than the thickness on the fin sidewall. In one embodiment, the gate dielectric thickness on the top surface of the fin is less than 20 Angstroms. The gate dielectric may comprise a conventional material such as silicon dioxide or silicon oxynitride with a thickness ranging from 3 Angstroms to 100 Angstroms, and more preferably, from about 10 Angstroms or less. The gate dielectric may also comprise high permittivity (high-k)

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materials such as lanthalam oxide (La_2O_3), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), hafnium oxynitride (HfON), or zirconium oxide (ZrO_2), with an equivalent oxide thickness of 3 Angstroms to 100 Angstroms.

0049 In the next step, the gate material is deposited. The gate material may be polycrystalline-silicon (poly-Si), polycrystalline silicon-germanium (poly-SiGe), a refractory metal such as molybdenum and tungsten, compounds such as titanium nitride, or other conducting materials. A gate mask is defined and the underlying gate material is etched to form the gate electrode. The gate etch stops on the gate dielectric, and the gate is electrically isolated from the transistor structure by the gate dielectric. In the preferred embodiment, the gate material is poly-Si and the gate dielectric is silicon oxynitride. A plasma etch using chlorine and bromine chemistry may be used to achieve a high etch selectivity. A high etch selectivity is critical for device structures with a tall fin and aggressively scaled gate dielectric thickness.

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0050 After the definition of the gate, the gate mask can be removed. At this stage of the device fabrication, the three-dimensional perspective of the device is similar to that shown in Figure 5 (spacers and source/drain extensions are not shown). The lightly-doped drain (LDD) or drain extension is formed next. This may be achieved by ion implantation, plasma immersion ion implantation (PIII), or other techniques known and used in the art. Next, a spacer is formed on the sidewalls of the gate by techniques known and used in the art, e.g. deposition and selective etching of the spacer material. The spacer material may be comprised of a dielectric material such as silicon nitride or silicon dioxide. In the preferred embodiment, the spacer comprises a silicon nitride and an oxide composite spacer. After spacer formation, source and drain regions are doped by ion implantation, PIII, gas or solid source diffusion, or any other techniques known and used in the art. Any implant damage or amorphization can be annealed through subsequent exposure to elevated temperatures. The resistance of the source, drain, and gate can also be reduced by strapping the source, drain, and gate with a conductive material. The conductive material may be a metallic silicide such as titanium silicide, cobalt silicide or nickel silicide, a metallic nitride such as titanium nitride and tantalum nitride, a metal such as tungsten and

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copper, or a heavily doped semiconductor such as n+ doped Si. In the preferred embodiment, the conductive material is nickel silicide which may be formed by a self-aligned silicide (salicide) process. In the source and drain regions, the conductive material may be formed on both the top of the fin as well as on the sidewall of the fin.

0051 Contacts are then formed to the source, drain, and gate regions using techniques known and used in the art. It is important to achieve a very low contact resistance in nanoscale devices. This completes the fabrication of the triple-gate transistor.

0052 The fabrication process for the omega-FET is similar to that of the triple-gate transistor. The fabrication of the omega-FET adopts the same process as the triple-gate transistor up to the fin formation step, as shown in Figure 11C. Following Figure 11C, a recess in the insulator layer is formed and generally involves an etch process. Figures 12A and 12B show the cross-sections of the device after the recess is formed. An example of an etch process is a wet etch using dilute hydrofluoric acid (HF) (formed by a mixture of 25 parts water and 1 part concentrated HF) for 30 - 600

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seconds at 25°C to etch about 50 - 1000 Angstroms of thermally grown silicon oxide. In the preferred embodiment, the recess R is between 20 Angstroms and 500 Angstroms. After the formation of the recess, subsequent processes such as gate dielectric formation, gate electrode formation, and contact formation are exactly the same as that described for the triple-gate transistor.

0053 While the present invention has been described in an illustrative manner, it should be understood that the terminology used is intended to be in a nature of words of description rather than of limitation.

0054 Furthermore, while the present invention has been described in terms of a preferred and alternate embodiments, it is to be appreciated that those skilled in the art will readily apply these teachings to other possible variations of the inventions.

0055 The embodiment of the invention in which an exclusive property or privilege is claimed are defined as follows.

CLAIMS

1. An inverter comprising:

a first multiple-gate transistor comprises a source connected to a power supply, a drain connected to an output terminal, a semiconductor fin, and a gate electrode wrapping around said semiconductor fin and separating said source and drain;

a second multiple-gate transistor comprises another source connected to a ground, another drain connected to said output terminal, and another gate electrode wrapping around said semiconductor fin and separating said another source and another drain, wherein said first and second multiple-gate transistors are triple-gate transistors, and a width of said semiconductor fin at said first multiple-gate transistor is different from a width of said semiconductor fin at said second multiple-gate transistor; and

an input terminal connected to said gate electrodes of said first and second multiple-gate transistors.

2. The inverter of claim 1, wherein said first and second multiple-gate transistors are omega field-effect transistors.

3. The inverter of claim 1 or 2, wherein each of said first and second multiple-gate transistors further comprises:

a substrate having an insulating layer on top; and

a gate dielectric layer overlying said semiconductor fin;

wherein said semiconductor fin is formed vertically on said substrate, and said semiconductor fin has two fin sidewalls and a fin top.

4. The inverter of any one of the preceding claims, wherein said semiconductor fin comprises silicon.

5. The inverter of any one of the preceding claims, wherein said semiconductor fin comprises silicon and germanium.
6. The inverter of claim 3, wherein said first multiple-gate transistor and said second multiple-gate transistor are formed on different semiconductor fins.
7. The inverter of any one of the preceding claims, wherein said first multi-gate transistor and said second multi-gate transistor are formed on different numbers of semiconductor fins.
8. The inverter of any one of claims 3-7, wherein said insulating layer comprises a dielectric.
9. The inverter of any one of claims 3-8, wherein said insulating layer comprises silicon oxide.
10. The inverter of any one of claims 3-9, wherein said insulating layer has a thickness between 20 Angstroms and 1000 Angstroms.
11. The inverter of any one of claims 3-10, wherein said gate dielectric layer comprises silicon oxide.
12. The inverter of any one of claims 3-11, wherein said gate dielectric layer comprises silicon oxynitride.
13. The inverter of any one of claims 3-12, wherein said gate dielectric layer comprises a high permittivity material selected from the group consisting of La_2O_3 , Al_2O_3 , HfO_2 , HfON and ZrO_2 .

14. The inverter of any one of claims 3-13, wherein said gate dielectric layer comprises a high permittivity material having a relative permittivity of at least 5.
15. The inverter of any one of claims 3-14, wherein said gate dielectric layer having a thickness between 3 Angstroms and 100 Angstroms.
16. The inverter of any one of claims 3-15, wherein said gate dielectric layer having a thickness on said fin sidewall different than a thickness on said fin top.
17. The inverter of any one of claims 3-16, wherein said gate dielectric layer having a thickness on said fin top smaller than a gate dielectric thickness on said fin sidewall.
18. The inverter of any one of claims 3-17, wherein said gate dielectric layer having a thickness on said fin top of the semiconductor fin less than 20 Angstroms.
19. The inverter of any one of the preceding claims, wherein said gate electrode comprises poly-crystalline silicon.
20. The inverter of any one of the preceding claims, wherein said gate electrode comprises poly-crystalline silicon germanium.
21. The inverter of any one of the preceding claims, wherein said gate electrode comprises a metal.
22. The inverter of any one of the preceding claims, wherein said source and drain regions are strapped by a conductive material selected from the group consisting of metals and silicides.

23. The inverter of claim 2322, wherein electrical contact between said conductive material and said source and drain regions are made on at least one of the fin sidewalls and fin top of the semiconductor fin.

24. An inverter comprising:

a first plurality of P-channel multiple-gate transistors, each comprises a source connected to a power supply, a drain connected to an output terminal, a semiconductor fin, and a gate electrode wrapping around said semiconductor fin and separating said source and drain;

a second plurality of N-channel multiple-gate transistors, each comprises another source connected to ground, another drain connected to said output terminal, and another gate electrode wrapping around said semiconductor fin and separating said another source and another drain, wherein said first plurality of P-channel and said second plurality of N-channel multiple-gate transistors are triple-gate transistors, and a width of said semiconductor fin at said first plurality of P-channel multiple-gate transistors is different from a width of said semiconductor fin at said second plurality of N-channel multiple-gate transistors; and

an input terminal connected to the gate electrodes of said first plurality of P-channel and second plurality of N-channel multiple-gate transistors.

25. The inverter of claim 24, wherein said first plurality of P-channel and said second plurality of N-channel multiple-gate transistors are omega field-effect transistors.

26. The inverter of claim 24 or 25, wherein each of said first plurality of P-channel and said second plurality of N-channel multiple-gate transistors comprises:

a substrate having an insulating layer formed on top; and

a gate dielectric layer overlying said semiconductor fin;

wherein said semiconductor fin vertically is formed on said insulating layer, said semiconductor fin has a fin top and two fin sidewalls .

27. The inverter of any one of claims 24-26, wherein said semiconductor fin comprises silicon.
28. The inverter of any one of claims 24-27, wherein said semiconductor fin comprises silicon and germanium.
29. The inverter of any one of claims 24-28, wherein said first plurality of P-channel multiple-gate transistors and said second plurality of N-channel multiple-gate transistors are formed on different semiconductor fins.
30. The inverter of any one of claims 24-29, wherein said first plurality of P-channel multiple-gate transistors and said second plurality of N-channel multiple-gate transistors are formed on different numbers of semiconductor fins.
31. The inverter of any one of claims 26-30, wherein said insulating layer comprises a dielectric material.
32. The inverter of any one of claims 26-31, wherein said insulating layer comprises silicon oxide.
33. The inverter of any one of claims 26-32, wherein said insulating layer having a thickness between 20 Angstroms and 1000 Angstroms.
34. The inverter of any one of claims 26-33, wherein said gate dielectric layer comprises silicon oxide.

35. The inverter of any one of claims 26-24, wherein said gate dielectric layer comprises silicon oxynitride.
36. The inverter of any one of claims 26-35, wherein said gate dielectric layer comprises a high permittivity material selected from the group consisting of La_2O_3 , Al_2O_3 , HfO_2 , HfON and ZrO_2 .
37. The inverter of any one of claims 26-36, wherein said gate dielectric layer comprises a high permittivity material having a relative permittivity of at least 5.
38. The inverter of any one of claims 26-37, wherein said gate dielectric layer having a thickness between 3 Angstroms and 100 Angstroms.
39. The inverter of any one of claims 26-38, wherein said gate dielectric layer having a different thickness on said fin sidewall than on said fin top.
40. The inverter of any one of claims 26-39, wherein said gate dielectric layer having a smaller thickness on said fin top than on said fin sidewall.
41. The inverter of any one of claims 26-40, wherein said gate dielectric layer having a thickness on said fin top less than 20 Angstroms.
42. The inverter of any one of claims 24-41, wherein said gate electrode comprises polycrystalline silicon.
43. The inverter of any one of claims 24-42, wherein said gate electrode comprises polycrystalline silicon germanium.

44. The inverter of any one of claims 24-43, wherein said gate electrode comprises a metal.
45. The inverter of any one of claims 24-44, wherein said source and drain regions are strapped by a conductive material selected from the group consisting of metals and silicides.
46. The inverter of claim 45, wherein electrical contact between said conductive material and said source and drain regions is made on at least one of the fin sidewalls and fin top of the semiconductor fin.

CMOS INVERTERS CONFIGURED USING MULTIPLE-GATE TRANSISTORS

ABSTRACT OF THE DISCLOSURE

0056 An inverter that includes a first multiple-gate transistor including a source connected to a power supply, a drain connected to an output terminal, and a gate electrode; a second multiple-gate transistor including a source connected to a ground, a drain connected to the output terminal, and a gate electrode; and an input terminal connected to the gate electrodes of the first and second multiple-gate transistors. Each of the first and second multiple-gate transistors may further include a semiconductor fin formed vertically on an insulating layer on top of a substrate, a gate dielectric layer overlying the semiconductor fin, and a gate electrode wrapping around the semiconductor fin separating the source and drain regions.

FIG. 7