SRAM DEVICE HAVING HIGH ASPECT RATIO CELL BOUNDARY

ABSTRACT

A static random access memory (SRAM) device including a substrate and an SRAM unit cell. The substrate includes an n-doped region interposing first and second p-doped regions. The SRAM unit cell includes: (1) a first pass-gate transistor and a first pull-down transistor located at least partially over the first p-doped region; (2) first and second pull-up transistors located at least partially over the n-doped region; and (3) a second pass-gate transistor, a second pull-down transistor, and first and second read port transistors, all located at least partially over the second p-doped region. A boundary of the SRAM unit cell comprises first and second primary dimensions having an aspect ratio of at least about 3.2.

Fig. 5