Description

The present invention relates to a full adder circuit having a sum output terminal and a carry output terminal.

Conventionally, as shown in Fig. 1, a full adder circuit which generates sum signals S and $\overline{S}$ and carry output signals CO and $\overline{CO}$ in response to logic input signals A and B and carry input signals C and $\overline{C}$ is known from US-A-3.519.810. The full adder circuit comprises transistors TR1 and TR2 having bases respectively connected to input terminals IT1 and IT2 for receiving the input signals A and B and collectors connected to a power source terminal VCC; transistors TR3 to TR8 having bases commonly connected to an input terminal IT3 for receiving the carry input signal C; and transistors TR9 to TR14 having bases commonly connected to an input terminal IT4 for receiving the carry input signal $\overline{C}$. The collectors of the transistors TR3, TR6, TR10 and TR11 are commonly connected to the base of a transistor TR15 and are also commonly connected to the terminal VCC through a resistor R1. The collectors of the transistors TR4, TR5, TR9 and TR12 are commonly connected to the base of a transistor TR16 and are also commonly connected to the terminal VCC through a resistor R2. The collectors of the transistors TR7 and TR8 are commonly connected to the base of a transistor TR17 and are also connected to the terminal VCC through a resistor R3. The collectors of the transistors TR13 and TR14 are commonly connected to the base of a transistor TR18 and are also commonly connected to the terminal VCC through a resistor R4.

The collectors of the transistors TR15 to TR18 are commonly connected to the terminal VCC, and the emitters thereof are each commonly connected to a power source terminal VEE through resistors.

Furthermore, the full adder circuit comprises transistors TR19 to TR22 having bases commonly connected to the emitter of the transistor TR1; transistors TR23 to TR26 having bases commonly connected to a reference voltage terminal VR1; transistors TR27 and TR28 having bases commonly connected to the emitter of the transistor TR2 through a diode D; transistors TR29 and TR30 having bases commonly connected to a reference voltage terminal VR2; and transistors TR31 and TR32 having bases commonly connected to a reference voltage terminal VR3. The collectors of the transistors TR19, TR20, TR22, TR23, TR24 and TR25 are respectively connected to the emitters of the transistors TR3 and TR9, the emitters of the transistors TR5 and TR11, the emitters of the transistors TR8 and TR14, the emitters of the transistors TR4 and TR10, the emitters of the transistors TR6 and TR12, and the emitters of the transistors TR7 and TR13. The collectors of the transistors TR21 and TR26 are connected to the terminal VCC respectively through the resistors R3 and R4. The collectors of the transistors TR27 to TR32 are respectively connected to the emitters of the transistors TR19 and TR23, the emitters of the transistors TR21 and TR25, the emitters of the transistors TR20 and TR24, the emitters of the transistors TR22 and TR26, the emitters of the transistors TR27 and TR29, and the emitters of the transistors TR28 and TR30.

In the full adder circuit, the sum signal S and its inverted signal $\overline{S}$ thereof and the carry output signal CO and its inverted signal $\overline{CO}$ are generated from the emitters of the transistors TR16, TR15, TR18 and TR17 in accordance with the input signals A, B, C and $\overline{C}$, respectively. Assume that the input signals A and B are at "1" level, and the carry input signals C and $\overline{C}$ are "0" and "1" levels. In this case, a current flows through the transistors TR9, TR19, TR27 and TR31, thereby rendering the transistors TR15 and TR16 conductive and nonconductive, respectively. Therefore, the "0" level sum signal S can be derived from the emitter of the transistor TR16. On the other hand, since the input signals A and B and the carry input signal $\overline{C}$ are "1" level, a current flows through the transistors TR21, TR28 and TR32, thus rendering the transistors TR18 and TR17 conductive and nonconductive, respectively. Therefore, the "1" level carry output signal CO can be derived from the emitter of the transistor TR18.

In the conventional full adder circuit, a circuit section for generating the sum signal and that for generating the carry signal are formed independently of each other. For this reason, the number of transistors required for constituting the full adder circuit is increased, and it is difficult to constitute an integrated circuit. Furthermore, in the conventional full adder circuit, since current paths of a number of transistors are connected in series between the terminals VCC and VEE, it is difficult to determine levels of input and reference voltages. In addition, this circuit cannot be driven at a low voltage.

A conventional full adder circuit comprising CMOS transistors having a first exclusive-OR circuit for receiving logic input signals A and B; a second exclusive-OR circuit for receiving an output signal from the first exclusive-OR circuit and a carry input signal C so as to generate a sum signal SO; and a selection circuit for selecting the input signal B or the carry signal C in accordance with the output signal from the first exclusive-OR circuit so as to generate the selected signal as a carry output signal CO has been proposed. The configuration of the full adder circuit is based on a relationship among the input signals A and B, the carry input signal C, an exclusive-OR value of the signals A and B, the sum signal SO and the carry output signal CO. Unlike a conventional full adder circuit comprising CMOS transistors, the number of

elements is decreased, and the circuit is suited for integration. However, in this full adder circuit, since a number of MOS transistors are used, the operating speed is low.

In bipolar technology, ECL technique is advantageous for high speed operation. High speed gating like double balance type differential amplifier is disclosed in figure 5-2 of the publication TOUTE L'ELECTRONIQUE, No. 477 published in October 1982, pages 60 to 68.

It is an object of the present invention to provide a full adder circuit having a simple structure and suited for integration.

In order to achieve the above object, there is provided a full adder circuit comprising an exclusive-OR circuit for generating an output signal corresponding to an exclusive-OR value of first and second input signals; a sum signal selection circuit for generating a sum signal corresponding to a carry input signal when the output signal from said exclusive-OR circuit is at "0" level, and for generating a sum signal corresponding to an inverted carry input signal when the output signal from said exclusive-OR circuit is at "1" level; and a carry output signal selection circuit for generating a carry output signal corresponding to the first input signal when the output signal from that exclusive-OR circuit is at "0" level and for generating the carry output signal responding to the carry input signal characterized in that the exclusive-OR circuit comprises a double balance type differential amplifier connected between first and second power source terminals; said double balance type differential amplifying including a lower stage differential amplifier section operated in accordance with the second input signal and connected to an upper stage differential amplifier section operated in accordance with the first input signal; said sum signal selection circuit comprises a double balance type differential amplifier connected between said first and second power source terminals, said double balance type differential amplifier including a lower stage differential amplifier section having first and second current paths selectively activated in accordance with the output signal from said exclusive-OR circuit and an upper stage differential amplifier section generating said sum signal and having third to sixths current paths selectively activated in accordance with the carry input signal, said third and fourth current paths connected in series with said first current path and said fifth and sixth current path connected in series with said second current path; and said carry output signal selection circuit comprises a first differential amplifier having seventh and eighth current paths selectively activated in accordance with the output signal from said exclusive-OR circuit, a second differential amplifier having ninth and tenth current paths selectively activated in accordance with the first input signal and connected in series with said seventh current path and a third differential amplifier having eleventh and twelfth current paths selectively activated in accordance with the carry input signal and connected in series with said eighth current path, said carry output signal being provided by said second and third differential amplifiers.

Further advantageous features and embodiments of the present invention are disclosed in the sub-claims.

Since the exclusive-OR circuit and the sum selection circuit comprise the double balance type differential amplifiers and the carry output signal selection circuit comprises two-stage differential amplifier circuit, the full adder circuit of the present invention can be constructed with biopolar transistors having a simple arrangement. Since the number of the transistors having current paths series connected between the first and second power source terminals can be decreased, the circuit can be driven at a low voltage.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

- Fig. 1 is a circuit diagram of a conventional full adder circuit;
- Fig. 2 is a diagram showing a full adder circuit according to an embodiment of the present invention;
- Fig. 3 is a detailed circuit diagram of an exclusive-OR circuit shown in Fig. 2;
- Fig. 4 is a detailed circuit diagram of a sum signal selection circuit shown in Fig. 2;
- Fig. 5 is a detailed circuit diagram of a carry output signal selection circuit shown in Fig. 2; and
- Fig. 6 is a circuit diagram of the full adder circuit obtained by combining the circuits shown in Figs. 3 to 5.

Fig. 2 is a diagram showing a full adder circuit according to an embodiment of the present invention. The full adder circuit is constructed by utilizing the relationship among input signals A and B, a carry input signal C, an output signal OX from an exclusive-OR circuit 10 which receives the input signals A and B, a sum output signal QS and a carry output signal QC. This full adder circuit operates in accordance with the truth table shown below.

Table

A	B	C	QS	QC	QX
0	0	0	0 (= C)	0 (= A)	0
0	0	1	1 (= C)	0 (= A)	0
1	1	0	0 (= C)	1 (= A)	0
1	1	1	1 (= C)	1 (= A)	0
0	1	0	1 (= $\overline{C}$)	0 (= C)	1
0	1	1	0 (= $\overline{C}$)	1 (= C)	1
1	0	0	1 (= $\overline{C}$)	0 (= C)	1
1	0	1	0 (= $\overline{C}$)	1 (= C)	1

As can be seen from this truth dable, when the output signal QX of the exclusive-OR circuit 10 is at "0" level, the sum signal QS is equal to the carry input signal C and the carry output signal QC is equal to the input signal A. When the output signal QX of the circuit 10 is at "1" level, the sum signal QS is equal to a signal $\overline{C}$ which is obtained by inverting the carry input signal C and the carry output signal QC is equal to the carry input signal C.

In the full adder circuit shown in Fig. 2, the output terminal of the circuit 10 is connected to control terminals of a sum signal selection circuit 12 and a carry output signal selection circuit 14. The circuit 12 serves as a switching circuit having a first input terminal which directly receives the carry input signal C and a second input terminal which receives the carry input signal C through an inverter, and having an operation mode or switching position controlled by the output signal QX from the circuit 10. The circuit 12 is set in a first operation mode in response to the "0" output signal QX from the circuit 10 so as to generate the carry input signal C as a sum signal QS. The circuit is set in a second operation mode in response to the "1" output signal QX from the circuit 10 so as to generate as the sum signal QS a signal $\overline{C}$ obtained by inverting the carry input signal C. The circuit 14 serves as a switching circuit having a first input terminal which receives the input signal A and a second input terminal which receives the carry input signal C, and having an operation mode or switching position controlled by the output signal QX from the circuit 10. The circuit 14 is set in a first operation mode in response to the "0" output signal QX from the circuit 10 so as to generate the input signal A as the carry output signal QC, and is set in a second operation mode in response to the "1" output signal QX from the circuit 10 so as to generate the carry input signal C as the carry output signal QC. These circuits 10, 12 and 14 are driven by a power supply voltage VC.

Fig. 3 is a detailed circuit diagram of the exclusive-OR circuit 10 shown in Fig. 2. The circuit 10 includes a double balance type differential amplifier circuit having npn transistors Q1 to Q6, load resistors R10 and R11 and a constant current source CCS1, and an output circuit having npn transistors Q7 and Q8 and constant current sources CCS2 and CCS3. In this differential amplifier circuit, the emitters of the transistors Q1 and Q2 are grounded through the current source CCS1, and the emitters of the transistors Q3 and Q4 are commonly connected to the collector of the transistor Q1. The emitters of the transistors Q5 and Q6 are commonly connected to the collector of the transistor Q2. The input signal A is supplied to the bases of the transistors Q3 and Q6, and the input signal B is supplied to the base of the transistor Q1. A voltage V1 having a level between HIGH and LOW levels of the signal B is supplied to the base of the transistor Q2, and a voltage V2 having a level between HIGH and LOW levels of the signal A is supplied to the bases of the transistors Q4 and Q5. However, in this case, a signal $\overline{B}$ can be supplied to the base of the transistor Q2 and a signal $\overline{A}$ can be supplied to the bases of the transistors Q4 and Q5.

The collectors of the transistors Q3 and Q5 are commonly connected to the base of the transistor Q8, and are commonly connected to a power source terminal VC through the resistor R10. The collectors of the transistors Q4 and Q6 are connected to the base of the transistor Q7, and are commonly connected to the power source terminal through the resistor R11. The collectors of the transistors Q7 and Q8 are commonly connected to the terminal VC and emitters thereof are grounded through the current sources CCS2 and CCS3. The output signal QX corresponding to the exclusive-OR value of the input signals A and B and an inverted signal $\overline{QX}$ thereof is generated from the emitters of the transistors Q8 and Q7.

For example, when the input signals A and B are respectively at "1" and "0" levels, the transistors Q2 and Q6 are turned on and the transistors Q1 and Q5 are turned off. Thus, the HIGH and LOW level signals are supplied to the bases of the transistors Q7 and Q8, respectively, thereby turning them on and off. Therefore, output signals of "0" and "1" levels are generated from the emitters of the transistors Q7 and Q8, respectively.

Fig. 4 shows a detailed circuit diagram of the sum signal selection circuit 12. The circuit 12 includes a

double balance type differential amplifier circuit having npn transistors Q9 to Q14, load resistors R12 and R13 and a constant current source CCS4. In this differential amplifier circuit, the emitters of the transistors Q9 and Q10 are grounded through the current source CCS4, and the emitters of the transistors Q11 and Q12 are commonly connected to the collector of the transistor Q9. The emitters of the transistors Q13 and Q14 are commonly connected to the collector of the transistor Q10. The output signals QX and $\overline{QX}$ from the circuit 10 are respectively supplied to the bases of the transistors Q9 and Q10. The carry input signal C is supplied to the bases of the transistors Q11 and Q14, and a voltage V3 having an intermediate level between HIGH and LOW levels of the signal C is applied to the bases of the transistors Q12 and Q13. The signal C can be supplied to the bases of the transistors Q12 and Q13 instead of the voltage V3. The collectors of the transistors Q11 and Q13 are commonly connected to the power source terminal VC through the resistor R12, and the collectors of the transistors Q12 and Q14 are commonly connected to the terminal VC through the resistor R13. The sum signal QS is generated from the collectors of the transistors Q11 and Q13, and the inverted sum signal $\overline{QS}$ is generated from the collectors of the transistors Q12 and Q14.

The circuit 12 generates the sum signal QS in correspondence with the output signals QX and $\overline{QX}$ and the carry input signal C so as to satisfy the relation shown in the above truth table. That is, when the signals QX and C are at "1" and "0" levels, respectively, the "1" level sum signal QS is generated, and in other cases, the "0" level sum signal QS is generated.

Fig. 5 is a detailed circuit diagram of the carry output signal selection circuit 14. The circuit 14 includes a differential amplifier having npn transistors Q15 and Q16, a differential amplifier having npn transistors Q17 and Q18, a differential amplifier having npn transistors Q19 and Q20, a constant current source CCS5 and load resistors R14 and R15. The emitters of the transistors Q15 and Q16 are grounded through the current source CCS5, the emitters of the transistors Q17 and Q18 are commonly connected to the collector of the transistor Q15, and the emitters of the transistors Q19 and Q20 are commonly connected to the collector of the transistor Q16. The collectors of the transistors Q17 and Q19 are commonly connected to the power source terminal VC through the resistor R14, and the collectors of the transistors Q18 and Q20 are commonly connected to the terminal VC through the resistor R15. Furthermore, the output signals QX and $\overline{QX}$ from the circuit 10 are respectively supplied to the bases of the transistors Q16 and Q15, and the input signal A and the carry input signal C are respectively supplied to the bases of the transistors Q17 and Q19. A voltage V4 having an intermediate level between HIGH and LOW levels of the input signal A is applied to the base of the transistor Q18. A voltage V5 having an intermediate level between HIGH and LOW levels of the carry input signal C is applied to the base of the transistor Q20. In this case, the inverted input signal $\overline{A}$ can be supplied to the base of the transistor Q18 instead of the voltage V4, and the inverted carry input signal $\overline{C}$ can be supplied to the base of the transistor Q20 instead of the voltage V5.

The circuit 14 generates the carry output signal QC so as to satisfy the relation shown in the above truth table in response to the output signals QX and $\overline{QX}$ from the circuit 10, the input signal A and the carry input signal C. That is, when the signal QX is at "0" level and the signal A is at "0" level, or when the signal QX is at "1" level and the signal C is at "0" level, the "0" carry output signal QC is generated. In other cases, the "1" carry output signal is generated.

Fig. 6 shows a circuit combining the circuits 10, 12 and 14 shown in Figs. 3 to 5. Note that in Fig. 6, the signals $\overline{B}$; $\overline{A}$; $\overline{C}$; $\overline{A}$ and $\overline{C}$ are respectively supplied to the bases of the transistors Q2, Q4 and Q5; Q12 and Q13, Q18; and Q20.

Assuming that the input signals A and B are at "1" level and the carry input signal C is at "0" level, since the transistors Q1, Q2 and Q6 are turned on, the transistor Q7 is turned on and the transistor Q8 is turned off. Thus, the output signals QX and $\overline{QX}$ of "0" and "1" levels are generated from the circuit 10. In the circuit 12, since the transistors Q10 and Q13 are turned on, the sum signal QS of "0" level is generated therefrom. On the other hand, in the circuit 14, since the transistors Q15 and Q17 are turned on, the carry output signals QC and $\overline{QC}$ or "1" and "0" levels are generated therefrom. In this manner, when the input signals A and B of "1" level and the carry input signal of "0" level are supplied to the full adder circuit, the circuit generates the sum signal QS of "0" level and the carry output signal QC of "1" level. As shown in the truth table described before, the full adder circuit can generated the sum input signal QS and the carry output signal QC with respect to various combinations of the input signals A, B and C so as to satisfy the relation shown in the truth table.

The full adder circuit according to the above embodimnt comprises the transistors Q1 to Q20 and as compared to the circuit comprising TR1 to TR32 shown in Fig. 1, the number of elements can be greatly decreased and an arrangement thereof is simple. Since the number of the transistors series-connected between the power source terminal VC and ground is small, a drive voltage applied to this power soure terminal can be decreased.

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Claims

1. A bipolar full adder circuit comprising

an exclusive-OR circuit (10) for generating an output signal (QX) corresponding to an exclusive-OR value of first and second input signals (A, B);

a sum signal selection circuit (12) for generating a sum signal (QS) corresponding to a carry input signal (c) when the output signal (QX) from said exclusive-OR circuit (10) is at "0" level, and for generating a sum signal (QS) corresponding to an inverted carry input signal ($\bar{c}$) when the output signal (QX) from said exclusive-OR circuit (10) is at "1" level; and

a carry output signal selection circuit (14) for generating a carry output signal (QC) corresponding to the first input signal (A) when the output signal (QX) from said exclusive-OR circuit (10) is at "0" level, and for generating the carry output signal (QC) corresponding to the carry input signal (C);

characterized in that

said exclusive-OR circuit (10) comprises a double balance type differential amplifier connected between first and second power source terminals (TC, GND); said double balance type differential amplifier including a lower stage differential amplifier section (Q1, Q2) operated in accordance with the second input signal (B) and and connected to an upper stage differential amplifier section (Q3, Q4, Q5, Q6) operated in accordance with the first input signal (A);

said sum signal selection circuit (12) comprises a double balance type differential amplifier connected between said first and second power source terminals (TC, GND), said double balance type differential amplifier including a lower stage differential amplifier section (Q9, Q10) having first and second current paths selectively activated in accordance with the output signal (QX) from said exclusive-OR circuit (10), and an upper stage differential amplifier section (Q11, Q12, Q13, Q14) generating said sum signal (Q5) and having third to sixth current paths selectively activated in accordance with the carry input signal (c), said third and fourth current paths connected in series with said first curent path and said fifth and sixth current paths connected in series with said second current path; and

said carry output signal selection circuit (14) comprises a first differential amplifier (Q15, Q16) having seventh and eight current paths selectively activated in accordance with the output signal (QX) from said exclusive-OR circuit (10), a second differential amplifier (Q17, Q18) having ninth and tenth curent paths selectively activated in accordance with the first input signal (A) and connected in series with said seventh current path, and a third differential amplifier (Q19, Q20) having eleventh and twelfth current paths selectively activated in accordance with the carry input signal (c) and connected in series with said eighth current path, said carry output signal being provided by said second and third differential amplifiers.

2. A circuit according to claim 1,
characteerized in that
said exclusive-OR circuit (10) comprises a differential amplifier including first and second transistors (Q1, Q2) having emitters commonly connected to said second power source terminal through a first current source (CSS1) and operated in accordance with the second input signal (B);

a differential amplifier including third and fourth transistors (Q3, Q4) whose emitters are commonly connected to the collector of said first transistor (Q1) and operated in accordance with the first input signal (A);

a differential amplifier including fifth and sixth transistors (Q5, Q6) whose emitters are commonly connected to the collector of said second transistor (Q2) and operated in accordance with the first input signal (A);

first resistor means (R10) connected between said first power source terminal (VC) and a node between the collectors of said third and fifth transistors (Q3, Q5); and

second resistor means (R11) connected between said first power source terminal (VC) and a node between the collectors of said fourth and sixth transistors (Q4, Q6).

3. A circuit according to claim 2,
characterized in that
said sum signal selection circuit (12) comprises

a differential amplifier including seventh and eight transistors (Q9, Q10) whose emitters are connected to said second power source terminal (GND) through a second current source (CCS4) and operated in accordance with the output signal (QX) from said exclusive-OR circuit (10);

a differential amplifier including ninth and tenth transistors (Q11, Q12) whose emitters are commonly connected to the collector of said seventh transistor (Q9) and operated in accordance with the carry input signal (c);

a differential amplifier including eleventh and twelfth transistors (Q13, Q14) whose emitters are commonly connected to the collector of said eigth transistor (Q10) and operated in accordance with the carry input signal (c);

third resistor means (R12) connected between said first power source terminal (VC) and a node between the collectors of said ninth and eleventh transistors (Q11, Q13); and

fourth resistor means (R13) connected between said first power source terminal (VC) and a node between the collectors of said tenth and twelfth transistors (Q12, Q14).

4. A circuit according to claim 3,
characterized in that
said first differential amplifier (Q15, Q16) of said carry output signal selection circuit (14) includes thirteenth and fourteenth transistors (Q15, Q16) whose emitters are commonly connected to said second power source terminal (GND) through a third current source (CCS5),

said second differential amplifier (Q17, Q18) includes fifteenth and sixteenth transistors (Q17, Q18) whose emitters are commonly connected to the collector of said thirteenth transistor (Q15), and

said third differential amplifier (Q19, Q20) includes seventeenth and eighteenth transistors (Q19, Q20) whose emitters are commonly connected to the collector of said fourteenth transistor (Q16), the collectors of said fifteenth and seventeenth transistors being connected to said first power source terminal (VC) through fifth resistor means (R14), and the collectors of said sixteenth and eighteenth transistors being connected to said first power source terminal (VC) through sixth resistor means (R15).

Revendications

1. Circuit additionneur complet bipolaire comprenant
un circuit OU-exclusif (10) pour engendrer un signal de sortie (QX) correspondant à une valeur de OU-exclusif de premier et second signaux d'entrée (A,B);
un circuit de sélection de signal de somme (12) pour engendrer un signal de somme (QS) correspondant à un signal d'entrée de report (C) quand le signal de sortie (QX) dudit circuit OU-exclusif (10) est à un niveau "0", et pour engendrer un signal de somme (QS) correspondant à un signal d'entrée de report inversé ($\overline{C}$) quand le signal de sortie (QX) dudit circuit OU-exclusif (10) est à un niveau "1"; et
un circuit de sélection de signal de sortie de report (14) pour engendrer un signal de sortie de report (QC) correspondant au premier signal d'entrée (A) quand le signal de sortie (QX) dudit circuit OU-exclusif (10) est à un niveau "0", et pour engendrer le signal de sortie de report (QC) correspondant au signal d'entrée de report (C);
caractérisé en ce que
ledit circuit OU-exclusif (10) comprend un double amplificateur différentiel du type à équilibrage connecté entre des première et seconde bornes de source d'alimentation (TC,GND), ledit double

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amplificateur différentiel du type à équilibrage incluant une partie d'amplificateur différentiel d'étage inférieur (Q1,Q2) rendu actif selon le second signal d'entrée (B) et connecté à une partie d'amplificateur différentiel d'étage supérieur (Q3,Q4,Q5,Q6) rendu actif selon le premier signal d'entrée (A);

ledit circuit de sélection de signal de somme (12) comprend un double amplificateur différentiel du type à équilibrage connecté entre lesdites première et seconde bornes de source d'alimentation (TC,GND), ledit double amplificateur différentiel du type à équilibrage incluant une partie d'amplificateur différentiel d'étage inférieur (Q9,Q10) comportant des première et deuxième voies de courant rendues actives sélectivement selon le signal de sortie (QX) dudit circuit OU-exclusif (10), et une partie d'amplificateur différentiel d'étage supérieur (Q11,Q12,Q13,Q14) générant ledit signal de somme (QS) et comportant des troisième à sixième voies de courant rendues actives sélectivement selon le signal d'entrée de report (C), lesdits troisième et quatrième voies de courant étant connectées en série à ladite première voie de courant et les cinquième et sixième voies de courant étant connectées en série à ladite deuxième voie de courant; et

ledit circuit de sélection de signal de osrtie de report (14) comprend un premier amplificateur différentiel (Q15,Q16) comportant des septième et huitième voies de courant rendues actives sélectivement selon le signal de sortie (QX) dudit circuit OU-exclusif (10), un deuxième amplificateur différentiel (Q17,Q18) comportant des neuvième et dixième voies de courant rendues actives sélectivement selon le premier signal d'entrée (A) et connectées en série à ladite septième voie de courant, et un troisième amplificateur différentiel (Q19,Q20) comportant des onzième et douzième voies de courant rendues actives sélectivement selon le signal d'entrée de report (C) et connectées en série à ladite huitième voie de courant, ledit signal de sortie de report étant fourni par lesdits deuxième et troisième amplificateurs différentiels.

2. Circuit selon la revendication 1, caractérisé en ce que ledit circuit OU-exclusif (10) comprend

un amplificateur différentiel incluant des premier et deuxième transistors (Q1,Q2) comportant des émetteurs connectés en commun à ladite seconde borne de source d'alimentation par l'intermédiaire d'une première source de courant (CCS1) et rendu actif selon le second signal d'entrée (B);

un amplificateur différentiel incluant des troisième et quatrième transistors (Q3,Q4) dont les émetteurs sont connectés en commun au collecteur dudit premier transistor (Q1) et rendu actif selon le premier signal d'entrée (A);

un amplificateur différentiel incluant des cinquième et sixième transistors (Q5,Q6) dont les émetteurs sont connectés en commun au collecteur dudit deuxième transistor (Q2) et rendu actif selon le premier signal d'entrée (A);

un premier moyen à résistance (R10) connecté entre ladite première borne de source d'alimentation (VC) et un noeud entre les collecteurs desdits troisième et cinquième transistors (Q3,Q5); et

un deuxième moyen à résistance (R11) connecté entre ladite première borne de source d'alimentation (VC) et un noeud entre les collecteurs desdits quatrième et sixième transistors (Q4,Q6).

3. Circuit selon la revendication 2,caractérisé en ce que ledit circuit de sélection de signal de somme (12) comprend

un amplificateur différentiel incluant des septième et huitième transistors (Q9,Q10) dont les émetteurs sont connectés à ladite seconde borne de source d'alimentation (GND) par l'intermédiaire d'une deuxième source de courant (CCS4) et rendu actif selon le signal de sortie (QX) dudit circuit OU-exclusif (10);

un amplificateur différentiel incluant des neuvième et dixième transistors (Q11,Q12) dont les émetteurs sont connectés en commun au collecteur dudit septième tran - sistor (Q9) et rendu actif selon le signal d'entrée de report (C);

un amplificateur différentiel incluant des onzième et douzième transistors (Q13,Q14) dont les émetteurs sont connectés en commun au collecteur dudit huitième transistor (Q10) et rendu actif selon le signal d'entrée de report (C);

un troisième moyen à résistance (R12) connecté entre ladite première borne de source d'alimentation (VC) et un noeud entre les collecteurs desdits neuvième et onzième transistors (Q11,Q13); et

un quatrième moyen à résistance (R13) connecté entre ladite première borne de source d'alimentation (VC) et un noeud entre les collecteurs desdits dixième et douzième transistors (Q12,Q14).

4. Circuit selon la revendication 3, caractérisé en ce que

ledit premier amplificateur différentiel (Q15,Q16) dudit circuit de sélection de signal de sortie de report (14) comprend des treizième et quatorzième transistors (Q15,Q16) dont les émetteurs sont

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connectés en commun à ladite seconde borne de source d'alimentation (GND) par l'intermédiaire d'une troisième source de courant (CCS5),

ledit deuxième amplificateur différentiel (Q17,Q18) comprend des quinzième et seizième transistors (Q17,Q18) dont les émetteurs sont connectés en commun au collecteur dudit treizième transistor (Q15), et

ledit troisième amplificateur différentiel (Q19,Q20) comprend des dix-septième et dix-huitième transistors (Q19,Q20) dont les émetteurs sont connectés en commun au collecteur dudit quatorzième transistor (Q16), les collecteurs desdits quinzième et dix-septième transistors étant connectés à ladite première borne de source d'alimentation (VC) par l'intermédiaire d'un cinquième moyen à résistance (R14), et les collecteurs desdits seizième et dix-huitième transistors étant connectés à ladite première borne de source d'alimentation (VC) par l'intermédiaire d'un sixième moyen à résistance (R15).

Patentansprüche

1. Bipolare Volladdiererschaltung, mit:
   - einer Exklusiv-ODER-Schaltung (10) zur Erzeugung eines Ausgangssignals (QX) entsprechend einem Exklusiv-ODER-Wert eines ersten und zweiten Eingangssignals (A, B);
   - einer Summensignal-Auswahlschaltung (12) zur Erzeugung eines Summensignals (QS) entsprechend einem Übertrageingangssignal (C), wenn sich das von der Exklusiv-ODER-Schaltung (10) gelieferte Ausgangssignal (QX) auf Pegel "0" befindet, und zur Erzeugung eines Summensignals (QS) entsprechend einem invertierten Übertrageingabesignal ($\overline{C}$), wenn sich das von der Exklusiv-ODER-Schaltung gelieferte Ausgangssignal (QX) auf Pegel "1" befindet; und
   - einer Übertragausgabesignal-Auswahlschaltung (14) zur Erzeugung eines Übertragausgabesignals (QC) entsprechend dem ersten Eingangssignal (A), wenn sich das von der Exklusiv-ODER-Schaltung gelieferte Ausgangssignal (QX) auf Pegel "0" befindet, und zur Erzeugung des Übertragausgabesignals (QC) entsprechend dem Übertrageingabesignal (C);

   dadurch **gekennzeichnet,** daß:
   - die Exklusiv-ODER-Schaltung (10) einen zwischen erste und zweite Leistungsversorgungsanschlüsse (TC, GND) angeschlossenen doppelsymmetrischen Differenzverstärker aufweist, der einen Differenzverstärkerteil (Q1, Q2) einer unteren Stufe umfaßt, welcher entsprechend dem zweiten Eingangssignal (B) betrieben wird und an einen Differenzverstärkerteil (Q3, Q4, Q5, Q6) einer oberen Stufe angeschlossen ist, der entsprechend dem ersten Eingangssignal (A) betrieben wird;
   - die Summensignal-Auswahlschaltung (12) einen zwischen erste und zweite Leistungsversorgungsanschlüsse (TC, GND) angeschlossenen doppelsymmetrischen Differenzverstärker aufweist, der einen Differenzverstärkerteil (Q9, Q10) einer unteren Stufe mit ersten und zweiten, selektiv entsprechend dem von der Exklusiv-ODER-Schaltung (10) gelieferten Ausgangssignal (QX) aktivierten Strompfaden und einen Differenzverstärkerteil (Q11, Q12, Q13, Q14) einer oberen Stufe umfaßt, der das Summensignal (QS) erzeugt und dritte bis sechste, selektiv entsprechend dem Übertrageingabesignal (C) aktivierte Strompfade besitzt, wobei der dritte und vierte Strompfad in Reihe mit dem ersten Strompfad, und der fünfte und sechste Strompfad in Reihe mit dem zweiten Strompfad geschaltet ist; und
   - die Übertragausgangssignal-Auswahlschaltung (14) einen ersten Differenzverstärker mit siebten und achten Strompfaden, die selektiv entsprechend dem von der Exklusiv-ODER-Schaltung (10) gelieferten Ausgangssignal (QX) aktiviert werden; einen zweiten Differenzverstärker (Q17, Q18) mit neunten und zehnten Strompfaden, die selektiv entsprechend dem ersten Eingangssignal (A) aktiviert werden und in Reihe mit dem siebten Strompfad geschaltet sind; und einen dritten Differenzverstärker (Q19, Q20) mit elften und zwölften Strompfaden aufweist, die selektiv entsprechend dem Übertragungssignal (C) aktiviert werden und in Reihe mit dem achten Strompfad geschaltet sind, wobei das Übertragsausgabesignal vom zweiten und dritten Differenzverstärker geliefert wird.

2. Schaltung nach Anspruch 1,
   dadurch **gekennzeichnet,** daß die
   Exklusiv-ODER-Schaltung (10) aufweist:
   - einen Differenzverstärker mit ersten und zweiten Transistoren (Q1, Q2), deren Emitter gemeinsam über eine erste Stromquelle (CSS1) an den zweiten Leistungsversorgungsanschluß angeschlossen sind und entsprechend dem zweiten Eingangssignal (B) betrieben werden;

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- einen Differenzverstärker mit dritten und vierten Transistoren (Q3, Q4), deren Emitter gemeinsam an den Kollektor des ersten Transistors (Q1) angeschlossen sind und entsprechend dem ersten Eingangssignal (A) betrieben werden;
- einen Differenzverstärker mit fünften und sechsten Transistoren (Q5, Q6), deren Emitter gemeinsam an den Kollektor des zweiten Transistors (Q2) angeschlossen sind und entsprechend dem ersten Eingangssignal (A) betrieben werden;
- erste Widerstandsmittel (R10), die zwischen den ersten Leistungsversorgungsquellenanschluß (VC) und einen Knoten zwischen den Kollektoren der dritten und fünften Transistoren (Q3, Q5) geschaltet sind; und
- zweite Widerstandsmittel (R11), die zwischen den ersten Leistungsversorgungsquellenanschluß (VC) und einen Knoten zwischen den Kollektoren der vierten und sechsten Transistoren (Q4, Q6) geschaltet sind.

3. Schaltung nach Anspruch 2,
dadurch **gekennzeichnet,** daß die Summensignal-Auswahlschaltung aufweist:
- einen Differenzverstärker mit siebten und achten Transistoren (Q9, Q10), deren Emitter über einen zweiten Leistungsversorgungsanschluß (CCS4) an den zweiten Leistungsversorgungsanschluß (GND) angeschlossen sind und entsprechend dem von der Exklusiv-ODER-Schaltung (10) gelieferten Ausgangssignal (QX) betrieben werden;
- einen Differenzverstärker mit neunten und zehnten Transistoren (Q11, Q12), deren Emitter gemeinsam an den Kollektor des siebten Transistors (Q9) angeschlossen sind und entsprechend dem Übertrageingabesignal (C) betrieben werden;
- einen Differenzverstärker mit elften und zwölften Transistoren (Q13, Q14), deren Emitter gemeinsam an den Kollektor des achten Transistors (Q10) angeschlossen sind und entsprechend dem Übertrageingabesignal (C) betrieben werden;
- dritte Widerstandsmittel (R12), die zwischen den ersten Leistungsversorgungsquellenanschluß (VC) und einen Knoten zwischen den Kollektoren der neunten und elften Transistoren (Q11, Q13) geschaltet sind; und
- vierte Widerstandsmittel (R13), die zwischen den ersten Leistungsversorgungsquellenanschluß (VC) und einen Knoten zwischen den Kollektoren der zehnten und zwölften Transistoren (Q12, Q14) geschaltet sind.

4. Schaltung nach Anspruch 3,
dadurch **gekennzeichnet,** daß:
- der erste Differenzverstärker (Q15, Q16) der Übertragausgabesignal-Auswahlschaltung (14) dreizehnte und vierzehnte Transistoren (Q15, Q16) aufweist, deren Emitter über eine dritte Stromquelle (CCS5) gemeinsam an den zweiten Leistungsversorgungsanschluß (GND) angeschlossen sind;
- der zweite Differenzverstärker (Q17, Q18) fünfzehnte und sechzehnte Transistoren (Q17, Q18) aufweist, deren Emitter gemeinsam an den Kollektor des dreizehnten Transistors (Q15) angeschlossen sind; und
- der dritte Differenzverstärker (Q19, Q20) siebzehnte und achtzehnte Transistoren (Q19, Q20) aufweist, deren Emitter gemeinsam an den Kollektor des vierzehnten Transistors angeschlossen sind, wobei die Kollektoren des fünfzehnten und siebzehnten Transistors über die fünften Widerstandsmittel (R14) an den ersten Leistungsversorgungsanschluß (VC) und die Kollektoren des sechzehnten und achtzehnten Transistors über die sechsten Widerstandsmittel (R15) an den ersten Leistungsversorgungsanschluß (VC) angeschlossen sind.