DESCRIPTION

METHODS OF FORMING THROUGH SUBSTRATE INTERCONNECTS

TECHNICAL FIELD

Embodiments disclosed herein pertain to methods of forming through substrate interconnects.

BACKGROUND

Integrated circuits are commonly fabricated using semiconductor substrates. Numerous processes are used in the fabrication of the circuits, including, for example, deposition of material, etching of material, doping, photolithography, metallization, oxidation, etc. Most often, a plurality of identical integrated circuits are formed over a single substrate, commonly referred to as a wafer, to define individual circuit die. These are ultimately singulated into separated die or chips, which are then packaged. In other applications, a single wafer or other substrate might be fabricated to comprise one or more different integrated circuits, and may not be singulated. Regardless, a continuing goal in the fabrication of integrated circuitry is to make ever denser and smaller devices, and resultant integrated circuitry.

One manner of increasing density in a semiconductor assembly is to stack individual substrates, such as semiconductor die, one upon another. The stacked semiconductor die may be interconnected by forming conductive vias in through holes in one or more of the semiconductor dies, for example prior to singulation. An interior of each of the vias may be coated with an electrically insulating material followed by an electrically conductive material to electrically connect the vias to integrated circuitry fabricated on a primary circuitry side of the substrate. Thus, the conductive vias provide a conductive pathway from the primary circuitry side of a semiconductor substrate to its back-side or back-surface for conductive contact with another substrate.

The integrated circuit die, when near completion and prior to singulation, are usually provided with one or more dielectric passivation layers on one or both sides of the substrate. Such layers might provide one or more of insulative protection, stress buffering, and/or a moisture barrier to underlying circuitry. The through hole vias are then formed through the passivation layer(s) and into

semiconductive and other material of the substrate. As above, in order to isolate the conductive portion of the through substrate interconnect from other portions of the substrate, the vias are lined with one or more electrically insulating materials. As the throughway for vias become narrower, it can be problematic to completely line sidewalls of such vias with dielectric material prior to forming conductive material therein. One existing manner of doing so comprises pulsed chemical vapor deposition of an aluminum oxide-comprising material. Such is deposited over the dielectric layer and into the via to line the sidewalls of the via. Differences in thermal coefficients of expansion among the aluminum oxide-comprising material, the passivation dielectric material and materials of the substrate can undesirably cause separation and cracking or one or more of these materials.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagrammatic sectional view of a semiconductor substrate in process in accordance with an embodiment of the invention.

Figs. 2-5 illustrate a method embodiment of the invention.

Fig. 6 is a diagrammatic sectional view of another semiconductor substrate in process in accordance with an embodiment of the invention.

Figs. 7 and 8 illustrate a method embodiment of the invention.

Fig. 9 is a diagrammatic sectional view of another semiconductor substrate in process in accordance with an embodiment of the invention.

Figs. 10-12 illustrate a method embodiment of the invention.

Fig. 13 is a diagrammatic sectional view of another semiconductor substrate in process in accordance with an embodiment of the invention.

Figs. 14-17 illustrate a method embodiment of the invention.

Fig. 18 is a diagrammatic sectional view of another semiconductor substrate in process in accordance with an embodiment of the invention.

Fig. 19 is a diagrammatic sectional view of another semiconductor substrate in process in accordance with an embodiment of the invention.

Figs. 20 and 21 illustrate a method embodiment of the invention.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Embodiments of the invention encompass methods of forming through substrate interconnects, sometimes referred to in the existing art as through wafer interconnects. In the context of this document, a "through substrate interconnect" is a conductive interconnect extending from a back-side of a semiconductor substrate to integrated circuitry formed on or proximate a front-side of the substrate. Further in the context of this document, the "front-side" of a semiconductor substrate is that one of the two major opposing sides of the substrate (the other being the "back-side") from which the circuit components of the integrated circuitry are primarily fabricated. Further in the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Example methods of forming through substrate interconnects are initially described with reference to Figs. 1-5. Referring to Fig. 1, a semiconductor substrate is indicated generally with reference numeral 10, and comprises a first major side 12 and a second major side 14. By way of example only, a thickness range for substrate 10 is from about 700 microns to about 800 microns. Side 12 may comprise a back-side of the semiconductor substrate and side 14 may comprise a front-side of the semiconductor substrate. Yet alternately, side 12 may comprises the front-side of the semiconductor substrate and side 14 may comprise the back-side of the semiconductor substrate. Regardless, semiconductor substrate 10 is depicted as comprising some region 16 and a passivation dielectric layer 18 has been formed thereover. In the context of this document, a "passivation dielectric" is any dielectric material formed over an outer surface of a substrate after completion of most all of the integrated circuit components. Redistribution layers and/or other conductive lines might be formed over passivation dielectric 18, and other insulating and/or passivating layers might be provided thereover as well, but regardless the vast majority of

the integrated circuit devices has been fabricated inwardly of the passivation dielectric in what is generally depicted as region 16. Accordingly, region 16 will include a plurality of different materials, layers, and regions having integrated circuit components and devices (not shown) fabricated therein, including at least some semiconductive material.

Fig. 1 depicts passivation dielectric 18 being deposited onto substrate side 12. Where substrate region 16 comprises bulk semiconductor material and substrate side 12 comprises the back-side, passivation dielectric 18 has been formed over bulk semiconductive material of substrate region 16. Silicon, for example bulk monocrystalline silicon, is but one example semiconductive material. An example thickness range for layer 18 is from 1 micron to 25 microns. By way of example only, example materials for layer 18 include polyimide, polybenzoxazole, spin-on dielectric, and epoxies.

Referring to Fig. 2, a via 20 has been formed through passivation dielectric 18 and into semiconductive material of substrate 10 from side 12. Such may comprise a through via at this point or subsequent in the processing. In the context of this document, a "through via" is at some point a passageway extending from a substrate back-side to at least proximate a substrate front-side for ultimate conductive connection with one or more circuit devices on the front-side or with another substrate received over/proximate the front-side. For purposes of the continuing discussion, via 20 can be considered as comprising sidewalls 22 and a base 24. Fig. 2 also depicts via 20 as only being formed partially through substrate 10, although formation of via 20 completely through substrate 10 might also be utilized. Further, substrate 10 might be thinned by polishing or other action prior to or after forming via 20, and regardless of whether via 20 extends partially or completely through substrate 10. By way of examples only, cross-sectional configurations for via 20 are circular or oval, having an example minimum diameter/cross-dimension of from about 5 microns to about 70 microns.

Referring to Fig. 3, a liquid dielectric 30 has been applied over passivation dielectric 18 and into via 20 to line at least an elevationally outermost portion of via sidewalls 22 relative substrate side 12 from which via 20 was at least initially formed. In one embodiment and as shown, the application of a liquid dielectric 30 lines all of sidewalls 22 of via 20 with

liquid dielectric 30, and completely covers base 24 of via 20 with liquid dielectric 30. Alternately by way of example only, liquid dielectric 30 may line only an elevationally outermost portion of sidewalls 22 relative substrate side 12, for example only 5%, 25%, 50%, 75%, etc. of the outermost elevational length of sidewalls 22 of via 20. Further by way of example only, liquid dielectric 30 might be applied to line all of sidewalls 22 yet only a portion of via base 24, or only a portion of sidewalls 22 and none of via base 24. In one embodiment, the application of liquid dielectric lines all sidewalls of at least passivation dielectric 18 of via 20 with dielectric material 30. In one embodiment, the application of liquid dielectric lines at least an elevationally outermost portion of semiconductive material sidewalls of via 20 inward of passivation dielectric 18 with liquid dielectric 30, for example where substrate side 12 is the back-side and semiconductor region 16 immediately adjacent passivation dielectric 18 comprises bulk semiconductor material, for example silicon.

In one embodiment, the liquid dielectric 30 comprises a liquid polymer, and regardless in one embodiment comprises a spin-on dielectric applied over substrate side 12 in a spin-on manner, and whether by an existing method or a yet-to-be developed method. However, any suitable flowable dielectric is contemplated whether existing or yet-to-be developed, and whether provided onto substrate 10 by spin-on or other technique. Example materials are JSR WPR-S170P available from JSR Corporation of Tokyo, Japan, CRC-7561 available from Sumitomo Bakelite of Tokyo, Japan, and SINR-3150HSM from Shin-Etsu MicroSi of Phoenix, AZ. Of course, solvent or other material might be added to provide a desired viscosity, and various spin coating times and rpms might be utilized where spin coating is used to achieve desired degree of covering of liquid dielectric 30 relative to one or both via sidewalls 22 and via base 24. Spin-on dielectric application may be desirable to take advantage of simpler and lower cost existing such techniques without requiring vacuum processing.

Liquid dielectric 30 within via 20 is solidified, and conductive material is formed within via 20 over solidified dielectric 30 and a through substrate interconnect is formed with the conductive material. The solidifying is effective to adhere and cease flow of material 30 relative to substrate 16/18, and may

include one or more elevated temperature baking steps to drive solvent from material 30 as part of ultimate solidification. Further and by way of example only, application of liquid dielectric 30 to a desired thickness and coverage relative to all or portions of sidewalls 22 and/or base 24 might occur or be conducted in a single liquid dielectric application step, or in multiple separate liquid dielectric application steps which may or may not include one or more elevated baking steps in between separate spaced liquid applications.

By way of example only, Figs. 4 and 5 depict subsequent processing of the Fig. 3 substrate. Referring to Fig. 4, substrate 10 has been subjected to example substrate-side 14 polishing to effectively thin substrate 10 at least to a point of exposing via 20. Thereby in one example, via 20 extends completely through substrate 10 from substrate side 12 to substrate side 14. Prior to the thinning depicted by Fig. 4, and by way of example only, solidified dielectric 30 might be subjected to an anisotropic etch to remove material 30 from being received over passivation dielectric 18 and from over via base 24 (not shown).

Referring to Fig. 5, conductive material 32 has been formed within via 20, and a through substrate interconnect 35 has been formed therewith. Example materials 32 include any conductive material, including conductively doped semiconductive materials, elemental metals, alloys of elemental metals, and/or conductive metal compounds, including any combinations thereof. In one embodiment, a method of forming a through substrate interconnect is conducted to be void of using any chemical vapor deposition of any dielectric material to within via 20.

Figs. 4 and 5 depict one embodiment wherein example polishing of substrate side 14 occurred prior to forming of conductive material within via 20. Such could of course be reversed wherein some or all of conductive material 32 is deposited within via 20 of the Fig. 3 substrate prior to the example polishing of Fig. 4.

The above-described embodiments are by way of example only, and depict forming via 20 initially only partially into substrate 10, and including removing material of the substrate from an opposing side from which the via was initially formed to extend the via completely through the substrate from one substrate side 12 to the other substrate side 14. Such might be conducted regardless of whether substrate side 12 comprises the substrate back-side or

substrate side 14 comprises the substrate back-side. By way of example only, an alternate embodiment semiconductor substrate 10a is next described in conjunction with processing associated with Figs. 6-8. Like numerals from the first-described embodiment are utilized where appropriate, with differences being indicated with the suffix "a" or with different numerals. In one embodiment, semiconductor substrate 10a can be considered as having substrate side 12 being the back-side, and substrate side 14 as being the substrate front-side. In one embodiment, semiconductor substrate 10a can be considered as having substrate side 12 being the front-side, and substrate side 14 as being the substrate back-side. Fig. 6 depicts substrate side 14 as comprising a conductive bond pad 36, which is thereby depicted as being more proximate substrate side 14 than substrate side 12. Bond pad 36 can be considered as comprising a back-side 38. Via 20a has been formed to conductive bond pad 36 from side 12. Such might be formed partially into bond pad 36 or to extend completely therethrough (not shown). Fig. 6 depicts via 20a extending to essentially stop on via back-side 38. A liquid dielectric 30a has been applied to line at least an elevationally outermost portion of sidewalls 22 of via 20a. The Fig. 6 embodiment also depicts application of liquid dielectric 30a over back-side 38 of bond pad 36.

Referring to Fig. 7, liquid dielectric 30a has been solidified and subjected to any suitable anisotropic etch which removes material 30a from being received elevationally outward of passivation dielectric 18 and from over back-side 38 of bond pad 36.

Referring to Fig. 8, conductive material 32a has been formed within via 20a and a through substrate interconnect 35a has been formed therewith. Material composition may be as described in the above embodiments.

Additional embodiments are next described with reference to Figs. 9-12 in connection with a semiconductor substrate 10b. Like numerals from the first-described embodiments are utilized where appropriate, with differences being indicated with the suffix "b" or with different numerals. Not all embodiments of the invention require deposit of a passivation dielectric layer over a semiconductor substrate. However when utilized, the above-depicted embodiments provide but examples where a passivation dielectric layer is deposited over the side of the substrate from which the via is formed before

forming the via, and then forming the via through the passivation dielectric layer. Figs. 9-12 depict an embodiment wherein a passivation dielectric layer is deposited over the side of the substrate from which the via is at least initially formed after initially forming the via.

Referring to Fig. 9, a via 20b has been formed into semiconductive material of semiconductor substrate 10b from substrate side 12. Liquid dielectric 30b has been applied to line at least an elevationally outermost portion of sidewalls 22 of via 20b, for example using any of the materials, manners and resultant constructions as described with the above embodiments.

Referring to Fig. 10, liquid dielectric 30b has been solidified within via 20b, and a passivation dielectric 18b has been formed over substrate side 12 and at least partially over via 20b. In one embodiment and as shown, passivation dielectric 18b is formed over all of via 20b. In one embodiment and as shown, passivation dielectric 18b extends to within via 20b at least to some degree. In another embodiment, none of the passivation dielectric layer extends to within the via, for example bridging partially or wholly thereover without any lower portion thereof extending therein (not shown).

In one embodiment, the passivation dielectric layer is removed from over the via (and in one embodiment from being over and within the via), and conductive material is formed within the via over the solidified dielectric and a through substrate interconnect is formed therewith. Figs. 11 and 12 depict one such example manner of doing so. For example, Fig. 11 depicts formation of a mask 42 over passivation dielectric 18b. By way of example only, an example masking material is photoresist that is patterned using photolithographic techniques. Further, layers 42 and 18b might be of the same composition, for example photosensitive polyimide. Regardless, mask 42 is depicted as comprising an opening 43 therethrough to via 20b, and passivation dielectric 18b has been etched through opening 43 to be removed from over and from within via 20b.

Referring to Fig. 12, masking 42 (not shown) has been removed, and conductive material 32b has been formed within via 20b and a through substrate interconnect 35b has been formed with conductive material 32b. Alternately by way of example only, masking material 42 in one embodiment might remain as part of substrate 10b (not shown). Materials, methods, and constructions may

be as described with any of the above embodiments. For example and by way of example only, Fig. 12 depicts thinning of substrate 10b from substrate side 14 to expose via 20b prior to formation of conductive material 32b within via 20b. Any alternate methods are contemplated, including by way of example that described above generally in connection with Fig. 1-8.

Additional embodiments are next described in connection with Figs. 13-17 with respect to a semiconductor substrate 10d. Like numerals from the above-described embodiments are utilized where appropriate, with differences being indicated with the suffix "d" or with different numerals. The above-described examples do not require, and may be void of, any vapor deposition of dielectric material to line any portion of the depicted via after its formation. However, certain embodiments of the invention do contemplate some combination of vapor depositing of a dielectric material within a via in the fabrication of a through substrate interconnect in combination with some application of a liquid dielectric within a via in the fabrication of a through substrate interconnect. For example and by way of example only, existing and yet-to-be developed vapor deposition methods might be better capable of lining through vias having very high aspect ratios as compared to existing and yet-to-be developed liquid dielectric application techniques. In such and other instances, it might be desirable to use a combination of vapor depositing of dielectric material and liquid application of dielectric within through vias in the fabrication of through substrate interconnects. By way of example and not of limitation, another reason for doing so might be to provide vapor deposited dielectric at the base of a via while providing a liquid dielectric proximate the via opening top which has a solidified coefficient of thermal expansion which is between that of the passivation dielectric layer and the vapor deposited dielectric.

Referring to Fig. 13, a passivation dielectric 18 has been formed over substrate side 12 of semiconductor substrate 10d. A via 20 has been formed through passivation dielectric 18 and into semiconductive material of substrate 10d from substrate side 12.

Referring to Fig. 14, a dielectric material 50 has been vapor deposited over passivation dielectric 18 to line at least an elevationally outermost portion of sidewalls 22 of via 20. Any suitable dielectric material 50 might be used. In

one embodiment, the vapor depositing comprises chemical vapor depositing, and in one embodiment comprises pulsed chemical vapor depositing. One example dielectric material 50 comprises aluminum oxide, although other materials in combination with or exclusive of aluminum oxide are also of course contemplated. Dielectric material 50 might be deposited to completely line all of via sidewalls 22 as shown, or only at least an elevationally outermost portion thereof. An example thickness for vapor deposit dielectric material 50 is from about 0.1 micron to about 1 micron.

Dielectric material 50 might be recessed (for example by etching) to within the via, for example to be at or below the passivation dielectric. For example referring to Fig. 15, dielectric material 50 has been recessed to below the base of passivation dielectric 18 within via 20. In one embodiment, such recessing is conducted without any masking over substrate 10. In one embodiment, the recessing of dielectric material 50 within via 20 is such that it is received at least 2 microns elevationally inward of the base of passivation dielectric 18. Alternately by way of example only, the dielectric material 50 might be recessed to have its top coincide with the base of passivation dielectric 18 (not shown) or received elevationally outward thereof (not shown). Regardless in the depicted embodiment, such recessing of dielectric material 50 is shown as also effectively clearing it from being received atop passivation dielectric 18 and from over base 24 of via 20 between sidewall-received portions of dielectric material 50.

Referring to Fig. 16, liquid dielectric 30d has been applied over passivation dielectric 18 into via 20 at least to line an elevationally outermost portion of sidewalls 22 of via 20 above recessed dielectric material 50 and to be received over at least an elevationally outermost portion of recessed dielectric material 50 received within via 20. Example liquid dielectric materials and methods of application are as described above. Liquid dielectric 30d might be applied to completely cover over sidewalls of vapor deposited dielectric material 50 (not shown), or only partially received over an elevationally outermost portion thereof (as shown). Further, liquid dielectric material 30d may or may not cover any portion of via base 24.

The liquid dielectric is solidified within the via, and conductive material is formed therewithin over the solidified dielectric and a through substrate

interconnect is formed with the conductive material. One example resultant construction is depicted in Fig. 17 in conjunction with conductive material 32d in the fabrication of a through substrate interconnect 35d. Of course, any of the above-described attributes, methods, constructions, and materials might be used or alternately be formed.

In one embodiment, passivation dielectric 18 and dielectric material 50 are formed to have different coefficients of thermal expansion, with liquid dielectric 30d being solidified to have a coefficient of thermal expansion which is between those of passivation dielectric 18 and vapor deposited dielectric material 50. In one embodiment, liquid dielectric 30d is solidified to have a low Young's Modulus of less than or equal to approximately 2.0 GPa.

The above-described embodiment was in conjunction with conducting a recess etch of vapor deposited material 50 in going from the substrate depiction of Fig. 14 to that of Fig. 15. An alternate embodiment contemplates little or no etching of vapor deposited dielectric material 50, for example as shown in a resultant construction in Fig. 18 in conjunction with a semiconductor substrate 10e. Like numerals from the first-described embodiment are utilized where appropriate, with differences being indicated with the suffix "e" or with different numerals. Fig. 18 depicts vapor deposited dielectric material 50e as not having been recessed within via 20 prior to application and solidification of liquid dielectric 30e. Materials and manners of processing and construction can otherwise be as described in connection with all of the above embodiments.

Additional embodiment methods of forming through substrate interconnects are next described with reference to Figs. 19-21 with respect to a semiconductor substrate 10f. Like numerals from the first-described embodiment are utilized where appropriate, with differences being indicated with the suffix "f" or with different numerals. The above-described example Figs. 13-18 embodiments applied a liquid dielectric after forming a vapor deposited dielectric within a through via. Figs. 19-21 depict an alternate embodiment wherein a vapor deposited dielectric material is formed after application and solidification of a liquid dielectric material. Specifically and by way of example only, Fig. 19 depicts formation of a passivation dielectric 18 over substrate side 12, and a via 20 therethrough and into semiconductive material of substrate 10f from substrate side 12. A liquid dielectric 30f has been

applied over passivation dielectric 18 and into via 20 to line only an elevationally outermost portion of sidewalls 22 of via 20. In one embodiment, such lines no more than 50% of a combined elevational height/thickness of via 20 within passivation dielectric 18 and the depicted substrate region 16.

Referring to Fig. 20, liquid dielectric 30f is solidified and a dielectric material 50f is vapor deposited to within via 20 over solidified dielectric 30f and to line over sidewall portions 22 of via 20 that are received elevationally inward of solidified dielectric 30f within via 20. In the depicted embodiment, dielectric material 50f is completely covering of all sidewalls 22 of via 20, and also covering of all of base 24 of via 20, although such is not required. Conductive material is ultimately formed within via 20 over the vapor deposited dielectric material and solidified dielectric to form a through substrate interconnect, for example as shown in Fig. 21 of material 32f to form a through substrate interconnect 35f. Example materials, methods of construction, attributes, and other parameters can additionally or alternately be as described above. For example in one implementation, solidified spin-on dielectric 30f may be provided to have a coefficient of thermal expansion which is between that of passivation dielectric layer 18 and dielectric material 50f.

Again, all processing as described above might occur in connection with either a front-side or rear-side of a semiconductor substrate as above-defined.

The invention claimed is:

1. A method of forming a through substrate interconnect, comprising:

forming a passivation dielectric over a back-side of a semiconductor substrate;

after forming the passivation dielectric, etching through the passivation dielectric and then into semiconductive material of the substrate from the substrate back-side to form a via;

applying a liquid dielectric over the passivation dielectric and into the via to line only an elevationally outermost portion of sidewalls of the via;

solidifying the liquid dielectric within the via;

vapor depositing a dielectric material to within the via to line over the solidified dielectric within the via and to line over sidewall portions of the via received elevationally inward of the solidified dielectric within the via; and

forming conductive material within the via over the vapor deposited dielectric material and forming a through substrate interconnect with the conductive material.

2. The method of claim 1 wherein the liquid and solidified dielectric within the via lines no more than 50% of a combined elevational thickness of the passivation dielectric and the semiconductive material that forms the via.

3. The method of claim 1 wherein the solidified dielectric is thicker than the vapor deposited dielectric material.

4. The method of claim 1 wherein the liquid dielectric has a solidified coefficient of thermal expansion which is between that of the passivation dielectric and the vapor deposited dielectric.

5. The method of claim 1 wherein the vapor deposited dielectric material completely covers all sidewalls of the via elevationally inward of the solidified dielectric that is within the via.

6. The method of claim 5 wherein the via has a base, the vapor deposited dielectric material completely covering all of the via base.

7. The method of claim 6 wherein the liquid dielectric has a solidified coefficient of thermal expansion which is between that of the passivation dielectric and the vapor deposited dielectric.

8. The method of claim 1 wherein the via has a base, the vapor deposited dielectric material not completely covering at least one of a) all sidewall of the via, and b) all of the base.

9. A method of forming a through substrate interconnect, comprising:

forming a passivation dielectric over a front-side of a semiconductor substrate;

after forming the passivation dielectric, etching through the passivation dielectric and then into semiconductive material of the substrate from the substrate front-side to form a via;

applying a liquid dielectric over the passivation dielectric and into the via to line only an elevationally outermost portion of sidewalls of the via;

solidifying the liquid dielectric within the via;

vapor depositing a dielectric material to within the via to line over the solidified dielectric within the via and to line over sidewall portions of the via received elevationally inward of the solidified dielectric within the via; and

forming conductive material within the via over the vapor deposited dielectric material and forming a through substrate interconnect with the conductive material.

10. The method of claim 9 wherein the liquid and solidified dielectric within the via lines no more than 50% of a combined elevational thickness of the passivation dielectric and the semiconductive material that forms the via.

11. The method of claim 9 wherein the solidified dielectric is thicker than the vapor deposited dielectric material.

12. The method of claim 9 wherein the liquid dielectric has a solidified coefficient of thermal expansion which is between that of the passivation dielectric and the vapor deposited dielectric.

13. The method of claim 9 wherein the vapor deposited dielectric material completely covers all sidewalls of the via elevationally inward of the solidified dielectric that is within the via.

14. The method of claim 13 wherein the via has a base, the vapor deposited dielectric material completely covering all of the via base.

15. The method of claim 14 wherein the liquid dielectric has a solidified coefficient of thermal expansion which is between that of the passivation dielectric and the vapor deposited dielectric.

16. The method of claim 9 wherein the via has a base, the vapor deposited dielectric material not completely covering at least one of a) all sidewall of the via, and b) all of the base.