ABSTRACT

A semiconductor device including: a substrate including a PMOS region, an N-well tap forming region, and a boundary region; PMOS field effect transistors on the PMOS region; an N-well tap region doped with N-type impurities in the N-well tap forming region; a first metal pattern connected to at least one impurity region of the PMOS field effect transistors, wherein the first metal pattern extends so that an end of the first metal pattern is positioned on the boundary region; a second metal pattern electrically connected to the N-well tap region, wherein the second metal pattern extends so that an end of the second metal pattern is positioned on the boundary region; a first contact plug on the first metal pattern; a second contact plug on the second metal pattern; and an upper wiring on the first and second contact plugs.

FIG. 1