

CLAIMS

What is claimed is

1. A method for improving reliability of catalyst influenced chemical etching, the method comprising:
 - patterning a catalyst layer on a surface of a semiconducting material, wherein said catalyst layer comprises a plurality of features and lithographic links between two or more of the plurality of features;
 - exposing said patterned catalyst layer on said surface of said semiconducting material to an etchant, wherein said patterned catalyst layer causes etching of said semiconducting material to form fabricated structures corresponding to the plurality of features and gaps corresponding to the links; and
 - depositing material sufficient to fill said gaps.
2. The method as recited in claim 1, wherein said lithographic links have connecting lines that join substantially isolated nodes of said catalyst layer.
3. The method as recited in claim 1, wherein said lithographic links in said patterned catalyst layer result in missing portions of high aspect ratio structures, and the method further comprises filling the missing portions with SiO₂, SiN, epitaxial Si, W, TiN, or carbon.
4. The method as recited in claim 1, wherein the material is one of the following:
 - single crystal bulk silicon wafer, a layer of polysilicon of thickness greater than 100nm deposited on a substrate, a layer of amorphous silicon of thickness greater than 100nm deposited on a substrate, an SOI (silicon on insulator) wafer, or a layer of epitaxial silicon of thickness greater than 100nm on a substrate.
5. The method as recited in claim 1, wherein the material comprises alternating layers of semiconductor materials of varying doping levels and dopants, highly doped silicon and lightly doped silicon, undoped silicon and doped silicon or germanium, Silicon and Si_xGe_{1-x}, differently doped silicon and/or Si_xGe_{1-x}, differently doped silicon and/or Ge, or Si and Ge.
6. The method as recited in claim 5, wherein the fabricated structures have periodic variations in at least one of porosity, pore size, pore orientation, etch rate, or thermal processing rates.
7. The method as recited in claim 5, wherein a thickness of each alternating layer is between 1 nm and 100nm.

- 1 8. The method as recited in claim 5, wherein at least one of the alternating layers is selectively
2 removed.
- 3 9. The method as recited in claim 8, wherein $\text{Si}_x\text{Ge}_{1-x}$ layers are removed by HCl to create Si
4 nanosheets and/or lateral nanowires.
- 5 10. The method as recited in claim 5, wherein one of the doped layers of silicon becomes porous
6 in the presence of the etchant used in CICE.
- 7 11. The method as recited in claim 10, wherein the porous Si layers are removed using HF, HF
8 vapor, HF and a weak oxidant, KOH or TMAH.
- 9 12. The method as recited in claim 1, wherein said catalyst layer sinks into the semiconducting
10 material in the presence of an etchant.
- 11 13. The method as recited in claim 1, wherein said etchant comprises at least two of the following:
12 fluoride species containing chemicals HF or NH_4F ;
13 oxidants H_2O_2 , KMnO_4 , or dissolved oxygen;
14 alcohols ethanol, isopropyl alcohol, or ethylene glycol; or
15 protic, aprotic, polar and non-polar solvents such as DI water, or dimethyl sulfoxide (DMSO).
- 16 14. The method of claim 1, wherein the semiconducting material can be Ge, GaAs, GaN, Si, SiC,
17 SiGe, InGaAs, and other Group IV, III-V, II-V elements or compounds.
- 18 15. The method of claim 1, wherein the catalyst layer comprises one or more of the following: Au,
19 Pt, Pd, Ru, Ag, Cu, Ni, W, TiN, TaN, RuO_2 , IrO_2 , or Graphene.
- 20 16. The method as recited in claim 1, wherein the fabricated structures have at least one lateral
21 dimension that is less than 100nm; and an aspect ratio of height of features to minimum lateral
22 dimension that is at least 5:1.
- 23 17. The method as recited in claim 1, wherein a time varying electric field is used to produce
24 alternating layers of etched nanostructures wherein at least one of the alternating layers is
25 porous.
- 26 18. The method as recited in claim 17, wherein the fabricated structures have periodic variations
27 in at least one of the following: porosity, pore size, pore orientation, etch rate and thermal
28 processing rates.
- 29 19. The method as recited in claim 17, wherein the porous Si layers are removed using HF, HF
30 vapor, HF and a weak oxidant, KOH or TMAH.
- 31 20. The method in claim 1, wherein the resulting structures after modifying the connecting links
32 are used for subsequent formation of finFETs, lateral nanowire FETs or nanosheet FETs.
- 33 21. The method in claim 20, wherein a dielectric is deposited and a timed chemical etch is used
34 to create a shallow trench isolation for bulk finFETs or nanosheet FETs.

- 1 22. The method as recited in claim 1, wherein said semiconducting structures are used to make
2 DRAM cells.
- 3 23. The method as recited in claim 1, wherein said semiconducting structures are used to make
4 3D NAND Flash.
- 5 24. A method for preventing substantial collapse of high aspect ratio semiconducting structures
6 by catalyst influenced chemical etching, the method comprising:
7 patterning a catalyst layer on a surface of a semiconducting material, wherein said catalyst
8 layer comprises a plurality of features and lithographic gaps between two or more of the
9 plurality of features;
10 exposing said patterned catalyst layer on said surface of said semiconducting material to an
11 etchant, wherein said patterned catalyst layer causes etching of said semiconducting
12 material to form structures corresponding to the plurality of features and links
13 corresponding to the gaps; and
14 modifying one or more of said links.
- 15 25. The method as recited in claim 24, wherein said lithographic links in said interconnected high
16 aspect ratio structures are selectively modified by one or more of the following methods:
17 oxidation, nitridation, selective etch, lithography with precise alignment and plasma etch of
18 certain portions of the links.
- 19 26. The method as recited in claim 24, wherein the material is one of the following:
20 single crystal bulk silicon wafer, a layer of polysilicon of thickness greater than 100nm
21 deposited on a substrate, a layer of amorphous silicon of thickness greater than 100nm
22 deposited on a substrate, an SOI (silicon on insulator) wafer, a layer of epitaxial silicon
23 of thickness greater than 100nm on a substrate.
- 24 27. The method as recited in claim 24, wherein the material comprises alternating layers of
25 semiconductor materials of varying doping levels and dopants, highly doped silicon and lightly
26 doped silicon, undoped silicon and doped silicon or germanium, Silicon and $\text{Si}_x\text{Ge}_{1-x}$,
27 differently doped silicon and/or $\text{Si}_x\text{Ge}_{1-x}$, differently doped silicon and/or Ge, or Si and Ge.
- 28 28. The method as recited in claim 24, wherein the material comprises alternating layers of
29 semiconductor material wherein the semiconducting materials have varying doping levels
30 and dopants, highly doped silicon, lightly doped silicon, undoped silicon, doped silicon and
31 germanium, silicon and $\text{Si}_x\text{Ge}_{1-x}$, differently doped silicon, and/or $\text{Si}_x\text{Ge}_{1-x}$, with differently
32 doped silicon and/or Ge, or Si and Ge.
- 33

- 1 29. The method as recited in claim 28, wherein the fabricated structures have periodic variations
2 in at least one of the following- porosity, pore size, pore orientation, etch rate and thermal
3 processing rates.
- 4 30. The method as recited in claim 28, wherein the thickness of each layer is between 1nm and
5 100nm.
- 6 31. The method as recited in claim 28, wherein at least one of the set of alternating layers is
7 selectively removed.
- 8 32. The method as recited in claim 31, wherein $\text{Si}_x\text{Ge}_{1-x}$ layers are removed by HCl to create Si
9 nanosheets and/or lateral nanowires.
- 10 33. The method as recited in claim 28, wherein one of the doped layers of silicon becomes porous
11 in the presence of the etchant used in CICE.
- 12 34. The method as recited in claim 33 wherein the porous Si layers are removed using HF, HF
13 vapor, HF and a weak oxidant, KOH or TMAH.
- 14 35. The method as recited in claim 24, wherein said catalyst layer sinks into the semiconducting
15 substrate in the presence of an etchant.
- 16 36. The method as recited in claim 24, wherein said etchant comprises at least two of the
17 following:
18 fluoride species including HF or NH_4F ;
19 oxidants including H_2O_2 , KMnO_4 , or dissolved oxygen;
20 alcohols including ethanol, isopropyl alcohol, or ethylene glycol; or
21 protic, aprotic, polar and non-polar solvents including DI water, or dimethyl sulfoxide (DMSO).
- 22 37. The method of claim 24, wherein the semiconducting material can be Ge, GaAs, GaN, Si,
23 SiC, SiGe, InGaAs, and other Group IV, III-V, II-V elements or compounds.
- 24 38. The method of claim 24 where the catalyst layer comprises one or more of the following: Au,
25 Pt, Pd, Ru, Ag, Cu, Ni, W, TiN, TaN, RuO_2 , IrO_2 , or Graphene.
- 26 39. The method as recited in claim 24, wherein the fabricated structures have at least one lateral
27 dimension that is less than 100nm; and an aspect ratio of height of features to minimum lateral
28 dimension that is at least 5:1.
- 29 40. The method as recited in claim 24, wherein a time varying electric field is used to produce
30 alternating layers of etched nanostructures wherein at least one of the alternating layers is
31 porous.
- 32 41. The method as recited in claim 40, wherein the fabricated structures have periodic variations
33 in at least one of the following- porosity, pore size, pore orientation, etch rate and thermal
34 processing rates.

- 1 42. The method as recited in claim 40, wherein the porous Si layers are removed using HF, HF
2 vapor, HF and a weak oxidant, KOH or TMAH.
- 3 43. The method in claim 24, wherein the resulting structures after modifying the connecting links
4 are used for subsequent formation of finFETs, lateral nanowire FETs or nanosheet FETs.
- 5 44. The method in claim 43, wherein a dielectric is deposited and a timed chemical etch is used
6 to create a shallow trench isolation for bulk finFETs or nanosheet FETs.
- 7 45. The method as recited in claim 24, wherein said semiconducting structures are used to make
8 DRAM cells.
- 9 46. The method as recited in claim 24, wherein said semiconducting structures are used to make
10 3D NAND Flash.
- 11 47. A method for preventing substantial collapse of high aspect ratio semiconducting structures
12 by catalyst influenced chemical etching, the method comprising:
13 creating a support structure by depositing a material on either a patterned catalyst layer or
14 across two or more uncollapsed semiconductor structures; and
15 exposing said support structure to an etchant to form higher aspect ratio semiconductor
16 structures with said material to prevent substantial collapse of said higher aspect ratio
17 said semiconducting structures.
- 18 48. The method as recited in claim 47, wherein said uncollapsed semiconductor structures are
19 made from one or more of the following processes: plasma etch, dry etch, chemical etch and
20 catalyst influenced chemical etching.
- 21 49. The method as recited in claim 47, wherein a substrate of said structure comprises one or
22 more layers of semiconducting films.
- 23 50. The method as recited in claim 47, wherein said material is resistant to etchant material that
24 includes Cr, polymer, carbon, Cr_2O_3 , or Al_2O_3 .
- 25 51. The method of claim 47, where the material is deposited either at the top or along the length
26 of the structures.
- 27 52. The method of claim 51, wherein the material deposition location is at a height of L/N from the
28 top of the uncollapsed structures, where L is the height of the said structures and N is a
29 number that is greater than or equal to 1, and is determined by height stability mechanics to
30 avoid collapse.

- 1 53. The method as recited in claim 47, wherein said material is made porous either during
2 deposition or after exposure to said etchant.
- 3 54. The method as recited in claim 47, wherein the capping material is patterned to ensure etchant
4 flow to catalyst film during CICE.
- 5 55. The method as recited in claim 47, wherein voids between said high aspect ratio
6 semiconducting structures are filled with second material.
- 7 56. The method in claim 55, wherein the support structure material is selectively removed after
8 further filling with second material.
- 9 57. The method as recited in claim 56, wherein said structure is used to make DRAM cells.
- 10 58. The method as recited in claim 56, wherein said structure is used to make 3D NAND flash
11 arrays with vertical channels.
- 12 59. An apparatus for catalyst influenced chemical etching, comprising:
13 a process chamber to house a semiconductor wafer which comprises a catalyst on at least
14 one surface of the semiconductor wafer and an etchant;
15 a plurality of actuators configured to control environmental properties within the process
16 chamber;
17 a control system to control rate of catalyst influenced etching across the semiconductor wafer
18 by adjusting the one or more environmental properties via the plurality of actuators; and
19 a rinsing station to remove the etchant.
- 20 60. The apparatus as recited in claim 59, wherein environmental properties include temperature,
21 vapor pressure, electric field, etchant concentration, etchant composition and illumination.
- 22 61. The apparatus as recited in claim 59, wherein the rinsing station is the same as the process
23 chamber.
- 24 62. The apparatus as recited in claim 59, wherein the rinsing occurs in a separate apparatus.
- 25 63. The apparatus as recited in claim 59, wherein the rinsing is done using DI water to remove all
26 the etchant chemicals from the substrate after the etch is completed, and the substrate is dried
27 using dry heated nitrogen or clean dry air.
- 28 64. The apparatus as recited in claim 59, further comprising a plurality of sensors to detect the
29 etch state.

- 1 65. The apparatus as recited in claim 64, wherein said etch state comprises one or more of the
2 following: an etch depth, a material porosity, number of alternating layers etched, electrical
3 conductivity of doped semiconducting material in contact with an etchant, optical properties of
4 features, and electrical properties of features measured during and/or after the etching
5 process.
- 6 66. The apparatus in claim 59, further comprising a send ahead wafer that is processed through
7 the equipment and an offline metrology system to sense etch state of the send ahead wafer.
- 8 67. The apparatus of claim 66, wherein the offline metrology estimates process excursions
9 noticed in the send ahead wafer.
- 10 68. The apparatus as recited in claim 59, further comprising a drying mechanism configured to
11 transfer fluid to enable a surface tension gradient to prevent collapse of high aspect ratio
12 structures.
- 13 69. The apparatus as recited in claim 59 wherein the local and/or global etch depth is monitored
14 using one or more of the following:
- 15 local electric field measurements based on voltage, current, capacitance, resistance, or
16 inductance;
- 17 optical measurements using cameras, optic cables or spectrophotometers and image
18 processing; or
- 19 thermal measurements using thermal chucks or micromirrors.
- 20 70. The apparatus as recited in claim 69, wherein the optical measurement is performed at IR
21 wavelength that allows process monitoring through the silicon.
- 22 71. The apparatus as recited in claim 59 wherein the local and/or global etch depth is controlled
23 using one or more of the following:
- 24 local electrodes to apply AC or DC electric fields of desired waveforms, amplitudes,
25 frequencies, with multiple coinciding electric fields to avoid edge effects and leakage;
- 26 local illumination of the front or back of the substrate being etched using laser and light
27 sources of desired wavelengths;
- 28 temperature changes in local regions to even out etch depth variations using thermal chucks
29 or micromirrors; or

1 varying local etchant concentrations using inkjets and jetting blocking or enhancing etchant
2 components or air bubbles to modify etch rates locally.

3 72. The apparatus as recited in claim 54 wherein the local and/or global etchant concentrations
4 are monitored during catalyst influenced chemical etching using:
5 refractive index measurement of the etchant solution; or
6 conductance of the etchant solution.

7 73. The apparatus as recited in claim 59 wherein the local and/or global etchant
8 concentrations are controlled during catalyst influenced chemical etching using:
9 flow control and circulation of etchant;
10 spinning of the substrate;
11 diffuser to create uniform etchant concentrations;
12 temperature gradients for diffusion of etchants;
13 local addition of chemicals to drive diffusion of etchants;
14 acoustic streaming;
15 jetting of air; or
16 local addition of depleting components of etchant.

17 74. The apparatus as recited in claim 59, comprising components for monitoring and control of
18 local and/or global temperature wherein:
19 micromirrors are used to heat wafers from front or back;
20 electrodes are used to locally heat the solution above the die; or
21 individual "wells" for each die which are filled with finite volume of etchant and pumped
22 out/circulated have controlled temperatures.

23 75. The apparatus in claim 59, wherein the etchant solution is maintained at low temperatures for
24 near-zero etch rate, and local heating is used to start/control/stop etch per die.

25 76. The apparatus as recited in claim 59, comprising components for monitoring and control of
26 local and/or global electric fields wherein:
27 an electric field array mechanism configured to control an etching profile in real-time when an
28 electric bias is applied to a semiconductor substrate; and

1 an inline electrical metrology and electrochemical etch stop mechanism configured to
2 measure current and voltage across said semiconductor substrate as the etch
3 progresses to determine a number of alternating layers etched in a device or as an etch
4 stop indicator for nanostructure etching.

5 77. The apparatus as recited in claim 59, comprising components for monitoring and control of
6 local and/or global electric fields wherein:

7 a patterned bottom electrode is used whose design is based on a catalyst pattern;

8 electric fields are used for making alternating porous/non-porous layers;

9 global/local electric fields are used to prevent wandering of catalyst;

10 the electric fields may have square waveforms at a certain wavelength, frequency and duty
11 cycle;

12 the electrodes are patterned in the tool on the front or backside of the wafer;

13 the electrodes are patterned on the front, back, or between the front and back surfaces of a
14 wafers, for instance in an SOI wafer;

15 an electrical contact is made to the wafer using a metal brush with contact outside O-ring;

16 local variations from edge to center are controlled via pulsed electric fields; or

17 etch uniformity and depth is monitored across wafer by measurement of I, V, R, C in each
18 local electrode.

19 78. The apparatus as recited in claim 59 wherein inkjets are configured to dispense etchant fluids
20 on a portion of said semiconducting material.

21 79. The apparatus as recited in claim 78, wherein said inkjets dispense etchant components at
22 locations that require etching.

23 80. The apparatus as recited in claim 79, wherein said locations that require etching are isolated
24 by walls of etchant resistant material that includes a patterned photoresist, Cr, polymer, or
25 Al_2O_3 , that are later removed.

26 81. The apparatus as recited in claim 59, wherein the catalyst influenced chemical etching
27 process is done by:

28 alternately pulsing H_2O_2 vapor and HF vapor;

29 alternately pulsing H_2O_2 liquid and HF liquid;

- 1 alternately pulsing H₂O₂ vapor and HF liquid;
2 alternately pulsing H₂O₂ liquid and HF vapor; or
3 using stronger oxidant for porous layers and weaker oxidant for non-porous layers.
- 4 82. The apparatus as recited in claim 59 wherein the etchants are in vapor or ionic form, the
5 apparatus comprising:
6 control of local temperatures using a thermal chuck;
7 monitoring of vapor pressure of each component; and
8 applying an electric field in the form of a plasma.
- 9 83. The apparatus as recited in claim 59, for catalyst influenced chemical etching arranges all the
10 components for monitoring and control such that:
11 the setup can etch industry standard wafers or wafers that can go through standard CMOS
12 processes;
13 the setup provides for automated handling of all substrates, etch components and chemicals;
14 the components are arranged alongside other portions of the tool and include local and/or
15 global components for electric field monitoring and control;
16 the components are arranged to accommodate electric field components, inkjets and
17 temperature control components; and
18 the setup is compatible with the etchant chemicals.
- 19 84. A method for making alternating multilayer nanostructures, the method comprising:
20 providing a semiconducting material;
21 patterning a catalyst layer on a surface of said semiconducting material;
22 exposing said patterned catalyst layer to an etchant, wherein said patterned catalyst layer and
23 said etchant cause etching of semiconducting material to form vertical nanostructures;
24 exposing said semiconducting material to a time-varying electric field to produce alternating
25 layers of etched nanostructures wherein at least one of the alternating layers is porous;
26 filling a second material in at least a portion of the nanostructures; and
27 selectively processing one of the alternating layers to either change its chemical composition
28 or remove it.

- 1 85. The method as recited in claim 84, wherein the material is single crystal bulk silicon wafer, a
2 layer of polysilicon of thickness greater than 100nm deposited on a substrate, a layer of
3 amorphous silicon of thickness greater than 100nm deposited on a substrate, an silicon on
4 insulator (SOI) wafer, a layer of epitaxial silicon of thickness greater than 100nm on a
5 substrate.
- 6 86. The method as recited in claim 84 wherein said catalyst layer comprises an intended design
7 and lithographic links, wherein said lithographic links substantially connect two or more
8 isolated features of said catalyst layer and/or said semiconducting material.
- 9 87. The method as recited in claim 86, wherein said lithographic links have connecting lines that
10 join substantially isolated nodes of said catalyst layer.
- 11 88. The method as recited in claim 84, wherein the dimensions of the intended design are
12 corrected for thickness of oxide layer during post-processing of the etched material after SiSE.
- 13 89. The method in claim 84, where the pattern is designed using a predefined method to generate
14 the connecting links.
- 15 90. The method in claim 84, where the patterns can be lines and spaces, circles, and arbitrary
16 linked patterns.
- 17 91. The method in claim 84, that are fabricated using one or more of the following: electron beam
18 lithography, imprint lithography, photolithography, directed self-assembly.
- 19 92. The method in claim 91, wherein different electron beam patterns are aligned by
20 photolithography or imprint lithography to form a master pattern.
- 21 93. The method in claim 92, wherein the master pattern is replicated onto the semiconducting
22 substrates using imprint lithography.
- 23 94. The method in claim 84, wherein the pattern is designed based on 3D NAND Flash cell array
24 architectures.
- 25 95. The method in claim 84, wherein the resulting structures with alternating layers are used for
26 subsequent formation of lateral nanowire FETs or nanosheet FETs.
- 27 96. The method of claim 86, wherein the links in interconnected high aspect ratio structures are
28 modified by one or more of the following: oxidation, nitridation and selective etch; to provide
29 substantially free-standing semiconducting structures without collapse.
- 30 97. The method of claim 87, wherein additional material is filled around the interconnected high
31 aspect ratio structures to make high aspect ratio isolated trenches.

- 1 98. The method as recited in claim 84 further comprising:
2 designing a catalyst pattern to substantially prevent process excursions, wherein said process
3 excursions comprise a collapse of high aspect ratio nanostructures and wandering of isolated
4 catalyst.
- 5 99. The method as recited in claim 84, wherein said catalyst layer sinks into the semiconducting
6 substrate in the presence of an etchant.
- 7 100. The method as recited in claim 84, wherein said etchant comprises at least two of the
8 following:
9 fluoride species containing chemicals HF or NH_4F ;
10 oxidants including H_2O_2 , KMnO_4 or dissolved oxygen;
11 alcohols including ethanol, isopropyl alcohol, or ethylene glycol; or
12 protic, aprotic, polar and non-polar solvents including DI water, or dimethyl sulfoxide (DMSO).
- 13 101. The method of claim 84, wherein the semiconducting material can be Ge, GaAs, GaN, Si,
14 SiC, SiGe, InGaAs, and other Group IV, III-V, II-V elements or compounds.
- 15 102. The method of claim 84, wherein the catalyst material comprises one or more of the following:
16 Au, Pt, Pd, Ru, Ag, Cu, Ni, W, TiN, TaN, RuO_2 , IrO_2 , or Graphene.
- 17 103. The method as recited in claim 84, wherein an electric field on the semiconducting substrate
18 with modulated current densities as well as a catalyst layer cause periodic portions of the
19 semiconducting substrate to become porous in the presence of the etchant.
- 20 104. The method as recited in claim 84, wherein at least one of the alternating layers has a
21 porosity less than 10%.
- 22 105. The method as recited in claim 84, wherein at least one of the alternating layers has a
23 porosity less than 1%.
- 24 106. The method as recited in claim 84, wherein at least one of the alternating layers has a
25 porosity less than 0.1%.
- 26 107. The method as recited in claim 84, wherein the catalyst layer causes periodic portions of the
27 semiconducting substrate adjacent to the catalyst to become porous in the presence of an
28 etchant.

- 1 108. The method as recited in claim 84, wherein the porous portions of the semiconducting
2 substrate enhance diffusion of the etchant reactants and products.
- 3 109. The method as recited in claim 84, wherein the fabricated structures have at least one lateral
4 dimension that is less than 100nm.
- 5 110. The method as recited in claim 84, wherein the fabricated structures have periodic variations
6 in at least one of the following- porosity, pore size, pore orientation, etch rate and thermal
7 processing rates.
- 8 111. The method as recited in claim 84, wherein the alternating multilayers have a total thickness
9 greater than 100nm.
- 10 112. The method of claim 84, wherein non-collapsing alternating multilayer nanostructures are
11 used for 3D NAND Flash.
- 12 113. The method of claim 84, wherein the porous alternating layers have porosities that enable
13 thermal processing without substantial stresses.
- 14 114. The method as recited in claim 113 further comprising:
15 oxidizing said etched material stack such that porous layers of said two or more layers of
16 alternating semiconducting films become completely oxidized and non-porous layers of said
17 two or more layers of alternating semiconducting films develop a thin oxide wall.
- 18 115. The method as recited in claim 114, where the non-porous alternating layers have a porosity
19 less than 10%.
- 20 116. The method as recited in claim 115, wherein the non-porous layers are resistant to thermal
21 processing with respect to porous layers.
- 22 117. The method as recited in claim 115, wherein the non-porous layers are resistant to etchant
23 chemicals used to selectively remove porous layers.
- 24 118. The method of claim 113, where the porous alternating layers have porosities that enable
25 oxidation without substantial increase in volumes.
- 26 119. The method of claim 113, where the porous alternating layers have porosities that enable
27 nitridation without substantial increase in volumes.
- 28 120. The method of claim 113, where material is deposited in specific regions of the high aspect
29 ratio nanostructures by lithography, deposition and etching.

- 1 121. The method of claim 120, wherein one of the alternating layers is selectively removed, with
2 an etch selectivity greater than 10:1.
- 3 122. The method of claim 120, wherein one of the alternating layers is selectively removed, with
4 an etch selectivity greater than 50:1.
- 5 123. The method of claim 120, where a material is deposited to replace the alternating layer that
6 was selectively removed.
- 7 124. The method as recited in claim 123, wherein said deposited material for conducting lines
8 comprises one or more of the following: tantalum nitride, tungsten, titanium, cobalt, copper
9 and nickel.
- 10 125. The method as recited in claim 123, wherein said deposited material for insulating lines
11 comprises one of the following: silicon dioxide, silicon nitride, low-k dielectrics.
- 12 126. The method of claim 120, wherein the alternating layers are of porous and non-porous
13 silicon, and the porous silicon layers are removed using alkaline etchants including TMAH and
14 KOH, or fluoride based chemistries or with fluoride based chemistries and mild oxidants.
- 15 127. The method of claim 124, wherein the alternating layers are of a conducting material and
16 non-porous silicon, and the non-porous silicon layers are removed using alkaline etchants
17 including TMAH and KOH, or with fluoride-based chemistries and oxidants.
- 18 128. The method of claim 117, wherein the alternating layers are of a porous silicon oxide and
19 non-porous silicon, and the porous silicon oxide layers are removed using fluoride-based
20 etchants in liquid or vapor form, including HF and buffered HF.
- 21 129. The method as recited in claim 126 further comprising:
22 selectively depositing gate and conducting line materials on said non-porous layers and
23 annealed to form silicides for conducting lines.
- 24 130. The method as recited in claim 129, wherein said gate and conducting line materials
25 comprise one of the following: tantalum nitride, tungsten, titanium, cobalt and nickel.
- 26 131. The method as recited in claim 115 further comprising:
27 depositing memory film and oxide core filler in channel while protecting word line slits.
- 28 132. The method as recited in claim 131, wherein said memory film comprises a tri-layer of
29 silicon oxide, silicon nitride and silicon oxide, and a core of polysilicon with or without doping,
30 and an insulator such as silicon oxide.

- 1 133. A method for making substantially non-collapsing alternating multi-layer stacked
2 nanostructures, the method comprising:
3 creating a material stack comprising two or more layers of alternating semiconducting films,
4 wherein each of said two or more layers of alternating semiconducting films is different
5 from another in at least one of the following properties: material, doping concentration
6 and dopant material;
7 etching said material stack by catalyst influenced chemical etching such that layers differing
8 in said properties produce etched nanostructures differing in at least one of the following:
9 morphology, porosity, etch rates and thermal processing rates;
10 filling a second material in at least a portion of the nanostructures; and
11 selectively processing one of the alternating layers to either change a chemical composition
12 or remove one of the alternating layers.
- 13 134. The method of claim 133, wherein the material comprises alternating layers of semiconductor
14 materials, wherein the semiconducting materials have varying doping levels and dopants,
15 highly doped silicon, lightly doped silicon, undoped silicon, doped silicon and germanium,
16 silicon and $\text{Si}_x\text{Ge}_{1-x}$, differently doped silicon and/or $\text{Si}_x\text{Ge}_{1-x}$, differently doped silicon and/or
17 Ge, or Si and Ge.
- 18 135. The method of claim 133 wherein said catalyst layer comprises an intended design and
19 lithographic links, wherein said lithographic links substantially connect one or more isolated
20 features of said catalyst layer and/or said semiconducting material.
- 21 136. The method of claim 135, wherein said lithographic links have connecting lines that join
22 substantially isolated nodes of said catalyst layer.
- 23 137. The method of claim 133, wherein the dimensions of the intended design are corrected for
24 thickness of oxide layer during post-processing of the etched material after SiSE.
- 25 138. The method of claim 133, wherein the pattern is designed using a predefined method to
26 generate the connecting links.
- 27 139. The method of claim 133, wherein the patterns can be lines and spaces, circles, and arbitrary
28 linked patterns.
- 29 140. The method of claim 133, that are fabricated using one or more of the following: electron
30 beam lithography, imprint lithography, photolithography, directed self-assembly.

- 1 141. The method of claim 140, wherein different electron beam patterns are aligned by
2 photolithography or imprint lithography to form a master pattern.
- 3 142. The method of claim 141, wherein the master pattern is replicated onto the semiconducting
4 substrates using imprint lithography.
- 5 143. The method of claim 133, wherein the pattern is designed based on 3D NAND Flash cell
6 array architectures.
- 7 144. The method of claim 133, wherein the resulting structures with alternating layers are used
8 for subsequent formation of lateral nanowire FETs or nanosheet FETs.
- 9 145. The method of claim 135, wherein the links in interconnected high aspect ratio structures are
10 modified by one or more of the following: oxidation, nitridation and selective etch; to provide
11 substantially free-standing semiconducting structures without collapse.
- 12 146. The method of claim 136, wherein additional material is filled around the interconnected high
13 aspect ratio structures to make high aspect ratio isolated trenches.
- 14 147. The method of claim 133 further comprising:
15 designing a catalyst pattern to substantially prevent process excursions, wherein said
16 process excursions comprise a collapse of high aspect ratio nanostructures and
17 wandering of isolated catalyst.
- 18 148. The method of claim 133, wherein said catalyst layer sinks into the semiconducting substrate
19 in the presence of an etchant.
- 20 149. The method of claim 133, wherein said etchant comprises at least two of the following:
21 fluoride species containing chemicals including HF or NH₄F;
22 oxidants including H₂O₂, KMnO₄, or dissolved oxygen;
23 alcohols including ethanol, isopropyl alcohol, or ethylene glycol; or
24 protic, aprotic, polar and non-polar solvents including DI water, or dimethyl sulfoxide (DMSO).
- 25 150. The method of claim 133, wherein the semiconducting material can be Ge, GaAs, GaN, Si,
26 SiC, SiGe, InGaAs, and other Group IV, III-V, II-V elements or compounds.
- 27 151. The method of claim 133, wherein the catalyst material comprises one or more of the
28 following: Au, Pt, Pd, Ag, Cu, Ni, W, TiN, or Graphene.
- 29 152. The method as recited in claim 133, wherein an electric field is used to improve process
30 control and etch uniformity across the substrate.

- 1 153. The method of claim 133, wherein at least one of the alternating layers has a porosity less
2 than 10%.
- 3 154. The method of claim 133, wherein at least one of the alternating layers has a porosity less
4 than 1%.
- 5 155. The method of claim 133, wherein at least one of the alternating layers has a porosity less
6 than 0.1%.
- 7 156. The method of claim 133, wherein the catalyst layer causes periodic portions of the
8 semiconducting substrate adjacent to the catalyst to become porous in the presence of an
9 etchant.
- 10 157. The method of claim 133, wherein the porous portions of the semiconducting substrate
11 enhance diffusion of the etchant reactants and products.
- 12 158. The method of claim 133, wherein the fabricated structures have at least one lateral
13 dimension that is less than 100nm.
- 14 159. The method of claim 133, wherein the fabricated structures have periodic variations in at
15 least one of the following- porosity, pore size, pore orientation, etch rate and thermal
16 processing rates.
- 17 160. The method of claim 133, wherein the alternating multilayers have a total thickness greater
18 than 100nm.
- 19 161. The method of claim 133, where non-collapsing alternating multilayer nanostructures are
20 used for 3D NAND Flash.
- 21 162. The method of claim 133, where the porous alternating layers have porosities that enable
22 thermal processing without substantial stresses.
- 23 163. The method of claim 162 further comprising:
24 oxidizing said etched material stack such that porous layers of said two or more layers of
25 alternating semiconducting films become completely oxidized and non-porous layers of said
26 two or more layers of alternating semiconducting films develop a thin oxide wall.
- 27 164. The method of claim 163, where the non-porous alternating layers have a porosity less than
28 10%.
- 29 165. The method of claim 164, wherein the non-porous layers are resistant to thermal processing
30 with respect to porous layers.

- 1 166. The method of claim 164, wherein the non-porous layers are resistant to etchant chemicals
2 used to selectively remove porous layers.
- 3 167. The method of claim 162, where the porous alternating layers have porosities that enable
4 oxidation without substantial increase in volumes.
- 5 168. The method of claim 162, where the porous alternating layers have porosities that enable
6 nitridation without substantial increase in volumes.
- 7 169. The method of claim 162, where material is deposited in specific regions of the high aspect
8 ratio nanostructures by lithography, deposition and etching.
- 9 170. The method of claim 169, wherein one of the alternating layers is selectively removed, with
10 an etch selectivity greater than 10:1.
- 11 171. The method of claim 169, wherein one of the alternating layers is selectively removed, with
12 an etch selectivity greater than 50:1.
- 13 172. The method of claim 169, where a material is deposited to replace the alternating layer that
14 was selectively removed.
- 15 173. The method of claim 172, wherein said deposited material for conducting lines comprises
16 one of the following: tantalum nitride, tungsten, titanium, cobalt, copper and nickel.
- 17 174. The method of claim 172, wherein said deposited material for insulating lines comprises one
18 of the following: silicon dioxide, silicon nitride, low-k dielectrics.
- 19 175. The method of claim 169, where the alternating layers are of porous and non-porous silicon,
20 and the porous silicon layers are removed using alkaline etchants including TMAH and KOH,
21 with fluoride-based chemistries or with fluoride based chemistries and mild oxidants.
- 22 176. The method of claim 173, where the alternating layers are of a conducting material and non-
23 porous silicon, and the non-porous silicon layers are removed using alkaline etchants
24 including TMAH and KOH, or with fluoride-based chemistries and oxidants.
- 25 177. The method of claim 166, where the alternating layers are of a porous silicon oxide and non-
26 porous silicon, and the porous silicon oxide layers are removed using fluoride-based etchants
27 in liquid or vapor form, including HF or buffered HF.
- 28 178. The method of claim 175, further comprising:
29 selectively depositing gate and conducting line materials on said non-porous layers and
30 annealed to form silicides for conducting lines.

- 1 179. The method of claim 178, wherein said gate and conducting line materials comprise one
2 of the following: tantalum nitride, tungsten, titanium, cobalt and nickel.
- 3 180. The method of claim 163 further comprising:
4 depositing memory film and oxide core filler in channel while protecting word line slits.
- 5 181. The method of claim 180, wherein said memory film comprises a tri-layer of silicon oxide,
6 silicon nitride and silicon oxide, and a core of polysilicon with or without doping, and an
7 insulator such as silicon oxide.
- 8 182. A method for making alternating multilayer structures, the method comprising:
9 providing a semiconductor substrate;
10 etching a semiconductor substrate at taper with an angle less than 80 degrees;
11 further, catalyst influenced chemical etching of the semiconductor substrate to create
12 alternating layers with different porosities; and
13 etching said taper to reveal one of said two or more alternating layers while etching part of
14 another layer to create a staircase structure.
- 15 183. The method of claim 182, wherein said staircase structure is used to create contacts to
16 conducting layers of a 3D NAND flash device.
- 17 184. The method of claim 182, wherein the material is one of the following:
18 a single crystal bulk silicon wafer, a layer of polysilicon of thickness greater than 100nm
19 deposited on a substrate, a layer of amorphous silicon of thickness greater than 100nm
20 deposited on a substrate, an silicon on insulator (SOI) wafer, or a layer of epitaxial silicon of
21 thickness greater than 100nm on a substrate.
- 22 185. The method of claim 182, wherein the material comprises alternating layers of semiconductor
23 materials and wherein the semiconducting materials include varying doping levels and
24 dopants, two or more layers of alternating semiconducting films comprise silicon and
25 germanium, highly doped silicon/lightly doped silicon or undoped silicon/ doped
26 silicon/germanium.
- 27 186. The method of claim 182, wherein the semiconductor material is etched along a crystal plane
28 using a crystallographic dependent etch with an etchant comprising one of the following: KOH,
29 TMAH, NH₄OH, EDP.
- 30 187. The method of claim 182, wherein the semiconductor material is etched with plasma at an
31 angle to the substrate using faraday cages.

- 1 188. The method of claim 182, wherein said staircase structure is used to create contacts to
2 conducting layers of a 3D NAND flash device.
- 3 189. The method of claim 182, wherein the minimum thickness of at least one set of the alternating
4 layers is defined by the requirements of lithographic overlay, resistance of the contacts, and
5 lithographic resolution.
- 6 190. The method of claim 189, wherein the thickness of the insulating layers is 3 times more than
7 the thickness of the conducting layer.
- 8 191. The method of claim 167, wherein the thickness of the insulating layers is 2 times more than
9 the thickness of the conducting layer.
- 10 192. A method for improving reliability of catalyst influenced chemical etching, the method
11 comprising:
- 12 patterning a catalyst layer on a surface of a semiconducting material, wherein said catalyst
13 layer comprises a plurality of features;
- 14 exposing said patterned catalyst layer on said surface of said semiconducting material to a
15 preprocessing step, wherein the preprocessing step is used to modify surface properties
16 of the catalyst surface, the semiconductor surface, and the interface between the
17 catalyst and the semiconductor surface; and
- 18 exposing said preprocessed substrate to an etchant, wherein said patterned catalyst layer
19 causes etching of said semiconducting material to form structures corresponding to the
20 plurality of features.
- 21 193. The method of claim 192, wherein the preprocessing step comprises exposing the surfaces
22 to one or more of the following chemicals in various dilutions: Vapor HF, Piranha solution,
23 Buffered Oxide Etch, Hydrofluoric acid, Acetone, or Ethanol.
- 24 194. The method of claim 192, wherein the preprocessing step comprises exposing the surfaces
25 to a plasma such as oxygen plasma, carbon dioxide plasma, hydrogen plasma, argon or
26 helium plasma.
- 27 195. The method of claim 192, wherein the surface properties include surface energy, surface
28 wettability measured by contact angle, interfacial energy.
- 29 196. The method of claim 192, wherein the preprocessing step improves the uniformity of the etch
30 by improving surface energy of the catalyst and semiconductor interface.

- 1 197. A 3D flash memory device, comprising:
2 at least twenty layers of active memory arrays;
3 a gate or a channel with a wall angle greater than 89.5 degrees; and
4 isolating trenches between blocks of memory wherein the trenches also have a wall angle
5 greater than 89.5 degrees.
- 6 198. The 3D flash device of claim 197, wherein the wall angle is measured with respect to the
7 critical feature dimension on the top and bottom of one or more of the following: gate, channel,
8 and isolating trenches.
- 9 199. The 3D flash device of claim 198, wherein the critical feature dimension is extracted from a
10 metrology technique including Scanning Electron Microscopy (SEM), Transmission Electron
11 Microscopy (TEM), or Atomic Force Microscopy (AFM).
- 12 200. A 3D flash memory device, comprising:
13 at least twenty layers of active memory arrays; and
14 vertical gates or channels that have a center-to-center distance of less than 120nm.
- 15 201. A 3D flash memory device, comprising:
16 at least twenty layers of active memory arrays; and
17 vertical gates or channels that have a center-to-center distance of less than 100nm.
- 18 202. A 3D flash memory device, comprising:
19 at least twenty layers of active memory arrays; and
20 vertical gates or channels that have a center-to-center distance of less than 80nm.
- 21 203. A high aspect ratio finFET array, comprising:
22 fins that have at least an aspect ratio of at least 5:1;
23 wherein the fins have a wall angle that is greater than 89.5 degrees; and
24 a base of the fins is surrounded by a dielectric for shallow trench isolation.
- 25 204. The high aspect ratio finFET array of claim 203, wherein the fin wall angle is measured with
26 respect to the critical feature dimension on the top of the fin and at the bottom of the fin.

- 1 205. The high aspect ratio finFET array of claim 204, wherein the critical feature dimension is
2 extracted from a metrology technique such as Scanning Electron Microscopy (SEM),
3 Transmission Electron Microscopy (TEM), or Atomic Force Microscopy (AFM).
- 4 206. A high aspect ratio nanosheet FET array, comprising:
5 fins that have at least an aspect ratio of at least 5:1;
6 wherein the fin wall angle is greater than 89.5 degrees; and
7 a base of the nanosheet FET is a fin surrounded by a dielectric for shallow trench isolation.
- 8 207. The high aspect ratio nanosheet finFET array of claim 206, wherein the fins comprise lateral
9 layers of semiconducting materials with all around dielectric and gate metals.
- 10 208. The high aspect ratio nanosheet finFET array of claim 206, wherein the structure is also
11 defined as nanosheet FETs or lateral nanowire FETs.
- 12 209. The high aspect ratio nanosheet finFET array of claim 206, wherein the fin wall angle is
13 measured with respect to the critical feature dimension on the top of the fin and at the bottom
14 of the fin.
- 15 210. The high aspect ratio nanosheet finFET array as recited in claim 209, wherein the critical
16 feature dimension is extracted from a metrology technique such as Scanning Electron
17 Microscopy (SEM), Transmission Electron Microscopy (TEM), or Atomic Force Microscopy
18 (AFM).
- 19 211. A high aspect ratio finFET array, comprising:
20 fins having a center-to-center distance of 30nm and a height of at least 500nm; and
21 a base of the fins is surrounded by a dielectric for shallow trench isolation.
- 22 212. The high aspect ratio finFET array of claim 211, wherein the fins have a fin wall angle that is
23 greater than 89.5 degrees.
- 24 213. The high aspect ratio finFET array of claim 212, wherein the critical feature dimension is
25 extracted from a metrology technique such as Scanning Electron Microscopy (SEM),
26 Transmission Electron Microscopy (TEM), or Atomic Force Microscopy (AFM).
- 27 214. A method of creating high aspect ratio trenches using catalyst influenced chemical etching,
28 the method comprising:
29 providing a semiconductor substrate;

1 catalyst influenced chemical etching of the semiconductor substrate to create high aspect ratio
2 semiconductor holes with a top non-porous layer and one or more bottom porous layers;
3 depositing material to seal the one or more bottom porous layers; and
4 depositing material to fill the high aspect ratio holes.

5 215. The method of claim 214, wherein the top porous layer has a thickness of less than 100nm,
6 and one bottom porous layer has a thickness of more than 200nm.

7 216. The method of claim 214, wherein the one or more bottom porous layers are selectively
8 oxidized.

9 217. The method of claim 216, wherein the pores are sealed using silicon oxide deposited using
10 atomic layer deposition.

11 218. The method of claim 214, wherein the one or more bottom porous layers enable diffusion of
12 etchants between the high aspect ratio holes during CICE.

13 219. The method of claim 216, wherein the structure is used to make DRAM cells with trench
14 capacitors.

15 220. The method of claim 216, wherein the structure is used to make FinFETs with the top non-
16 porous structure as the active portion of the fin and the oxidized porous bottom structure acting
17 as shallow trench isolation (STI).

18 221. The method of claim 216, wherein the structure is used to make Nanosheet FETs with the
19 top structure comprising more than one non-porous and oxidized porous layers, and with the
20 oxidized porous bottom structure acting as shallow trench isolation (STI).