~~What is claimed is:~~

CLAIMS

1. A method of forming a semiconductor device comprising:

providing a substrate prepared with a device region surrounded by an isolation region, the device region includes edge portions along a width direction of the device region and a central portion between the edge portions;

forming a gate electrode layer in the device region, wherein the gate electrode layer comprises a graded thickness in which a thickness T_E at edge portions of the device region is different from a thickness T_C at the central portion of the device region.

2. The method of claim 1 wherein forming the gate electrode with the graded thickness comprises:

protecting the central portion of the gate electrode with a mask which leaves edge portions of the gate electrode exposed; and

thinning edge portions of the gate electrode to the thickness T_E.

3. The method of claim 2 wherein the mask is formed by printing the active area mask smaller.

4. The method of claim 1 wherein forming the gate electrode with the graded thickness comprises providing the isolation region with a top surface above a top surface of the substrate to form a raised isolation region.

5. The method of claim 4 wherein the gate electrode layer is formed by PVD.

6. The method of claim 4 wherein the top surface of the isolation region is sufficiently above the top surface of the substrate to form the gate electrode layer with the graded thickness.

7. The method of claim 4 wherein the top surface of the isolation region is about 40 – 50 Å higher than the top surface of the substrate.

8. The method of claim 1 wherein T_E is less than T_C.

9. The method of claim 8 wherein T_E is equal to about 30 – 40% of TC.

10. The method of claim 8 wherein T_E is sufficiently less than T_C to reduce V_T roll up.

11. The method of claim 8 wherein an edge portion is about 30% of an overall width of the device region.

12. The method of claim 8 wherein the graded thickness is a gradual change in thickness from T_C to T_E.

13. The method of claim 1 comprises forming a top gate electrode layer over the gate electrode layer.

14. A device comprising:

a substrate with a device region surrounded by an isolation region, the device region includes edge portions along a width of the device region and a central portion;

a gate layer disposed on the substrate over the device region, the gate layer includes a graded thickness in which the gate layer at edge portions of the device region has a thickness T_E that is different from a thickness T_C at the central portion of the device region.

15. The device of claim 14 wherein the isolated region comprises a raised isolation region, the raised isolation region has a top surface above a top surface of the substrate.

16. The device of claim 14 wherein T_E is less than T_C.

17. The device of claim 16 wherein T_E is equal to about 30 – 40% of T_C.

18. The device of claim 16 wherein T_E is sufficiently less than T_C to reduce V_T roll up.

19. The device of claim 16 wherein an edge portion is about 30% of an overall width of the device region.

20. The device of claim 16 wherein the graded thickness is a gradual change in thickness from T_C to T_E.

21. The device of claim 14 comprises a top gate electrode layer over the gate electrode layer.

22. The device of claim 14 comprises a high-K dielectric layer below the gate electrode layer.

23. A device comprising:

a substrate;

a device region in the substrate;

an isolation region surrounding the device region, wherein the device region comprises:

an edge portion proximate the isolation region;

a central portion distal the isolation region; and

a gate electrode layer on the device region, wherein a thickness T_E of the gate electrode layer at the edge portion is different from a thickness T_C of the gate electrode layer at the central portion.

What is claimed is:

CLAIMS

1. A method of forming a semiconductor device comprising:

providing a substrate having a substrate surface, the substrate is prepared with a device region surrounded by an isolation region, the device region serves as a device region of a transistor having a width direction and a length direction, wherein the width direction is a channel width direction of the transistor and the length direction is a channel length direction of the transistor, wherein a length of the channel is between source/drain regions of the transistor, the width and length directions are perpendicular, and the device region includes edge portions along the width direction of the device region and a central portion between the edge portions; and

forming a metal gate electrode layer over the surface of the substrate in the device region, the metal gate electrode having a top surface, wherein the metal gate electrode layer comprises a graded thickness along the width direction of the device region, the graded thickness resulting in the top surface of the metal gate electrode having an uneven height with respect to the substrate surface, wherein a thickness T_E at edge portions of the device region along the width direction with respect to the substrate surface is thinner than a thickness T_C at the central portion of the device region.

2. The method of claim 1 wherein forming the metal gate electrode with the graded thickness comprises:

protecting the central portion of the metal gate electrode with a mask which leaves edge portions of the metal gate electrode exposed; and

thinning edge portions of the metal gate electrode to the thickness T_E.

3. The method of claim 2 wherein the mask is formed by printing the mask smaller to expose the edge portions of the metal gate electrode.

4. The method of claim 1 wherein forming the metal gate electrode with the graded thickness comprises:

providing the isolation region with a top surface above the top surface of the substrate to form a raised isolation region; and

depositing the metal gate electrode layer over the raised isolation region and the substrate, wherein the raised isolation region creates a shadowing effect which thins the edge portions of the metal gate electrode to produce the thickness T_E.

5. The method of claim 4 wherein the metal gate electrode layer is formed by PVD.

6. The method of claim 4 wherein the top surface of the isolation region is sufficiently above the top surface of the substrate to form the metal gate electrode layer with the graded thickness.

7. The method of claim 4 wherein the top surface of the isolation region is about 40 – 50 Å higher than the top surface of the substrate.

8. The method of claim 1 wherein T_E is equal to about 30 – 40% of T_C.

9. The method of claim 1 wherein T_E is sufficiently less than T_C to reduce V_T roll up.

10. The method of claim 1 wherein an edge portion is about 30% of an overall width of the device region.

11. The method of claim 1 wherein the graded thickness is a gradual change in thickness from T_C to T_E.

12. The method of claim 1 comprises forming a gate dielectric layer, wherein the gate dielectric layer is in between the metal gate electrode layer and the substrate.

13. A device comprising:

a substrate with a device region surrounded by an isolation region, the device region serves as a device region of a transistor having a width direction and a length direction, wherein the width direction is a channel width direction of the transistor and the length direction is a channel length direction of the transistor, wherein a length of the channel is between source/drain regions of the transistor, the width and length directions are perpendicular, and the device region includes edge portions along the width of the device region and a central portion between the edge portions;

a metal gate electrode layer disposed over surface of the substrate over the device region, the metal gate electrode layer includes a graded thickness along the width direction of the device region in which a top surface of the metal gate electrode includes an uneven height with respect to the substrate surface, wherein the metal gate layer at the edge portions along the width direction of the device region has a thickness T_E that is thinner than a thickness T_C at the central portion of the device region.

14. The device of claim 13 wherein the isolated region comprises a raised isolation region, the raised isolation region has a top surface above a top surface of the substrate.

15. The device of claim 13 wherein T_E is equal to about 30 – 40% of T_C.

16. The device of claim 13 wherein T_E is sufficiently less than T_C to reduce V_T roll up.

17. The device of claim 13 wherein an edge portion is about 30% of an overall width of the device region.

18. The device of claim 13 wherein the graded thickness is a gradual change in thickness from T_C to T_E.

19. The device of claim 13 comprises a gate dielectric layer in between the metal gate electrode layer and the substrate.

20. The device of claim 19 wherein the gate dielectric layer comprises a high-K dielectric layer.

21. A device comprising:

a substrate having a substrate surface;

a device region in the substrate, wherein the device region serves as a device region of a transistor having a width direction and a length direction, wherein the width direction is a channel width direction of the transistor and the length direction is a channel length

direction of the transistor, wherein a length of the channel is between source/drain regions of the transistor, the width and length directions are perpendicular;

an isolation region surrounding the device region, wherein the device region along the width direction comprises

an edge portion proximate the isolation region, and

a central portion distal the isolation region;

a gate dielectric layer over the device region and in contact with the substrate; and

a metal gate electrode layer over and in contact with the gate dielectric layer, wherein the metal gate electrode includes a top gate electrode surface which is uneven in height along the width direction of the device region with respect to the substrate surface, a thickness T_E of the metal gate electrode layer at the edge portion with respect to the substrate surface along the width direction of the device region is thinner than a thickness T_C of the metal gate electrode layer at the central portion.

22. The device of claim 21 which further comprises a polycrystalline gate electrode layer directly over the metal gate electrode layer.

23. The device of claim 13 which further comprises a polycrystalline gate electrode layer directly over the metal gate electrode layer.

24. The method of claim 1 which further comprises forming a polycrystalline gate electrode layer directly over the metal gate electrode layer.

25. The method of claim 12 wherein:

the edge portions are proximate to the isolation region;

the central portion is distal the isolation region; and

the thickness T_E of the metal gate electrode layer at the edge portions with respect to the substrate surface which contacts the gate dielectric layer is thinner than the thickness T_C of the metal gate electrode layer at the central portion which contacts the gate dielectric layer along the width direction of the device region.

26. The device of claim 13 wherein:

the edge portions are proximate to the isolation region;

the central portion is distal the isolation region; and

the thickness T_E of the metal gate electrode layer at the edge portions with respect to the substrate surface which contacts the gate dielectric layer is thinner than the thickness T_C of the metal gate electrode layer at the central portion which contacts the gate dielectric layer along the width direction of the device region.