WHAT IS CLAIMED IS:

1. A memory device, comprising:

a memory array structure comprising at least one memory bank, each memory bank comprising a plurality of memory blocks; and

a peripheral structure comprising a word line driver circuit and a sense amplifier circuit,

wherein a first area comprising the word line driver circuit and the sense amplifier circuit at least partially overlaps a second area comprising a memory block in a plan view of the memory device,

wherein the first area comprises a first subarea comprising the word line driver circuit and two second subareas each comprising the sense amplifier circuit, wherein the first subarea is disposed between adjacent memory blocks in the plan view of the memory device, and the two second subareas overlap the second area of the memory block in the plan view of the memory device.

2. The memory device of claim 1, wherein the first area comprises a first subarea comprising the word line driver circuit and a second subarea comprising the sense amplifier circuit, wherein the first subarea and the second subarea are alternately arranged in the first area.

3. The memory device of claim 2, wherein the first area comprises two first subareas and two second subareas, two first subareas are disposed on diagonal corners in the first area, and two second subareas are disposed on diagonal corners in the first area.

4. The memory device of claim 1, wherein the first area completely overlaps the second area in the plan view of the memory device.

5. The memory device of claim 3, wherein the word line driver circuit in one of the two first subareas is coupled to odd word lines in the memory block, and the word line driver circuit in the other of the two first subarea is coupled to even word lines in the memory block.

6. The memory device of claim 1, wherein the first area comprises a first subarea comprising the word line driver circuit and two second subareas each comprising the sense amplifier circuit, wherein the two second subareas are disposed on two sides of the first subarea.

7. The memory device of claim 6, wherein the sense amplifier circuit in one of the two second subareas is shared by two adjacent memory blocks.

8. The memory device of claim 6, wherein the sense amplifier circuit in one of the two second subareas is coupled to odd bit lines in the memory block and odd bit lines in a first adjacent memory block, and the sense amplifier circuit in the other of the two second subareas is coupled to even bit lines in the memory block and even bit lines in a second adjacent memory block.

9. The memory device of claim 1, wherein the memory array structure is disposed on a first substrate, and the peripheral structure is disposed on a second substrate different from the first substrate.

10. The memory device of claim 8, wherein the word line driver circuit in the first subarea is coupled to odd word lines in the memory block and is coupled to even word lines in adjacent memory blocks.

11. The memory device of claim 1, wherein the first area comprises a first subarea comprising the word line driver circuit, a second subarea comprising the sense amplifier circuit, and a third subarea comprising a decoder circuit, wherein the first subarea is disposed between adjacent memory blocks in the plan view of the memory device, and the second subarea and the third subarea overlap the second area of the memory block in the plan view of the memory device.

12. The memory device of claim 11, wherein the first area further comprises a fourth subarea comprising a control circuit for the sense amplifier circuit, and the fourth subarea is disposed between the second subarea and the third subarea.

13. The memory device of claim 12, wherein the second subarea, the third subarea, and the fourth subarea overlap the second area of the memory block in the plan view of the memory device.

14. The memory device of claim 1, wherein the first area further comprises a third subarea comprising a control circuit for the sense amplifier circuit, and the third subarea is disposed between the two second subareas.

15. A memory device, comprising:

a memory array structure disposed on a first substrate comprising at least one memory bank, each memory bank comprising a plurality of memory blocks; and

a peripheral structure disposed on a second substrate different from the first substrate comprising a sense amplifier circuit and a word line driver circuit,

wherein the sense amplifier circuit overlaps a memory block in a plan view of the memory device,

wherein the word line driver circuit is disposed between adjacent memory blocks in the plan view of the memory device.

16. The memory device of claim 15, wherein the peripheral structure further comprises a decoder circuit overlapping the memory block in the plan view of the memory device.

17. A method for forming a memory device, comprising:

forming a memory array structure on a first substrate, the memory array structure comprising at least one memory bank, each memory bank comprising a plurality of memory blocks;

forming a peripheral structure on a second substrate different from the first substrate, the peripheral structure comprising a word line driver circuit and a sense amplifier circuit; and

bonding the memory array structure and the peripheral structure to have the word line driver circuit and the sense amplifier circuit at least partially overlap a memory block in a plan view of the memory device, wherein the word line driver circuit is disposed between adjacent memory blocks in the plan view of the memory device.

18. The method of claim 17, wherein forming the peripheral structure on the second substrate, comprises:

forming the word line driver circuit in a first subarea and the sense amplifier circuit in a second subarea.

19. The method of claim 17, wherein forming the peripheral structure on the second substrate, comprises:

forming the word line driver circuit in a first subarea and the sense amplifier circuit in a second subarea and a third subarea.

20. The method of claim 17, wherein forming the peripheral structure on the second substrate, comprises:

forming the word line driver circuit in a first subarea, the sense amplifier circuit in a second subarea, and a decoder circuit in a third subarea.