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APPARATUS AND METHOD FOR DEMODULATING A MODULATED SIGNAL

Field of the invention

The present invention relates to an apparatus and method for demodulating a modulated signal.

Background of the invention

Bandpass sampling techniques are popular in the field of digital intermediate frequency (D-IF) receivers. In such techniques, a main consideration is to reduce the power consumption by using a low sampling rate. With bandpass sampling, the sampling rate can be lower than the IF frequency as long as it is higher than two times the bandwidth of the signal being processed. Conventional bandpass sampling techniques typically oversample the signal being processed whilst undersampling the IF signal. The sampling rate of bandpass sampling should meet the following requirement:

$$\frac{2f_u}{n} \leq f_s \leq \frac{2f_L}{n-1} \quad 1 \geq n \leq \left\lfloor \frac{f_u}{B} \right\rfloor \quad (1)$$

where , f_u is the highest frequency of the IF signal, f_L is the lowest frequency of the IF signal, f_s is the sampling rate, and B is the occupied bandwidth of the IF signal.

The equivalent digital IF after sampling will be denoted by:

$$f_{DIF} = (f_{IF} - n * f_s) \quad (2)$$

where f_{IF} is the analog IF of the received signal and n is an integer.

Normally, the sampling rate will be set as an integer multiple of the symbol rate. Also, there are some practical considerations in the selection of analog IF signals. For example, if a conventional D-IF receiver has the following parameters $f_{IF}=40$ MHz, $B=5$ MHz, $f_{sym}=2.048$ M, the lowest sampling rate equal to the integer multiple of the symbol rate will be 12.288 MHz ($n=6$) according to equation (1). The equivalent IF signal after sampling is denoted by equation (2) as follows:

$$f_{DIF} = (f_{IF} - n * f_s) = (40 - 3 * 12.288) = 3.136 \text{ MHz}$$

In traditional demodulators for MPSK and DMPK signals, an analogue to digital converter (ADC) is used to convert the received analogue signal (either a baseband signal or an intermediate frequency (IF) signal) into digital form for further processing. For digital processing, the signal is passed through a digital down converter (DDC) and a low pass filter (LPF) before being demodulated. A problem with the hardware typically used in conventional bandpass sampling techniques is that the digital down converter (DDC) and following LPF (low pass filter) structure cannot generally be simplified. Thus there is a need for a less complex and more economical system and method for bandpass sampling which ameliorates or substantially overcomes the abovementioned disadvantages.

Summary of the invention

In general terms, the invention provides a method and apparatus for demodulating a signal using a digital down converter to reduce the frequency of the digital signal being demodulated to one quarter of the sampling rate thereof.

This is particularly advantageous as it assists in simplifying the circuitry of the digital down converter and low pass filter used in the apparatus.

In particular, according to a first aspect of the present invention there is provided an apparatus for demodulating a modulated signal comprising:

- an analog to digital converter for converting an analog modulated input signal to a digital signal having an associated frequency, the analog to digital converter being arranged to sample the input signal at a predetermined sampling rate;

- a digital down converter for receiving the digital signal from an output of the analog to digital converter at the sampling rate and being arranged to reduce the frequency of the digital signal from the predetermined sampling rate to one quarter of the sampling rate;

- a low pass filter for receiving an output signal from the digital down converter and for filtering selected frequencies therefrom and produce a filtered output signal;

- a frequency offset stage for receiving the filtered signal and for applying a modification to the frequency of the filtered signal to reduce a frequency offset in the signal, and

- a differential demodulator for demodulating the signal after application of the modification to reduce the frequency offset in the signal.

Preferably, the digital down converter is arranged to separate the digital signal into inphase and quadrature components, the low pass filter being arranged to filter the inphase and quadrature components separately.

In a preferred embodiment, the analogue input signal has an associated symbol rate, the predetermined sampling rate being an integer multiple of the symbol rate.

Preferably, the frequency offset stage comprises a fixed frequency offset stage for applying a fixed frequency compensation modification to the frequency of the filtered signal to reduce the frequency offset in the signal due to the frequency of the signal being reduced by the digital down converter to one quarter of the sampling rate.

In an alternative preferred embodiment, the frequency offset stage is arranged to estimate a frequency offset value indicative of drift in the apparatus and to apply a frequency correction to the frequency of the filtered signal to reduce the frequency offset in the signal, the frequency correction being based on the estimated frequency offset value and the frequency offset due to the frequency of the signal being reduced by the digital down converter to one quarter of the sampling rate.

According to a second aspect of the present invention there is provided a method for demodulating a modulated signal comprising:

- converting an analog modulated input signal to a digital signal having an associated frequency using an analog to digital converter, the analog to digital converter being arranged to sample the input signal at a predetermined sampling rate;

- applying at the sampling rate the digital signal from an output of the analog to digital converter to a digital down converter,

- reducing in the digital down converter the frequency of the digital signal from the predetermined sampling rate to one quarter of the sampling rate;

filtering selected frequencies from an output signal from the digital down converter using a low pass filter to produce a filtered output signal;

applying the filtered signal to a frequency offset stage,

applying a modification to the frequency of the filtered signal using the frequency offset stage to reduce a frequency offset in the signal, and

demodulating the signal using a differential demodulator after application of the modification to reduce the frequency offset in the signal.

Preferably, the method further comprises separating the digital signal into inphase and quadrature components using the digital down converter, and wherein the step of filtering the signal comprises filtering the inphase and quadrature components separately.

In a preferred embodiment, the step of applying a modification to the frequency in the frequency offset stage comprises applying a fixed frequency compensation modification to the frequency of the filtered signal to reduce the frequency offset in the signal due to the frequency of the signal being reduced by the digital down converter to one quarter of the sampling rate.

In a further preferred embodiment, the step of applying a modification to the frequency in the frequency offset stage comprises estimating a frequency offset value indicative of drift in the apparatus and applying a frequency correction to the frequency of the filtered signal to reduce the frequency offset in the signal, the frequency correction being based on the estimated frequency offset value and the frequency offset due to the frequency of the signal being reduced by the digital down converter to one quarter of the sampling rate.

According to a third aspect of the invention there is provided a receiver comprising the apparatus defined above.

Brief description of the drawings

The present invention will now be described by way of example and with reference to the drawings in which:

Figure 1 is a graph showing the variation of amplitude with frequency for a conventional bandpass sampling system showing the frequency components present in the system;

Figure 2 is a block schematic of a digital IF receiver system according to a first preferred embodiment of the present invention; and

Figure 3 is a block schematic of a digital IF receiver system according to a second preferred embodiment of the present invention with frequency offset estimation.

Detailed description of preferred embodiments

Figure 1 is a graph showing the variation of amplitude with frequency for a conventional bandpass sampling system. The spectrum after analogue-to-digital (ADC) is shown for a sampling rate of 12.288MHz. The amplitude of the positive component 1 is shown at 3.136 MHz, 15.424MHz, 27.712 MHz and 40 MHz. The amplitude of the negative component 2 is shown at 9.152 MHz, 21.0440MHz and 33.728MHz.

Figure 2 shows a block diagram of a number of stages in D-IF receiver embodying a first preferred embodiment of the invention. The stages shown comprise an analog-to-digital converter 2, a digital down conversion stage 4, two low pass filter stages 6, a frequency offset compensation stage 8 and a differential demodulator stage 10. The analog modulated input signal is

applied to the analog to digital converter 2 where it is sampled at a sampling rate and converted to a digital signal. The digital signal is then applied to the input of the digital down conversion stage 4 which reduces the frequency of the digital signal from the sampling rate to one quarter of the sampling rate and provides inphase I and quadrature Q component signals. These two components are passed to two low pass filter stages 6, one for each component and the filtered outputs are applied to the fixed frequency offset compensation stage 8. The compensated outputs are applied to the differential demodulation stage 10 to produce final I and Q components which may then be further processed in other stages (not shown) to obtain a fully demodulated signal.

Figure 3 shows a block diagram of a number of stages in a D-IF receiver embodying a second preferred embodiment of the invention. The stages shown comprise an analog-to-digital converter 12, a digital down conversion stage 14, two low pass filter stages 16, a frequency offset estimation and correction stage 18 and a differential demodulator stage 20.

The analog modulated input signal is applied to the analog to digital converter 12 where it is sampled at a sampling rate and converted to a digital signal. The digital signal is then applied to the input of the digital down conversion stage 14 which reduces the frequency of the digital signal from the sampling rate to one quarter of the sampling rate and provides inphase I and quadrature Q component signals. These two components are passed to two low pass filter stages 16, one for each component and the filtered outputs are applied to the frequency offset estimation and correction stage 18. . The outputs of the frequency offset estimation and correction stage 18 are applied to the differential demodulation stage 20 to produce the final I and Q components which may then be further processed in other stages (not shown) to obtain a fully demodulated signal.

In operation, a D-IF receiver based on bandpass sampling may be used, for example, to demodulate $\pi/4$ DQPSK modulated signals. Signal digitization is performed by the analog-to-digital converter stages 2 and 12. The digital IF of the digital down conversion stage 4 and 14 is set to be one quarter of the sampling rate. By setting the digital IF of the digital down conversion stage 4 and 14 to be one quarter of the sampling rate, according to one or more preferred embodiments of the present invention, a simplified digital down conversion stage design may be achieved. This is in contrast to conventional systems which generally require the sampling rate to be at least greater than two times the bandwidth of the signal being processed and an integer multiple thereof, with the effect that the equivalent digital IF of the digital down conversion stage is not equal to a quarter of the sampling rate, particularly when the practical limitations of analogue IF selection are also considered. This is shown from the example given in Figure 1,

If the digital IF of the digital down conversion stage is set to be one quarter of the sampling rate, the sine and cosine signals that represent the complex phasor of the digital down conversion stage degenerate to two simple sequences of $\{1 \ 0 \ -1 \ 0 \dots\}$ and $[0 \ -1 \ 0 \ 1 \dots]$. The frequency offset introduced into the digital down conversion stage may be compensated in the fixed frequency offset compensation stage, as shown in Figure 2, as it is a fixed frequency offset.

Thus the complexity of the digital down conversion stage may be reduced with appropriate selection of the sampling rate and digital IF in the digital down conversion stage. Moreover, the low pass filter following the digital down conversion stage may also be simplified as set out in commonly-assigned, co-pending Singapore Patent Application No. 200505405-1 (not yet published) herein incorporated by reference in its entirety. There is little or no performance penalty in the system of Figure 2, as the fixed frequency offset introduced by the digital down conversion stage may be compensated.

Usually, frequency offset estimation and correction is necessary in wireless communication systems as there are frequency offsets caused by clock drift and Doppler shift. Therefore, as shown in Figure 3, the pre-compensation for the fixed frequency offset inherent in the digital down conversion stage 14 may be removed provided that the total frequency offset is still within the working range of frequency offset estimation and correction scheme. This results in a further reduction in complexity of the hardware of such a system.

Thus, the one or more preferred embodiments of the present invention provide a simple and efficient apparatus and method for simplifying the hardware of down conversion and filtering for D-IF receivers with bandpass sampling. Such a digital IF receiver based on bandpass sampling is particularly suitable for use in wireless communication systems.

Various modifications to the embodiments of the present invention described above may be made. For example, other components and method steps can be added or substituted for those above. Thus, although the invention has been described above using particular embodiments, many variations are possible within the scope of the claims, as will be clear to the skilled reader, without departing from the scope of the invention.

Claims

1. An apparatus for demodulating a modulated signal comprising:

an analog to digital converter for converting an analog modulated input signal to a digital signal having an associated frequency, the analog to digital converter being arranged to sample the input signal at a predetermined sampling rate;

a digital down converter for receiving the digital signal from an output of the analog to digital converter at the sampling rate, the digital down converter being arranged to reduce the frequency of the digital signal from the predetermined sampling rate to one quarter of the sampling rate;

a low pass filter for receiving an output signal from the digital down converter and for filtering selected frequencies therefrom and produce a filtered output signal;

a frequency offset stage for receiving the filtered signal and for applying a modification to the frequency of the filtered signal to reduce a frequency offset in the signal, and

a differential demodulator for demodulating the signal after application of the modification to reduce the frequency offset in the signal.

2. An apparatus according to claim 1, wherein the digital down converter is arranged to separate the digital signal into inphase and quadrature components, the low pass filter being arranged to filter the inphase and quadrature components separately.

3. An apparatus according to claim 1, wherein the analogue input signal has an associated symbol rate, the predetermined sampling rate being an integer multiple of the symbol rate.

4. An apparatus according to claim 1, wherein the frequency offset stage comprises a fixed frequency offset stage for applying a fixed frequency compensation modification to the frequency of the filtered signal to reduce the frequency offset in the signal due to the frequency of the signal being reduced by the digital down converter to one quarter of the sampling rate.

5. An apparatus according to claim 1, wherein the frequency offset stage is arranged to estimate a frequency offset value indicative of drift in the apparatus and to apply a frequency correction to the frequency of the filtered signal to reduce the frequency offset in the signal, the frequency correction being based on the estimated frequency offset value and the frequency offset due to the frequency of the signal being reduced by the digital down converter to one quarter of the sampling rate.

6. A method for demodulating a modulated signal comprising:

converting an analog modulated input signal to a digital signal having an associated frequency using an analog to digital converter, the analog to digital converter being arranged to sample the input signal at a predetermined sampling rate;

applying at the sampling rate the digital signal from an output of the analog to digital converter to a digital down converter;

reducing in the digital down converter the frequency of the digital signal from the predetermined sampling rate to one quarter of the sampling rate;

filtering selected frequencies from an output signal from the digital down converter using a low pass filter to produce a filtered output signal;

applying the filtered signal to a frequency offset stage,

applying a modification to the frequency of the filtered signal using the frequency offset stage to reduce a frequency offset in the signal, and

demodulating the signal using a differential demodulator after application of the modification to reduce the frequency offset in the signal.

7. A method according to claim 6, further comprising separating the digital signal into inphase and quadrature components using the digital down converter, and wherein the step of filtering the signal comprises filtering the inphase and quadrature components separately.

8. A method according to claim 6, wherein the analogue input signal has an associated symbol rate, the predetermined sampling rate being an integer multiple of the symbol rate.

9. A method according to claim 6, wherein the step of applying a modification to the frequency in the frequency offset stage comprises applying a fixed frequency compensation modification to the frequency of the filtered signal to reduce the frequency offset in the signal due to the frequency of the signal being reduced by the digital down converter to one quarter of the sampling rate.

10. A method according to claim 6, wherein the step of applying a modification to the frequency in the frequency offset stage comprises estimating a frequency offset value indicative of drift in the apparatus and applying a frequency correction to the frequency of the filtered signal to reduce the frequency offset in the signal, the frequency correction being based on the estimated frequency offset value and the frequency offset due to the frequency of the signal being reduced by the digital down converter to one quarter of the sampling rate.

11. A receiver comprising the apparatus according to claim 1.