CLAIMS

1. A through silicon interposer wafer having at least one cavity formed therein for MEMS applications, the interposer wafer comprising one or more filled silicon vias proximate to the at least one cavity, the one or more filled silicon vias framing the at least one cavity by defining walls of the cavity on all vertical sides and providing support for the walls of the at least one cavity during subsequent processing of the interposer wafer, wherein the one or more filled silicon vias are filled with material, the material comprising a first conductive material and a second conductive material, the first and second conductive materials separated by a first dielectric material.

2. The interposer wafer as claimed in claim 1, wherein the one or more filled silicon vias comprises one or more filled through silicon vias.

3. The interposer wafer as claimed in claim 2, wherein the one or more filled through silicon vias are filled with material for providing electrical feedthrough from one side to other of the interposer wafer.

4. The interposer wafer as claimed in claim 1, wherein at least a portion of the first and the second conductive materials is electrically connected through a third conductive material, the third conductive material disposed on at least a portion of the second conductive material.

5. The interposer wafer as claimed in any one of claims 1 to 4, comprising a second dielectric material disposed on a surface of the interposer wafer, the second dielectric further disposed within the one or more filled silicon vias and between the material that fills the filled silicon vias and the interposer wafer.

6. The interposer wafer as claimed in claim 4, further comprising at least one standoff, wherein the at least one standoff comprises the first and second conductive materials separated by the first dielectric material and electrically connected through the third conductive material.

7. The interposer wafer as claimed in claim 6, wherein each of the at least one standoff defines a local bonding area for one or more bond pads and/or one or more sealing rings.

8. The interposer wafer as claimed in any one of claims 4 or 6, further comprising at least one electrode, wherein the at least one electrode comprises the first conductive material and the third conductive material.

9. The interposer wafer as claimed in any one of claims 4, 6 or 8, further comprising at least one redistribution line, wherein the at least one redistribution line comprises the first conductive material and/or the third conductive material.

10. The interposer wafer as claimed in any one of claims 4, 6, 8 or 9, wherein the first and the second conductive material comprise either polysilicon or copper.

11. The interposer wafer as claimed in any one of claims 4, 6, 8 or 9, wherein the third conductive material comprises a material selected from a group comprising tantalum, tantalum alloys, tantalum nitrides, titanium, titanium alloys, titanium nitrides and germanium or a combination of these materials.

12. The interposer wafer as claimed in any one of claims 1 to 11, further comprising a getter material formed over an open surface of the at least one cavity.

13. A method of manufacturing a through silicon interposer wafer having at least one cavity formed therein for MEMS applications, the method comprising:

forming one or more filled silicon vias in the interposer wafer; and

thereafter forming the at least one cavity within the interposer wafer proximate to at least one of the one or more silicon vias; and

filling the one or more silicon vias with a material to provide support for walls of the at least one cavity during formation and subsequent processing of the interposer wafer,

wherein the at least one of the one or more silicon vias frame the at least one cavity by defining walls of the cavity on all vertical sides, and

wherein filling the one or more silicon vias with the material comprises:

depositing a first conductive material on the interposer and within the one or more silicon vias;

forming a first dielectric material on the first conductive material; and

depositing a second conductive material on the first dielectric material.

14. The method as claimed in claim 13, wherein the step of forming one or more filled silicon vias in the interposer wafer comprises forming one or more through silicon vias in the interposer wafer.

15. The method as claimed in claim 16, wherein the step of filling the one or more silicon vias comprises filling the one or more through silicon vias with material which will provide electrical feedthrough from one side to other of the interposer wafer.

16. The method as claimed in claim 13, further comprising depositing a third conductive material on at least a portion of the second conductive material, wherein the third conductive material electrically connects at least a portion of the first and the second conductive material.

17. The method as claimed in claim 13, wherein the step of filling the one or more silicon vias with the material comprises forming a second dielectric material on a surface of the interposer wafer, the at least one cavity having an opening in the surface of the interposer wafer, the second dielectric further formed within the one or more silicon vias and between the first conductive material and the interposer wafer.

18. The method as claimed in claim 16, further comprising patterning the second conductive material and then depositing the third conductive material to form at least one standoff, the standoff comprising the first and second conductive materials separated by the first dielectric layer, and electrically connected through the third conductive material.

19. The method as claimed in claim 16 or 18, further comprising simultaneously patterning the first conductive material and the third conductive material to form at least one electrode, the electrode comprising the first conductive material and the third conductive material.

20. The method as claimed in claim 18, wherein the step of patterning the second conductive material to form the at least one standoff comprises patterning the second conductive material to form the at least one standoff and at least one additional element, the method further comprising patterning the third conductive material and the first conductive material at the at least one additional element after depositing the third conductive material to form at least one electrode, the electrode comprising the first conductive material and the third conductive material.

21. The method as claimed in claim 20, wherein the step of patterning the third conductive material and the first conductive material to form the at least one electrode comprises patterning the third conductive material and the first conductive material to form the at least one electrode and at least one redistribution line, the at least one redistribution line comprising the first conductive material and/or the third conductive material.

22. The method as claimed in any one of claims 13 to 21, wherein the first and the second conductive material comprise either polysilicon or copper.

23. The method as claimed in any one of claims 16, or 18 to 21, wherein the third conductive material comprises a material selected from a group comprising tantalum, tantalum alloys, tantalum nitrides, titanium, titanium alloys, titanium nitrides and germanium or a combination of these materials.

24. The method as claimed in any one of claims 13 to 23, further comprising a step of forming an open surface of the at least one cavity, comprising depositing a getter over a surface of the at least one cavity.

25. The method as claimed in claim 20, wherein the step of patterning the second conductive material to form the at least one standoff and the at least one additional element further comprises adjusting a height and/or a surface roughness of the second conductive material.