METHOD TO FORM A VERTICAL TRANSISTOR BY FIRST FORMING A GATE/SPACER STACK, THEN USING SELECTIVE EPITAXY TO FORM SOURCE, DRAIN AND CHANNEL

ABSTRACT

A method of manufacturing a vertical transistor. A doped region is formed in a substrate. We form sequentially on the substrate: a first spacer dielectric layer, a first gate electrode, a second spacer dielectric layer, a second gate electrode and a third spacer dielectric layer. A trench is formed through the first spacer dielectric layer, the first gate electrode, the second spacer dielectric layer, the second gate electrode and the third spacer dielectric layer. The trench has sidewalls. A gate dielectric layer is formed over the sidewalls of the trench. We form sequentially, in the trench: a first doped layer, a first channel layer, a second doped layer, a third doped layer, a second channel layer, and a fourth doped layer. A cap layer is formed over the structure. Contacts are preferably formed to the doped region, doped layers and gate electrodes.

FIGURE 6



162162



G00002