Description

The present invention, generally, relates to the packaging of electronic devices and, more particularly, to a first level electronic package, and method of making the same, for carrying an electronic device.

In recent years, the electronics industry has grown, improved and developed in its advance of the technology that it uses, and the technology involving the packaging of circuit components is advancing now with matching speed. For example, one monolithic chip measuring less than one-half inch square today can store one million bits of information, and in addition, such a chip can have many electronic circuits. Placing more and more electronic circuits on smaller and smaller chips makes the task of packaging these smaller chips with a module, approach the impossible.

A major restriction in attaching a device to a module seems to arise because of the mismatch in the respective coefficients of thermal expansion. This mismatch causes fractures and other circuit discontinuities in the electrical interconnections during thermal cycling. For example, the coefficient of thermal expansion for a typical chip is in the order of 3 micro inches per inch per degree Centigrade, while that of a typical ceramic module is in the order of 7 micro inches per inch per degree Centigrade (1 inch = 25,4 mm).

These fractures and other circuit discontinuities are the results of stresses that are developed when there is thermal cycling involved in their environment. This problem is compounded even further when a device is affixed rigidly to a module, as they are so frequently. The prior art is rich with efforts to solve the problems that arise from these thermal mismatches.

United States patent No. 3,777,220 to Tatusko et al. teaches a unique structure formed of discrete areas with different coefficients of thermal expansion and suggests the attaching of devices to those areas more closely matching the coefficient of thermal expansion of the device. This may well be a great teaching, theoretically, but with today's subminiturized devices, it lacks practicality.

United States patent No. 3,969,754 to Kuniya et al. describes an arrangement whereby a supporting electrode has embedded fibers of a coefficient of thermal expansion "substantially equal to" that of a device to be attached. The idea may be sound, but it lacks a degree of universal applicability that is necessary to attract financial investors in today's market.

One known technique for avoiding problems due to thermal mismatch is to mount the chip on a flexible film carrier. For example, U.S. Pat. No. 4,231,154 shows an integrated circuit chip mounted on a very thin layer of circuitized polyimide. This solution does however not recognize the problem of providing a support for the integrated circuit chip to be mounted.

United States patent No. 4,189,524 to Lazzari describes a multilayer, rigid support composed of a very thin layer of conductive material with negligible thermal expansion inserted between each conductive layer and each insulating layer. When this prior patent teaches that the problem of elevations of temperatures "can be ignored", it leads diametrically opposite to the present invention.

United States patent No. 4,413,308 to Brown clearly recognizes the problem of providing a support for a chip to prevent solder joint failures due to stress and differential thermal expansion, but the solution that is suggested is only limited and incomplete as it concerns the continuing problem in the manufacture of electronic equipment using microcircuit chips.

United States patent No. 4,480,288 describes a thin flexible film chip carrier having circuitry on both sides thereof. This double-sided circuitry is fabricated by depositing a first layer of chrome-copper-chrome circuitry on an aluminum substrate serving as an only temporary support member without any electrical function.

The problem arises because of the requirement of mounting, or packaging, the chip in such a way as to provide adequate heat sinking of the chip while permitting ease of mechanical and electrical connection, and disconnection, between the package and its printed circuit board. Underlying the problem is the thermal incompatibility of the carrier material, usually ceramic in nature, and the typical printed circuit board, usually an epoxy material.

A direct mounting of a chip carrier to a printed circuit board produces intolerable differential expansion that causes the above-described fractures or other discontinuities as a result of the stresses that are developed in these mounting connections during the normal cycles in temperature. As the above referred-to prior art patents indicate, there have been numerous approaches attempted in the past to solve this on-going problem, but until the present invention, none has appeared as totally effective.

A principal object of the present invention is to provide a new and improved flexible packaging structure for supporting an electronic device to overcome disadvantages inherent in prior structures.

It is also an important object of the invention to provide a method of fabricating a package for an electronic device to avoid operational limitations in an environment involving temperature cycling.

These objects are met by an assembly and a method of making it as defined in claims 1 and 5,

respectively.

Advantageous embodiments are defined in dependent claims 2 to 4 and 6 to 10.

One way of carrying out the invention is described in detail below with reference to drawings which illustrate only one specific embodiment in which:

FIG. 1 is a view in cross section, taken in elevation, illustrating significant aspects of the invention for use in the following description.

FIG. 2 is a view similar to FIG. 1 but illustrating another aspect as an aid in connection with the following description.

As has been mentioned hereinabove, the manufacture of electronic circuits has encountered problems in the increasingly tightening spiral to make these circuits smaller and smaller. Today such circuits have passed the miniaturized state to arrive at a true subminiaturized state, and the problems involved in the manufacturing end of the industry have been nearly as startling as the wonders produced by these circuits have been spectacular.

For example, to achieve the "stuffing" of electronic components into smaller and smaller spaces has developed a need for circuits to which these components are formed functionally to be increasingly more flexible. This miniaturization trend has reached a point where the mismatch in the coefficients of thermal expansion, between various silicon components and the carrier or other support to which they necessarily are attached, has stubbornly defied solution, that is, until this invention.

The coefficient of thermal expansion of silicon is approximately 3 micro inches per inch per degree Centigrade, and that of a ceramic substrate carrier is about 7 micro inches per inch per degree Centigrade. Therefore, when a silicon device is soldered directly to this ceramic substrate, this mismatch in their coefficients of thermal expansion causes the solder joint to crack during thermal cycling.

To make the substrate carrier of a very thin flexible material, taken alone without more, has proven to be effective. For example, see patent No. 4,231,154 which is assigned to the same Assignee as this invention. This thin film will not transfer a force to the solder connections during thermal cycling because the thin flexible material will itself buckle.

However, to achieve improved electrical performance of the package, a ground plane is required. But if a copper ground plane is used, then the coefficient of thermal expansion, which for copper is about 17 micro inches per inch per degree Centigrade, makes the mismatch problem even more severe.

A uniquely new structure is illustrated in FIG. 1 of the drawing and is formed by the method of the invention. A suitable insulating material, like TEFLON, is cast onto a metal carrier layer of INVAR. Paths are formed, called "vias", in the TEFLON, and next, a metal film is formed over the TEFLON. Finally, a desired circuit is formed of the metallized film.

Of course, copper-INVAR-copper or KOVAR are acceptable substitutes for INVAR, because it is only necessary that this material have a coefficient of thermal expansion that is close to that of a particular device to be bonded to the first level of this electronic package. To address the mismatch in coefficients of thermal expansion between the INVAR and the second level carrier, the Outer Lead Bonding (OLB) of leads are formed as illustrated in FIG. 2 of the drawings. This view illustrates a "stress relieved" manner of arrangement, particularly for the outer leads.

The mismatch in coefficients of thermal expansion between a device, such as a chip, and the carrier is solved effectively by making the insulating layer of a very thin, low modulus material such as a polyimide film of approximately 5 microns in thickness.

Now, the low coefficient of thermal expansion metal needed to address the chip to carrier mismatch problem is the cause of a problem of mismatch between the carrier and the second level carrier, whether a card or a board. However, an arrangement in accordance with the present invention solves this mismatch problem effectively.

Multiple layers can be fabricated using the steps of the invention repeatedly. To illustrate the respective steps of the invention, they are:

1. An electrically insulating material, such as TEFLON (PTFE), is cast onto INVAR, copper INVAR or KOVAR metal material, which can be in sheet or roll form.
2. Using masking and etching techniques, which can be wet or dry, form paths (vias) through the TEFLON to the metal carrier material.
3. Metallize the TEFLON with chromium and copper chromium by any suitable technique, such as evaporating or sputtering.
4. Form a predetermined electronic circuit on the metallized TEFLON, including circuit conductor paths, identified points for bonding devices, and other connector ends.

Multiple layers can be fabricated by using the above steps 1-4 repeatedly. The metal carrier is left in place and operates functionally as a means of connecting electrical power, including "ground", to the circuit as well as to the various devices.

A structure fabricated by the above-described method and as illustrated in the drawings permits the advantage that a chip, or other device or component, can be attached by bonding utilizing the connection process called Controlled Collapse Chip

Connection (or "C-4"). This is a reflow solder process for bonding the input/output terminals of the device to the pads or other connection points preformed on the circuit.

In addition, a structure fabricated by the method of the invention permits bonding also by thermal compression techniques. In other words, the structure of the invention removes the heretofore limitations and restrictions as to the type of bonding that is appropriate.

The inventive structure also permits the leads for providing means of connection and interconnection between devices, components and the respective power plane, to be more dense. Even though these circuits and the devices attached to them are getting smaller and smaller, the power needs to operate them is increasing. Therefore, the present structure permits a significant advantage.

The particular chromium-copper-chromium foil has a thickness as follows:

chromium - approximately 20 nm
copper - approximately 8000 nm
chromium - approximately 20 nm

As has been described hereinabove, an insulation and a circuit pattern can be applied to both sides of a copper-INVAR-copper metal carrier layer. In a preferred arrangement, the copper-INVAR-copper metal carrier layer functions as a ground plane, and circuit lines that are ground potential are connected to this carrier layer.

Since a major part of this structure is metal, an efficient thermal conduction is obtained.

With a multilayer arrangement of the inventive structure, the interleaved copper-INVAR-copper metal carrier planes form effective shields for the circuits from stray fields, particularly when these metal carrier planes are used for ground potential connections.

The polyimide as described herein that is suitable for use with a structure according to the invention is manufactured commercially by DuPont de Nemours, E. I. and Company and is identified as DuPont Polyimide 5878. KOVAR is a registered trademark of Westinghouse Electric Corp.

Claims

1. An electronic package assembly, comprising:
a flexible carrier layer formed of a material that is electrically conductive and has a coefficient of thermal expansion that is close to that of a particular electronic device to be bonded to this electronic package;
a layer of electrically insulating low modulus material formed as a thin film on and supported by said flexible carrier layer material;
an electrical circuit formed on and supported by said layer of electrically insulating low modulus material, including conductors of electrically conductive material in a predetermined pattern;
an electronic device bonded to said electrical circuit in a predetermined location to be operatively functional with said electrical circuit; and
at least one via formed through said layer of electrically insulating low modulus material for connecting said electrical circuit at a preselected location to said flexible carrier layer of electrically conductive material.

2. The electronic package assembly as described in claim 1 wherein said flexible carrier layer is formed from a material from the group including Invar, copper-Invar-copper, Kovar and copper-Kovar-copper.

3. The electronic package assembly as described in claim 1 or 2 wherein said layer of electrically insulating material consists of a polyimide.

4. The electronic package assembly as described in claim 1 or 2 wherein said layer of electrically insulating material includes Teflon.

5. A method of making an electronic package assembly, comprising the steps of:
providing a flexible carrier layer of an electrically conductive material with a coefficient of thermal expansion that is close to that of a particular electronic device to be bonded to this electronic package;
forming on said flexible carrier layer a thin film layer of electrically insulating low modulus material;
forming vias through said layer of electrically insulating low modulus material at predetermined locations to communicate with said flexible carrier layer;
metallizing said layer of electrically insulating low modulus material and said vias;
forming an electrical circuit from said metallization; and
bonding an electronic device to said electrical circuit in a predetermined location to be operatively functional with said electrical circuit.

6. The method of making an electronic package assembly as described in claim 5 wherein said step of providing a flexible carrier layer of an electrically conductive material includes the use of a material from the group including Invar, copper-Invar-copper, Kovar and copper-Kovar-copper.

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In addition, a structure fabricated by the method of the invention permits bonding also by thermal compression techniques. In other words, the structure of the invention removes the heretofore limitations and restrictions as to the type of bonding that is appropriate.

The inventive structure also permits the leads for providing means of connection and interconnection between devices, components and the respective power plane, to be more dense. Even though these circuits and the devices attached to them are getting smaller and smaller, the power needs to operate them is increasing. Therefore, the present structure permits a significant advantage.

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As has been described hereinabove, an insulation and a circuit pattern can be applied to both sides of a copper-INVAR-copper metal carrier layer. In a preferred arrangement, the copper-INVAR-copper metal carrier layer functions as a ground plane, and circuit lines that are ground potential are connected to this carrier layer.

Since a major part of this structure is metal, an efficient thermal conduction is obtained.

With a multilayer arrangement of the inventive structure, the interleaved copper-INVAR-copper metal carrier planes form effective shields for the circuits from stray fields, particularly when these metal carrier planes are used for ground potential connections.

The polyimide as described herein that is suitable for use with a structure according to the invention is manufactured commercially by DuPont de Nemours, E. I. and Company and is identified as DuPont Polyimide 5878. KOVAR is a registered trademark of Westinghouse Electric Corp.

Claims

1. An electronic package assembly, comprising:
a flexible carrier layer formed of a material that is electrically conductive and has a coefficient of thermal expansion that is close to that of a particular electronic device to be bonded to this electronic package;
a layer of electrically insulating low modulus material formed as a thin film on and supported by said flexible carrier layer material;
an electrical circuit formed on and supported by said layer of electrically insulating low modulus material, including conductors of electrically conductive material in a predetermined pattern;
an electronic device bonded to said electrical circuit in a predetermined location to be operatively functional with said electrical circuit; and
at least one via formed through said layer of electrically insulating low modulus material for connecting said electrical circuit at a preselected location to said flexible carrier layer of electrically conductive material.

2. The electronic package assembly as described in claim 1 wherein said flexible carrier layer is formed from a material from the group including Invar, copper-Invar-copper, Kovar and copper-Kovar-copper.

3. The electronic package assembly as described in claim 1 or 2 wherein said layer of electrically insulating material consists of a polyimide.

4. The electronic package assembly as described in claim 1 or 2 wherein said layer of electrically insulating material includes Teflon.

5. A method of making an electronic package assembly, comprising the steps of:
providing a flexible carrier layer of an electrically conductive material with a coefficient of thermal expansion that is close to that of a particular electronic device to be bonded to this electronic package;
forming on said flexible carrier layer a thin film layer of electrically insulating low modulus material;
forming vias through said layer of electrically insulating low modulus material at predetermined locations to communicate with said flexible carrier layer;
metallizing said layer of electrically insulating low modulus material and said vias;
forming an electrical circuit from said metallization; and
bonding an electronic device to said electrical circuit in a predetermined location to be operatively functional with said electrical circuit.

6. The method of making an electronic package assembly as described in claim 5 wherein said step of providing a flexible carrier layer of an electrically conductive material includes the use of a material from the group including Invar, copper-Invar-copper, Kovar and copper-Kovar-copper.

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7. The method of making an electronic package assembly as described in claim 5 or 6 wherein said step of forming vias through said layer of insulating low modulus material includes the steps of masking and etching.

8. The method of making an electronic package assembly as described in any one of claims 5 to 7 wherein said step of metallizing said layer of insulating low modulus material comprises an evaporation process.

9. The method of making an electronic package assembly as described in any one of the preceding claims 5 to 8 wherein said step of forming an electrical circuit from said metallization comprises a photolithographic process.

10. The method of making an electronic package assembly as described in any of the preceding claims 5 to 9 wherein said layer of insulating low modulus material includes a preselected polyimide; said metallizing step includes the use of a preselected chromium-copper-chromium material with thicknesses in the order of 20 nm, 8000 nm, and 20 nm, respectively; and said step of bonding an electronic device to said electrical circuit includes using a Controlled Collapse Chip Connection process.

Patentansprüche

1. Elektronische Packungsanordnung mit:
einer biegsamen Trägerschicht, die aus einem Material hergestellt ist, das elektrisch leitend ist und einen thermischen Ausdehnungskoeffizienten besitzt, der nahe bei demjenigen eines speziellen elektronischen Bausteins liegt, der an diese elektronische Packung gebondet werden soll;
einer Schicht aus elektrisch isolierendem Material mit niedrigem Modul, die als dünner Film auf der Schicht aus biegsamem Trägermaterial hergestellt und von dieser getragen wird;
einer elektrischen Schaltung, die auf dieser Schicht aus elektrisch isolierendem Material mit niedrigem Modul hergestellt und von dieser getragen wird und die in einem vorher festgelegten Muster elektrische Leiter aus elektrisch leitendem Material enthält;
einem elektronischen Baustein, der an einer vorher festgelegten Stelle an die elektrische Schaltung gebondet ist, um in der elektrischen Schaltung eine Funktion auszuführen; und
mindestens einer Durchverbindung, die durch die Schicht aus elektrisch isolierendem Material mit niedrigem Modul hindurch hergestellt wird, um die elektrische Schaltung an einer vorher festgelegten Stelle mit der biegsamen Trägerschicht aus elektrisch leitendem Material zu verbinden.

2. Elektronische Packungsanordnung gemäß Anspruch 1, wobei die biegsame Trägerschicht aus einem Material aus der Gruppe, die Invar, Kupfer-Invar-Kupfer, Kovar und Kupfer-Kovar-Kupfer enthält, hergestellt wird.

3. Elektronische Packungsanordnung gemäß Anspruch 1 oder 2, wobei die Schicht aus elektrisch isolierendem Material aus einem Polyimid besteht.

4. Elektronische Packungsanordnung gemäß Anspruch 1 oder 2, wobei die Schicht aus elektrisch isolierendem Material Teflon enthält.

5. Verfahren zur Herstellung einer elektronischen Packungsanordnung, das folgende Schritte umfaßt:
Herstellung einer biegsamen Trägerschicht aus einem elektrisch leitenden Material mit einem thermischen Ausdehnungskoeffizienten, der nahe bei demjenigen eines speziellen elektronischen Bausteins liegt, der an diese elektronische Packung gebondet werden soll;
Herstellung einer dünnen Filmschicht aus elektrisch isolierendem Material mit niedrigem Modul auf der biegsamen Trägerschicht;
Herstellung von Durchverbindungen durch die Schicht aus elektrisch isolierendem Material mit niedrigem Modul an vorher festgelegten Stellen, um mit der biegsamen Trägerschicht zu kommunizieren;
Metallisieren der Schicht aus elektrisch isolierendem Material mit niedrigem Modul und der Durchverbindungen;
Herstellung einer elektrischen Schaltung aus der metallisierten Schicht; und
Bonden eines elektronischen Bausteins an die elektrische Schaltung an einer vorher festgelegten Stelle, um in der elektrischen Schaltung eine Funktion auszuführen.

6. Verfahren zur Herstellung einer elektronischen Packungsanordnung gemäß Anspruch 5, wobei der Schritt der Herstellung einer biegsamen Trägerschicht aus einem elektrisch leitenden Material die Verwendung eines Materials aus der Gruppe, die Invar, Kupfer-Invar-Kupfer, Kovar und Kupfer-Kovar-Kupfer enthält, einschließt.

7. Verfahren zur Herstellung einer elektronischen Packungsanordnung gemäß Anspruch 5 oder 6, wobei der Schritt der Herstellung von Durch-

verbindungen durch die Schicht aus isolierendem Material mit niedrigem Modul die Schritte Maskieren und Ätzen einschließt.

8. Verfahren zur Herstellung einer elektronischen Packungsanordnung gemäß einem der Ansprüche 5 bis 7, wobei der Schritt der Metallisierung der Schicht aus isolierendem Material mit niedrigem Modul ein Aufdampfverfahren einschließt.

9. Verfahren zur Herstellung einer elektronischen Packungsanordnung gemäß einem der vorhergehenden Ansprüche 5 bis 8, wobei der Schritt der Herstellung einer elektrischen Schaltung aus der metallisierten Schicht ein fotolithografisches Verfahren einschließt.

10. Verfahren zur Herstellung einer elektronischen Packungsanordnung gemäß einem der vorhergehenden Ansprüche 5 bis 9, wobei die Schicht aus isolierendem Material mit niedrigem Modul ein vorher ausgewähltes Polyimid enthält; der Schritt der Metallisierung die Verwendung eines vorher ausgewählten Chrom-Kupfer-Chrom-Materials mit Dicken in der Größenordnung von 20 nm, 8000 nm bzw. 20 nm enthält; und der Schritt des Bondens eines elektronischen Bausteins an die elektrische Schaltung die Verwendung eines Controlled-Collapse-Chip-Connection-Verfahrens enthält.

Revendications

1. Assemblage électronique comprenant :

une couche de support flexible formée d'un matériau électriquement conducteur et ayant un coefficient de dilatation thermique proche de celui d'un dispositif électronique particulier à relier audit assemblage électronique ;

une couche d'isolant électrique formée d'un matériau à faible coefficient d'élasticité réalisée selon un film mince et supportée par ladite couche de matériau flexible ;

un circuit électrique formé sur, et supporté, par ladite couche d'isolant électrique, comportant des conducteurs en matériau électriquement conducteur selon un dessin pré-déterminé ;

un dispositif électronique soudé audit circuit électrique en un endroit pré-déterminé pour fonctionner avec ledit circuit électrique ; et

au moins une ouverture formée dans ladite couche d'isolant électrique en matériau à faible coefficient d'élasticité pour relier ledit circuit électrique en un endroit pré-déterminé à ladite couche de support flexible de matériau conducteur électrique.

2. Dispositif électronique selon la revendication 1 dans lequel ladite couche de support flexible est formée d'un matériau appartenant au groupe comprenant INVAR, cuivre-INVAR-cuivre, KOVAR et cuivre-KOVAR-cuivre.

3. Dispositif électronique selon la revendication 1 ou 2 dans lequel ladite couche de matériau isolant électrique est formée de polyimide.

4. Dispositif électronique selon la revendication 1 ou 2 dans lequel ladite couche de matériau isolant électrique comprend le Teflon.

5. Procédé de réalisation d'un assemblage électronique comprenant les étapes suivantes :

fourniture d'une couche de support flexible de matériau conducteur électrique ayant un coefficient de dilatation thermique proche de celui d'un dispositif électronique particulier à relier à l'assemblage électronique ;

formation, sur ladite couche de support flexible, d'une couche de film mince de matériau isolant électrique à faible coefficient d'élasticité ;

formation d'ouvertures à travers ladite couche de matériau isolant électrique à faible coefficient d'élasticité en des endroits pré-déterminés pour communiquer avec ladite couche de support flexible ;

métallisation de ladite couche de matériau isolant électrique à faible coefficient d'élasticité et desdites ouvertures ;

formation d'un circuit électrique à partir de ladite métallisation ; et

soudure d'un dispositif électronique audit circuit électrique en un endroit pré-déterminé pour fonctionner avec ledit circuit électrique.

6. Procédé de réalisation d'un assemblage électronique selon la revendication 5 dans lequel ladite étape de fourniture d'une couche de support flexible de matériau conducteur électrique comprend l'utilisation d'un matériau appartenant au groupe comportant INVAR, cuivre-INVAR-cuivre, KOVAR, et cuivre-KOVAR-cuivre.

7. Procédé de réalisation d'un dispositif électronique selon la revendication 5 ou 6 dans lequel ladite étape de formation d'ouvertures à travers ladite couche d'isolant en matériau à faible coefficient d'élasticité comprend les étapes de masquage et décapage.

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8. Procédé de réalisation d'un ensemble électronique selon l'une quelconque des revendications 5 à 7 dans lequel ladite étape de métallisation de ladite couche d'isolant en matériau à faible coefficient d'élasticité comprend un processus d'évaporation.

9. Procédé de réalisation d'un ensemble électronique selon l'une quelconque des revendications 5 à 8 dans lequel ladite étape de formation d'un circuit électronique à partir de ladite métallisation comprend un processus de photo-lithographie.

10. Procédé de réalisation d'un ensemble électronique selon l'une quelconque des revendications 5 à 9 dans lequel ladite couche d'isolant en matériau à faible coefficient d'élasticité comprend un polyimide pré-sélectionné ; ladite étape de métallisation comprend l'utilisation d'un matériau pré-sélectionné de chrome-cuivre-chrome ayant une épaisseur de l'ordre de 20 nm, 8000 nm, et 20 nm respectivement ; et ladite étape de soudure d'un dispositif électronique audit circuit électrique comprend l'utilisation du procédé de jonction d'une plaquette de semiconducteurs par affaissement contrôlé.