

ABSTRACT OF THE DISCLOSURE

A memory device has a plurality of power rails, including: a first power rail for transmitting a high power voltage, a second power rail for transmitting a low power voltage, a third power rail for selectively receiving the high power voltage from the first power rail through a first dynamic voltage and frequency scaling (DVFS) switch and for selectively receiving the low power voltage from the second power rail through a second DVFS switch, a fourth power rail connected to a first power gating (PG) switch to selectively receive the high power voltage or the low power voltage from the third power rail, and a first circuit block connected to the fourth power rail to receive a power voltage to which the DVFS and PG are applied. When power gating is applied, supply of the power voltage to the fourth power rail is blocked.

FIG. 1