Description

The invention relates to an apparatus for reproducing digital information *via* a transmission medium in the form of an optically readable record carrier on which digital information is stored in the form of a track of optically detectable areas which alternate with intermediate areas, which apparatus comprises:

oscillator means for generating a clock signal,

means for generating a decision level, and

means for comparing the signal obtained *via* the transmission medium with the decision level in order to restore the digital signal.

Such apparatus is used in the "compact-disc digital audio" player which is commercially available from N.V Philips' Gloeilampenfabrieken under the type designation CD 100. The integrated circuits used in this player are described in the article "ICs for Compact Disc Decoders" in Electronic Components and Applications, Vol. 4, No. 3, May 1982, pp 131—141. In this article it is described that in the demodulator IC a signal is generated which is a measure of the phase difference between the clock signal and the time base of the reproduced signal, which is determined by the intersections of the reproduced signal and the decision level, in order to lock the phase of the clock signal to said intersections by means of a phase-locked loop. This signal which is a measure of the phase difference is determined by measuring the time intervals between said intersections and the edges of the clock signal. When the reproduced signal is comparatively weak, for example owing to fingermarks on the disc, this time measurement becomes very unreliable because then it responds to intersections of the decision level (caused by) noise and the like. This gives rise to an erroneous phase detection and a consequent detuning of the clock oscillator. In order to mitigate these problems the phase detection is therefore interrupted in the event of the signal drop-out. However, this interruption demands some time, so that nevertheless the clock oscillator may be detuned.

It is the object of the invention to provide an apparatus of the type specified in the opening paragraph in which a phase detection is applied which is less susceptible to disturbances during signal drop-outs.

To this end the invention is characterized by means for sampling the amplitude of the reproduced signal on both sides of first instants at which the reproduced signal intersects the decision level in a first of two possible directions, which sampling is effected in phase-synchronism with the clock signal, and

means for generating a first signal which is a measure of the difference in amplitude between the decision level and an interpolation of the samples on both sides of said first instants and which is a measure of the phase difference between the clock signal and the restored digital signals.

When the phase difference is detected in accordance with the invention the first signals representing the phase difference is proportional to the slope of the reproduced signal around the intersections and hence proportional to the amplitude of this reproduced signal. In the case of signal drop-outs this amplitude becomes low, so that the first signal is also small and can hardly cause a detuning of the clock oscillator.

It should be noted that EP—A—109,837 falling within the terms of Art. 54(3) EPC, describes an apparatus which largely resembles the apparatus claimed, and which is aimed at reproducing digital information from a transmission medium in the form of a magnetic tape. The possibility to use this apparatus with optical recording media is not mentioned.

The apparatus in accordance with the invention may be further characterized in that the means for sampling are adapted to sample the amplitude of the reproduced signal on both sides of second instants at which the reproduced signal intersects the decision level in a second direction opposite to the first direction, and a second signal is generated which is a measure of the difference in amplitude between the decision level and an interpolation of the samples on both sides of said second instants.

With respect to the generation of the first and the second signals the apparatus in accordance with the invention may be further characterized in that the first and the second signal are generated in such a manner that the amplitudes of said signals satisfy the relationship $k+l-2m$, where k and l are the amplitudes of the samples on both sides of the first or the second instants and m is the amplitude of the decision level.

As regards the control of the clock oscillator the apparatus in accordance with the invention may be characterized in that a signal which is proportional to the difference between the first and the second signal is applied to the oscillator means for controlling said oscillator means in such a manner that the phase of the clock signal is locked to the time base of the reproduced digital signal.

For an optimum restoration of the digital signal the decision level must be situated as symmetrically as possible. In order to achieve this the apparatus in accordance with the invention may be characterized in that a signal which is proportional to the sum of the first and the second signal is applied to the means for generating the decision level as a negative-feedback signal.

The sum of the first and the second signal is proportional to the difference between the phase differences between the clock signal and the intersections with the decision level in both directions. This difference is minimized by the negative feedback.

The invention will now be described in more detail, by way of example, with reference to the accompanying drawings, in which

Fig. 1 is a block diagram of an apparatus in which the phase detector in accordance with the invention may be used,

Fig. 2 shows an example of the detector 19 of the apparatus shown in Fig. 1,

Fig. 3 shows some diagrams to explain the operation of the detector shown in Fig. 2,

Fig. 4 is a diagram to explain the operation of the circuit shown in Fig. 5,

Fig. 5 shows an example of that part of the circuit 37 (Fig. 1) which supplies the signal SL,

Fig. 6 is a diagram to explain the operation of the circuit shown in Fig. 7, and

Fig. 7 shows example of the phase detector 58 (Fig. 1) in accordance with the invention.

Fig. 1 shows an apparatus in which the phase detector in accordance with the invention may be used.

In this Figure a disc-shaped record carrier 1 is shown in a schematic cross-sectional view. This record carrier comprises a substrate 2 in which a track structure is formed, which structure comprises pits 3 and intermediate areas 4. This relief-type track structure is coated with a reflecting layer 5 and a transparent protective layer 6. The information contained in the relief-type track structure is read in that a laser beam generated by a laser 7 is projected and focused on the tracks *via* a lens system 8, the reflected beam being projected on an in line array of four optical detectors 11a, 11b, 11c and 11d *via* a semi-transparent mirror 9 and a beam splitter 10. The currents supplied by these photodetectors are converted into the signal voltage V_1, V_2, V_3 and V_4 by means of a current-voltage converter 12.

For a correct read-out the focusing of the lens system 8 is controlled in a manner, not shown by means of a focusing control signal FE'. For radial tracking the radial location of the spot produced by the laser beam is controlled by means of a radial control signal RE'. This is a fine-control system. Coarse control is obtained (in a manner not shown) by moving the entire optical system 7, 8, 9, 10, 11 in a radial direction under command of a control signal CE'.

The control signals CE', RE' and FE' are derived from the signal voltages V_1, V_2, V_3 and V_4. In addition to the sum $V_1+V_2+V_3+V_4$ required for recovering the high-frequency data signal, the signal $(V_1+V_4)-(V_2+V_3)$ is required for the signal FE' and the signal $(V_1+V_2)-(V_3+V_4)$ is required for the signal CE' and the signal RE'. All these control signals can be derived from three signals A', B' and C' which are obtained by combining the signals V_1, V_2, V_3 and V_4. In the present embodiment these signals are related as follows:

$$A'=V_1+V_2$$
$$B'=V_3+V_4$$
$$C'=V_1+V_4.$$

The combination of the signals V_1, V_2, V_3 and V_4 described in the foregoing is obtained by means of a matrix 13. This combination has the advantage that only three instead of four signals must be digitized, so that a lower local clock frequency can be used than would be the case if these signals are digitized serially. For this purpose the signals A', B' and C' are converted into serial form by means of a multiplexer 14, they are digitized in an analog-to-digital converter 15 and they are reconverted into parallel form to obtain the corresponding digital samples A, B and C by means of a demultiplexer 16. The multiplexer 14, the analog-to-digital converter 15 and the demultiplexer 16 receive clock signals from a clock-signal generating circuit 17, which supplies the required clock signals in the correct phase relationship under control of an oscillator 18 in such a manner that the samples A, B and C are supplied in synchronism with the bit frequency of the data signal.

For generating the various control signals it is important to suppress the data-signal spectrum as far as possible. This is achieved by selecting samples in synchronism with the data pattern (pits and intermediate areas) so that the instantaneous sampling frequency becomes equal to the instantaneous frequency of the data signal. For this purpose one sample for each pit (3) and for each intermediate area (4) is selected from each of the samples A, B and C and, in order to minimize the effect of the optical transfer function of the read-out (the signal amplitude is a function of the location of the projected laser beam relative to the pits and decreases towards the edges of the pits), the samples are taken only for pits and intermediate areas which are longer than a specific number of clock periods, in the present example longer than 5 clock periods. For this purpose a detector 19 (which will be described in more detail with reference to Fig. 2) generates a pulse on an output 20 when the sixth sample in one pit is detected and a pulse on output 21 when the sixth sample in one intermediate area is detected. The detector 19 receives the clock signals from the oscillator 18 on an input 22 and the digital sum of the signals A and B, obtained by means of the adder 25 and equalized by means of the circuit 24, on an input 23.

The samples A, B and C are each delayed by three clock periods (τ) of the oscillator 18 by means of delay networks 26, 27 and 28 respectively, are equalized by means of the equalizers 29, 30 and 31 respectively, and are applied to the hold circuits 32 and 33, 34 and 35, and 36 respectively. The hold circuits 32, 34 and 36 are clocked by the signal on output 21 of the detector 19 and the hold circuits 33 and 35 by the signal on output 20. During each intermediate area longer than five periods the third samples 2, and 6 and of the samples A, B and C respectively then appears on the outputs 38, 40 and 42 respectively of the hold circuits 32, 34 and 36 respectively and during each pit which is longer than five clock periods the third samples $\overline{a}$ and $\overline{b}$ of the samples A and B respectively then appear on the outpus 39 and 41 respectively of the hold circuits 33 and 35 respectively.

The signals a, $\overline{a}$, b, $\overline{b}$, and c are applied to a processing circuit 37, which supplies the signals RE, CE and FE on outputs 43, 44 and 45 respectively, and a signal TL representing a loss of track, a signal DO indicating a signal drop-out, a signal HFL indicating that the level of the high-frequency

data signal is too low, and a signal SL which is a decision level for the data-signal processing, on outputs 46, 47, 48 and 49, respectively. The signals RE, CE and FE are converted into analog signals by means of digital-to-analog converters 50, 51 and 52 and subsequently they are amplified by the amplifier 53, 54 and 55 to form the analog control signals RE', CE' and FE' for focusing and tracking control.

The sum of the signals A+B formed by means of the adder 25 and the equalizer 24 is not only applied to a detector 19 but also to a comparator 56 which also receives the decision level SL for restoring the digital data signal and applying it to an output 57 and to a phase comparator circuit 58, which compares the phase of the samples A+B with the phase of the data signal on the record carrier 1 and which supplies a signal which is a measure of this phase to an output 59 and a signal which is a measure of the asymmetry of the signal A+B to an output 60, which last-mentioned signal is applied to a circuit 37, which will be described in more detail with reference to Fig. 8. The phase-error signal on output 59 controls the oscillator 18 *via* a low-pass filter 61.

Fig. 2 shows an example of the detector 19 in the apparatus shown in Fig. 1, and Fig. 3 shows some diagrams to explain the operation of the circuit shown in Fig. 2. In the circuit shown in Fig. 2 the signal A+B from the equalizer 24 is applied to a high-pass filter 62 via an input 23 in order to remove the low-frequency components, thereby enabling the digital data signal to be restored by means of a simple comparator 63. The edges of the rectangular data signal are detected by means of a circuit 64, for example a differentiator. This edge detector starts a counter 65 which counts the clock pulses (from the oscillator 18) on its input 22 from the instant defined by the pulses from the edge detector 64. A decoder circuit 66 decodes a specific count, in the present example six. When the count "six" is reached, the pulses are applied to AND-gates 67 and 68. The gate 67 also receives the restored data signal on an inverting input and the gate 68 receives this signal on a non-inverting input. As a result of this, a pulse will appear on output 21 when the count "six" is reached during a positive data signal (3c) and on output 20 when the count "six" is reached during a negative data signal.

To illustrate this, Fig. 3a shows a part of a data track on the record carrier, which track comprises pits 3 and intermediate areas 4 between these pits. Fig. 3b shows the samples A+B originating from the track shown in Fig. 3a. Fig. 3c shows the restored data signal after the comparator 63, which is a substantially rectangular signal with a period corresponding to the length of the pits and intermediate areas. Fig. 3d shows the starting pulses for the counter 65 formed on the edges of the data signal, which counter counts the pulses of the clock signal shown in Fig. 3e. The counter 65 supplies a pulse each time the count "six" is reached and for a positive data signal (Fig. 3c), *i.e.* during an intermediate area, a pulse will appear on output 21 (Fig. 3f), whilst for a negative data signal, *i.e.* during a pit, the pulse will appear on output 20 (Fig. 3g). The signals A, B and C, which have been delayed by three clock periods, are thus sampled. Fig. 3h shows the signal A which has been delayed by three clock periods and for which the hold circuit 32 (Fig. 1) holds the third sample from each intermediate area longer than five clock periods (signal shown in Fig. 3i) and, the sample and hold circuit 33 holds the third sample from each pit longer than five clock periods (signal shown in Fig. 3j).

In the apparatus shown in Fig. 1 the data signal A+B is applied to a comparator 56 for restoring the data signal. In this comparator the samples A+B are compared with a decision level SL appearing on output 49 of the circuit 37. This decision level SL should be such that the restored data signal exactly corresponds to the pattern of pits on the disc. As is shown in Fig. 4, the signal A+B varies between the levels a+b and $\bar{a}+\bar{b}$, which are the values of the signal A+B during the third sample of long intermediate areas or pits respectively. A first approach adopted for a decision level SL is halfway between said levels a+b and $\bar{a}+\bar{b}$, so:

$$SL=\tfrac{1}{2}(a+b+\bar{a}+\bar{b}).$$

This approach is correct only if the signal A+B is symmetrical as regards its variation during the intermediate areas or pits, which is not always the case. Therefore, the level must be corrected by a factor α which is a measure of the assymmetry of the signal A+B. For generating this factor α reference is made to Figs. 6 and 7.

Fig. 5 shows an example of that part of the circuit 37 which generates the decision level SL. By means of an adder 79 the sum of the samples a, $\bar{a}$, b, and $\bar{b}$ is determined and this sum is halved by the divider 80. The resulting value

$$\tfrac{1}{2}(a+\bar{a}+b+\bar{b})$$

must be multiplied by a factor α in order to correct for assymmetries. However, multiplying by said factor α means that a fast multiplier must be used in order to cope with comparatively rapid variations of

$$\tfrac{1}{2}(a+b+\bar{a}+\bar{b}).$$

It is more effective to multiply by a factor $\alpha=(1+e)$ instead of by the factor α, which means that a fraction of the output signals of the divide-by-two circuit 80 must be added to said output signal by means of the adder 81. This fraction e is obtained by means of the multiplier 82. *Via* a low-pass filter 83 the factor e is derived from a signal on the output 60 of the phase comparator 58 (Fig. 1). This has the advantage that the multiplier 82 need not be fast, because the factor *e* varies comparatively slowly in comparison with the value

$\frac{1}{2}(a+b+\bar{a}+\bar{b})$.

Another advantage of this solution is that when the levels a+b and $\bar{a}+\bar{b}$ after one long pit and one long intermediate area are known after the control system has become operative, a reasonably reliable decision level

$$SL=\tfrac{1}{2}(a+b+\bar{a}+\bar{b})$$

will appear on output 49 even before the correction factor *e* is known.

Fig. 7 shows an example of the circuit 58 (Fig. 1) for generating a signal which is a measure of the phase error of the clock signal relative to the data recorded on the disc and a signal which is a measure of the assymmetry of the signal A+B and which must be applied to the circuit shown in Fig. 5 for correcting the decision level SL. The operation of the circuit shown in Fig. 7 will be described with reference to Fig. 6, in which $(A+B)_{n-1}$ and $(A+B)_n$ are two consecutive samples of the signal A+B situated on different sides of the decision level SL. Assuming that the analog signal, of which $(A+B)_{n-1}$ and $(A+B)_n$ are two samples, varies linearly between these samples, the point of intersection P_n with said decision level can be determined by linear interpolation.

The relative deviation of this intersection P_n relative to an instant which is situated exactly halfway between the instants at which the samples $(A+B)_{n-1}$ and $(A+B)_n$ appear is then a measure of the instantaneous phase difference between the clock signal with which the instants at which the samples $(A+B)_n$ and $(A+B)_{n-1}$ are synchronized and the edges of the pits 3, and consequently of the instantaneous phase difference with the bit frequency of the recorded data signal. In Fig. 6 this clock signal bears the reference S_c and the phase difference bears the reference φ_n. For the intersection P_m with the decision level SL between the samples $(A+B)_m$ and $(A+B)_{m-1}$ corresponding to the other edges of the pits 3 an instantaneous phase difference φ_p can be determined in the same way.

The sum $\varphi_p+\varphi_n$ is now a measure of the average phase deviation of the two edges and is consequently a measure of the phase error of the clock oscillator 18, whilst the difference between the phase errors φ_p and φ_n is a deviation of the decision level SL from the desired level. Indeed, if the level SL rises, φ_p increases and φ_n decreases, so that the difference $\varphi_p-\varphi_n$ increases in a positive sense. If the level SL decreases below the desired level, this difference $\varphi_p-\varphi_n$ becomes negative.

Therefore, the difference $\varphi_p-\varphi_n$ is a measure of the correction factor *e* for the circuit shown in Fig. 5. The phase difference φ_n and φ_p can be determined as follows by linear interpolation:

$$a\varphi_n=(A+B)_{n-1}+(A+B)_n-2\,SL, \text{ and}$$

$$-a\varphi_p=(A+B)_{m-1}+(A+B)_m-2\,SL$$

where *a* is a factor which depends on the slope of the interpolation line and which is therefore proportional to the amplitude of the data signal being read. The desired signals are generated by means of the circuit shown in Fig. 7. The samples A+B are applied to an input 84 which is connected to a device 85 which delays the sample by one clock period τ, so that the samples $(A+B)_m$ and $(A+B)_{m-1}$ appear on the input and the output respectively of said device in the case of an intersection of the level SL during a positive edge, and the samples $(A+B)_n$ and $(A+B)_{n-1}$ in the case of an intersection during a negative edge. The decision level generated by the circuit shown in Fig. 5 is applied to an input 89. This decision level SL together with the signal on input 84 is applied to a comparator 86 which produces an output signal when the signal on input 84 exceeds the decision level SL, and together with the delayed signal on the output of the delay network 85 the decision level is applied to a comparator 87 which produces an output signal when the decision level SL is higher than the signal on the output of the delay network 85. The output signals of the two comparators 86 and 87 are applied to an AND-gate 90 and a NAND-gate 91 so that the AND-gate 90 produces a signal in the case of an intersection of the decision level SL during a positive edge and the NAND-gate 91 produces an output when the decision level SL is intersected during an negative edge. By means of an adder 88 the signals obtained on both sides of the delay element 85 are added to each other and subsequently twice the decision level SL, which is obtained by means of the multiplier 92, is subtracted therefrom by means of a subtractor circuit 93. The result is sampled by a hold circuit 94 under command of the gate 90 and by a hold circuit 95 on command of the gate 91, so that the signal on the output of the hold circuit 94 is equal to $a\varphi_n$ and the signal on the output of the circuit 95 is equal to $-a\varphi_p$. These signals are subtracted by means of a subtractor circuit 97, so that on the output 59 of this circuit a signal equal to $a(\varphi_n+\varphi_p)$ appears, which is the desired signal which is a measure of the phase error of the *clock* signal, with which signal the oscillator 18 is corrected *via* the low-pass filter 61 in order to ensure that the clock signal has a fixed phase relationship with the recorded data signal. The signals on the outputs of the two hold circuits are added by the adder 96, so that on output 60 of this adder signal equal to $a(\varphi_n-\varphi_p)$ appears, which is the signal which is a measure of the asymmetry. This signal is applied to a device generating the threshold level (Fig. 5), so that a control loop is obtained which controls the height of the threshold level in such a manner that the signal $a(\varphi_n-\varphi_p)$ goes to zero if the phase difference φ_n (Fig. 7) becomes equal to the phase difference φ_p.

The signals appearing on outputs 59 and 60 are proportional to the amplitude of the signal A+B. This has the advantage that during signal dropouts the generated signals become zero, so that the oscillator 18 and device shown in Fig. 6 will

receive no signal instead of a comparatively large spurious signal, which often happens in the customary phase detectors.

Claims

1. An apparatus for reproducing digital information *via* transmission medium in the form of an optically readable record carrier (1) on which digital information is stored in the form of a track of optically detectable areas (3) which alternate with intermediate areas (4), which apparatus comprises:

oscillator means (18) for generating a clock signal,

means (37) for generating a decision level (SL), and

means (56) for comparing the signal obtained *via* the transmission medium with the decision level (SL) in order to restore the digital signal, characterized by

means (58) for sampling the amplitude of the reproduced signal on both sides of first instants at which the reproduced signal intersects the decision level (SL) in a first of two possible directions, which sampling is effected in phase-synchronism with the clock signal, and

means (58) for generating a first signal which is a measure of the difference in amplitude between the decision level (SL) and an interpolation of the samples on both sides of said first instant and which is a measure of the phase difference between the clock signal and the restored digital signal.

2. An apparatus as claimed in Claim 1, characterized in that the means (58) for generating the first signal generate a first signal which complies with the function k+l−2m, where *k* and *l* are the amplitudes of the samples on both sides of the first instants and *m* is the amplitude of the decision level (SL).

3. An apparatus as claimed in Claim 1 or 2, characterized in that said first signal is applied to the oscillator means (18) for controlling said oscillator means (18) in such a manner that the phase of the clock signal is locked to the time base of the reproduced digital signal.

4. An apparatus as claimed in Claim 1 or 2, characterized in that the means (58) for sampling are adapted to sample the amplitude of the reproduced signal on both sides of second instants at which the reproduced signal intersects the decision level (SL) in a second direction opposite to the first direction, and a second signal is generated which is a measure of the difference in amplitude between the decision level and an interpolation of the samples on both sides of said second instants.

5. An apparatus as claimed in Claim 4, characterized in that the first and the second signal are generated in such a manner that their amplitudes satisfy the relationship k+l−2m, where *k* and *l* are the amplitudes of the samples on both sides of the first or the second instants, and *m* is the amplitude of the decision level (SL).

6. An apparatus as claimed in Claim 4 or 5, characterized in that a signal which is proportional to the difference between the first and the second signal is applied to the oscillator means (18) for controlling said oscillator means (18) in such a manner that the phase of the clock signal is locked to the time base of the reproduced digital signal.

7. An apparatus as claimed in Claim 4, 5 or 6, characterized in that a signal which is proportional to the sum of the first and the second signal is applied to the means (37) for generating the decision level as a negative-feedback signal.

8. An apparatus as claimed in Claim 7, characterized in that under command of the clock signal samples of the reproduced signal are taken, which samples are added to the samples which have been delayed by one period of said clock signal, from which sum twice the decision level is substracted, after which the resulting signal is stored in a first hold circuit (94, Fig. 7) after every first instant in order to obtain the first signal and in a second hold circuit (95) after every second instant in order to obtain the second signal.

Patentansprüche

1. Gerät zur Wiedergabe digitaler Information über ein Übertragungsmittel, in Form eines optisch lesbaren Aufzeichnungsträgers (1), auf dem digitale Information in Form einer Spur optisch detektierbarer Gebiete (3) gespeichert ist, die durch Zwischengebiete (4) abgewechselt werden, wobei dieses Gerät folgende Elemente enthält:

Oszillatormittel (18) zum Erzeugen eines Taksignals,

Mittel (37) und Erzeugen eines Entscheidungspegels (SL), und

Mittel (56) zum Vergleichen des über das Übertragungsmittel erhaltene Signals mit dem Entscheidungspegel (SL) zum Wiederherstellen des digitalen Signals, dadurch gekennzeichnet, daß

Mittel (58) zum Abtasten der Amplitude des dargestellten Signals an beiden Seiten der ersten Zeitpunkte, zu denen das dargestellte Signal in einer ersten von zwei möglichen Richtungen den Entscheidungspegel (SL) schneidet, wobei diese Abtastung mit dem Taktsignal phasensyncrhon erfolgt, und

Mittel (58) zum Erzeugen eines ersten Signals vorgesehen sind, das ein Maß für den Amplitudenunterschied zwischen dem Entscheidungspegel (SL) und einer Interpolation jeweils der Abtastungen an beiden Seiten dieser ersten Zeitpunkte sowie ein Maß für den Phasenunterschied zwischen dem Taktsignal und den wiederhergestellten digitalen Signalen ist.

2. Gerät nach Anspruch 1, dadurch gekennzeichnet, daß die Mittel (58) zum Erzeugen des ersten Signals ein erstes Signal erzeugen, das entsprechend der Funktion k+l−2m verläft, worin k und l die Amplituden der Abtastungen an beiden Seiten der ersten Zeitpunkte und m die Amplitude des Entscheidungspegels sind.

receive no signal instead of a comparatively large spurious signal, which often happens in the customary phase detectors.

Claims

1. An apparatus for reproducing digital information *via* transmission medium in the form of an optically readable record carrier (1) on which digital information is stored in the form of a track of optically detectable areas (3) which alternate with intermediate areas (4), which apparatus comprises:

oscillator means (18) for generating a clock signal,

means (37) for generating a decision level (SL), and

means (56) for comparing the signal obtained *via* the transmission medium with the decision level (SL) in order to restore the digital signal, characterized by

means (58) for sampling the amplitude of the reproduced signal on both sides of first instants at which the reproduced signal intersects the decision level (SL) in a first of two possible directions, which sampling is effected in phase-synchronism with the clock signal, and

means (58) for generating a first signal which is a measure of the difference in amplitude between the decision level (SL) and an interpolation of the samples on both sides of said first instant and which is a measure of the phase difference between the clock signal and the restored digital signal.

2. An apparatus as claimed in Claim 1, characterized in that the means (58) for generating the first signal generate a first signal which complies with the function k+l−2m, where *k* and *l* are the amplitudes of the samples on both sides of the first instants and *m* is the amplitude of the decision level (SL).

3. An apparatus as claimed in Claim 1 or 2, characterized in that said first signal is applied to the oscillator means (18) for controlling said oscillator means (18) in such a manner that the phase of the clock signal is locked to the time base of the reproduced digital signal.

4. An apparatus as claimed in Claim 1 or 2, characterized in that the means (58) for sampling are adapted to sample the amplitude of the reproduced signal on both sides of second instants at which the reproduced signal intersects the decision level (SL) in a second direction opposite to the first direction, and a second signal is generated which is a measure of the difference in amplitude between the decision level and an interpolation of the samples on both sides of said second instants.

5. An apparatus as claimed in Claim 4, characterized in that the first and the second signal are generated in such a manner that their amplitudes satisfy the relationship k+l−2m, where *k* and *l* are the amplitudes of the samples on both sides of the first or the second instants, and *m* is the amplitude of the decision level (SL).

6. An apparatus as claimed in Claim 4 or 5, characterized in that a signal which is proportional to the difference between the first and the second signal is applied to the oscillator means (18) for controlling said oscillator means (18) in such a manner that the phase of the clock signal is locked to the time base of the reproduced digital signal.

7. An apparatus as claimed in Claim 4, 5 or 6, characterized in that a signal which is proportional to the sum of the first and the second signal is applied to the means (37) for generating the decision level as a negative-feedback signal.

8. An apparatus as claimed in Claim 7, characterized in that under command of the clock signal samples of the reproduced signal are taken, which samples are added to the samples which have been delayed by one period of said clock signal, from which sum twice the decision level is substracted, after which the resulting signal is stored in a first hold circuit (94, Fig. 7) after every first instant in order to obtain the first signal and in a second hold circuit (95) after every second instant in order to obtain the second signal.

Patentansprüche

1. Gerät zur Wiedergabe digitaler Information über ein Übertragungsmittel, in Form eines optisch lesbaren Aufzeichnungsträgers (1), auf dem digitale Information in Form einer Spur optisch detektierbarer Gebiete (3) gespeichert ist, die durch Zwischengebiete (4) abgewechselt werden, wobei dieses Gerät folgende Elemente enthält:

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Mittel (58) zum Abtasten der Amplitude des dargestellten Signals an beiden Seiten der ersten Zeitpunkte, zu denen das dargestellte Signal in einer ersten von zwei möglichen Richtungen den Entscheidungspegel (SL) schneidet, wobei diese Abtastung mit dem Taktsignal phasensyncrhon erfolgt, und

Mittel (58) zum Erzeugen eines ersten Signals vorgesehen sind, das ein Maß für den Amplitudenunterschied zwischen dem Entscheidungspegel (SL) und einer Interpolation jeweils der Abtastungen an beiden Seiten dieser ersten Zeitpunkte sowie ein Maß für den Phasenunterschied zwischen dem Taktsignal und den wiederhergestellten digitalen Signalen ist.

2. Gerät nach Anspruch 1, dadurch gekennzeichnet, daß die Mittel (58) zum Erzeugen des ersten Signals ein erstes Signal erzeugen, das entsprechend der Funktion k+l−2m verläft, worin k und l die Amplituden der Abtastungen an beiden Seiten der ersten Zeitpunkte und m die Amplitude des Entscheidungspegels sind.

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3. Gerät nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß dieses erste Signal den Oszillatormitteln (18) zur Steuerung dieser Oszillatormittel (18) derart zugeführt wird, daß die Phase des Taktsignals mit der Zeitbasis des dargestellten digitalen Signals verknüpft ist.

4. Gerät nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die Mittel (58) zum Abtasten ebenfalls zum Abtasten der Amplitude des dargestellten Signals an beiden Seiten der zweiten Zeitpunkte eingerichtet sind, zu denen das dargestellte Signal in einer zweiten, der ersten Richtung entgegengesetzten Richtung den Entscheidungspegel (SL) schneidet, und daß ein zweites Signal erzeugt wird, das ein Maß für den Amplitudenunterschied zwischen dem Entscheidungspegel und einer Interpolation jeweils der Abtastungen an beiden Seiten dieser zweiten Zeitpunkte ist.

5. Gerät nach Anspruch 4, dadurch gekennzeichnet, daß das erste und das zweite Signal derart erzeugt werden, daß sie amplitudenmäßig der Beziehung k+l−2m entsprechen, worin k und l die Amplitude der Abtastungen an beiden Seiten der ersten bzw. zweiten Zeitpunkte sind, und m die Amplitude des Entscheidungspegels ist.

6. Gerät nach Anspruch 4 oder 5, dadurch gekennzeichnet, daß ein Signal proportional dem Unterschied zwischen dem ersten und dem zweiten Signal den Oszillatormitteln (18) zur Steuerung dieser Oszillatormittel (18) derart zugeführt wird, daß die Phase des Taktsignals mit der Zeitbasis des dargestellten digitalen Signals verknüpft ist.

7. Gerät nach Anspruch 4, 5 oder 6, dadurch gekennzeichnet, daß ein Signal proportional der Summe des ersten und des zweiten Signals in gegenkoppelndem Sin den Mitteln (37) zum Erzeugen des Entscheidungspegels zugeführt werden.

8. Gerät nach Anspruch 7, dadurch gekennzeichnet, daß unter der Steuerung des Taksignals Abtastungen des dargestellten Signals vorgenommen werden, die bei den um eine Periode dieses Taktsignals verzögerten Abtastungen addiert werden und von denen anschließend der Doppelwert des Entscheidungspegels subtrahiert wird, wonach das so gewonnene Signal jeweils nach dem Auftreten erster Zeitpunkte in einer ersten Halteschaltung (94, Fig. 7) zur Erhaltung des ersten Signals und jeweils nach zweiten Zeitpunkten in einer zweiten Halteschaltung (95) zur Erhaltung des zweiten Signals gespeichert wird.

Revendications

1. Dispositif pour reproduire de l'information numérique par l'intermédiaire d'un milieu de transmission constitué par un support d'enregistrement à lecture optique (1) sur lequel de l'information numérique est stockée sous la forme d'une piste de zones optiquement détectables (3) alternant avec des zones intermédiaires (4), dispositif comportant:

des moyens oscillateurs (18) pour engendrer un signal d'horloge,

des moyens (37) pour engendrer un niveau de décision (SL) et

des moyens pour comparer le signal obtenu par l'intermédiaire du milieu de transmission avec le niveau de décision (SL) afin de restituer le signal numérique, caractérisé par

des moyens (58) pour échantillonner l'amplitude du signal reproduit de part et d'autre de premiers instants où le signal reproduit coupe le niveau de décision (SL) dans une première direction parmi deux direction possibles, échantillonnage qui est effectué en synchronisme de phase avec le signal d'horloge et

des moyens (58) pour engendrer un premier signal qui est une mesure de la différence d'amplitude entre le niveau de décision (SL) et une interpolation des échantillons de part et d'autre desdits premiers instants et qui est une mesure de la différence de phase entre le signal d'horloge et le signal numérique restitué.

2. Dispositif selon la revendication 1, caractérisé en ce que les moyens (58) pour engendrer le premier signal engendrent un premier signal satisfaisant la fonction k+l−2m, où k et l sont les amplitudes des échantillons de part et d'autre des premiers instants et m est l'amplitude du niveau de décision (SL).

3. Dispositif selon la revendication 1 ou 2, caractérisé en ce que ledit premier signal est appliqué aux moyens oscillateurs (18) pour commander lesdits moyens oscillateurs (18) de telle manière que la phase du signal d'horloge soit accrochée à la base de temps du signal numérique reproduit.

4. Dispositif selon la revendication 1 ou 2, caractérisé en ce que les moyens d'échantillonnage (58) sont conçus pour échantillonner l'amplitude du signal reproduit de part et d'autre de seconds instants où le signal reproduit coupe le niveau de décision (SL) dans une seconde direction, opposée à la première et en ce qu'il est engendré un second signal qui est une mesure de la différence d'amplitude entre le niveau de décision et une interpolation des échantillons de part et d'autre desdits seconds instants.

5. Dispositif selon la revendication 4, caractérisé en ce que les premier et second signaux sont engendrés de telle manière que leurs amplitudes satisfassent la relation k+l−2m, où k et l sont des amplitudes des échantillons de part et d'autre des premiers ou des seconds instants et m est l'amplitude du niveau de décision (SL).

6. Dispositif selon la revendication 4 ou 5, caractérisé en ce qu'un signal proportionnel à la différence entre le premier et le second signal est appliqué aux moyens oscillateurs (18), pour commander ces moyens oscillateurs (18) de telle manière que la phase du signal d'horloge soit accrochée à la base de temps du signal numérique reproduit.

7. Dispositif selon la revendication 4, 5 ou 6, caractérisé en ce qu'un signal proportionnel à la somme des premier et second signaux est appliqué comme signal de contreréaction aux moyens (37) pour engendrer le niveau de décision.

8. Dispositif selon la revendication 7, caractérisé en ce que, sous la commande du signal d'horloge,

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sont choisis des échantillons du signal reproduit, qui sont ajoutés aux échantillons retardés d'une période dudit signal d'horloge, somme dont est soustrait le double du niveau de décision, après quoi le signal ainsi obtenu est stocké dans un premier circuit de maintien (94, figure 7) après chaque premier instant, pour permettre d'obtenir le premier signal, et dans un second circuit de maintien (95) après chaque second instant, pour permettre d'obtenir le second signal.

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