

RECEIVING DATA IN A PAGING RECEIVER

The present invention relates to the receiving of data in a paging receiver.

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Generally, when using a paging receiver, if a word synchronization code is missed - for example, in an area of weak field strength or due to a fading phenomenon, etc., self-calling data cannot be received. Therefore, measures for this have been required.

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Ordinary battery saving circuits are used to minimize power consumption by supplying power to an RF (radio frequency) receiver periodically instead of continuously.

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POCSAG (Post Office Code Standardization Advisory Group) code is an exclusive signal code form for data received by paging receivers, in current use throughout the world, and is specified as CCIR recommendation 584.

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There has been known and applied for a long time a battery saving function which depends on the presence/absence of an RF carrier signal. If the carrier signal is checked, the power is successively supplied to the RF receiving unit for a predetermined time, to thus lower in efficiency. A more advanced battery saving method is to individually receive an RF signal in response to a carrier signal.

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In the calling procedure of a known paging receiver, if a predetermined code is missed, a subsequent address code is also missed. That is, under the operation of a battery saving function, a first predetermined code (preamble

data) is searched for, and if the first predetermined code is checked (detected), a second predetermined code is searched for. If the second predetermined code is checked, a subsequent specific address code is detected. Thereafter, a second predetermined code of a succeeding batch is to be searched for. If
5 the second predetermined code is not checked due to the occurrence of an error in the second predetermined code of the succeeding batch, a subsequent address code word is also missed. Such a type of paging receiver is disclosed in U.S. Patent No. 4,370,753.

10 Referring to Figure 3 of the accompanying diagrammatic drawings, the flow chart illustrates a calling procedure utilizing POCSAG code format, the disclosure of U.S. Patent No. 4,370,753 and an ordinary paging receiver which is presently on the market.

15 In a prior art application of battery saving function, a first predetermined code is searched for when a receiver is periodically turned on/off. If the first predetermined code is detected, a second predetermined code is searched for during a predetermined time. If the second predetermined code is not detected within a predetermined time, the calling
20 procedure is returned to the search routine of the initial first predetermined code. If the second predetermined code is detected within the predetermined time, whether a self-address code (a third predetermined code) is transmitted or not is checked by checking self-frame data in batch data. Thereafter, the procedure is returned to the routine which detects a second predetermined
25 code of the next batch data.

In more detail, under the operation of battery saving function, the first predetermined code is searched for in a step 11, and whether the first

predetermined code is detected or not is monitored in a step 12. If the first predetermined code is not detected, the procedure loops in the step 12 until the first predetermined code is detected and if it is detected, the operation advances to a step 13. In the above step 13, a second predetermined code check counter X1 is initialized to search for the second predetermined code during only a predetermined preparation time for checking a second predetermined code, and the battery saving function becomes disabled - that is, the receiver is continuously turned on. This is followed by a step 14 where whether or not the second predetermined code is detected is determined by checking the data being received. If the second predetermined code is not detected in the step 14, the program goes to a step 19 to increase the second predetermined code check counter X1. In a following step 20, whether an increased value of the second predetermined code check counter X1 in the step 19 exceeds a predetermined time or not is monitored. If the increased value exceeds the predetermined time, the operation is returned to the step 11 and if it does not exceed the predetermined time, the operation is returned to the step 14.

In the step 14, if the second predetermined code is detected, the operation advances to a step 15 to initialize a code word counter X2 for checking the number of the received code words in one batch. Next, whether one code word of 32 bit unit has been received or not is checked in a step 16. If one code word has been received, the program goes to a step 17 to search the self-address code (the third predetermined code) among the predetermined self-frame data and increase code word counter X2. This is followed by a step 18 where a point of time to receive the second predetermined code being received next is checked with the increased value of the code word counter X2. In this step, whether the value of the code word counter X2 is 16 or not

is checked since the number of the code words except the second predetermined code in one batch is 16. If it is a point of time to receive the second predetermined code of the next batch, that is, if the value of the code word counter X2 is 16, the procedure is returned to the step 13. Otherwise
5 the procedure is returned to the step 16.

In the returning process from the step 18 to the step 13, if an error which cannot be corrected occurs in the second predetermined code, that is, when the second predetermined code is missed, the program cannot be
10 followed by the step 14. Therefore, the subsequent address code is also missed. Further, when the word synchronization code is missed, a check routine is continuously repeated for a predetermined time.

As described above, in the calling procedure of a prior paging receiver,
15 when the word synchronization code is missed, self-calling data cannot be received.

Preferred embodiments of the invention aim to provide a method for receiving self-calling data in a paging receiver even if a predetermined code
20 such as a word synchronization code is missed.

Another aim is to provide a paging receiver which can improve reception efficiency even if the paging receiver is used in a weak area for field strength or a fading phenomenon is generated.
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In a preferred embodiment of the present invention, in the calling procedure of a process for searching a second predetermined code of a succeeding batch, if an error occurs in the second predetermined code, not the

second predetermined code is searched for but continuously BCH (Bose-Chaudhuri-Hocquenghem) decoding is performed with a succeeding code word by a BCH decoding algorithm. Thus, if a non-error code word is detected in predetermined code words, the second predetermined code in
5 which an error occurs previously is recognized as the normal second predetermined code and a subsequent address code word is searched for. Consequently, even if the second predetermined code is missed, at the normal batch construction, the missed second predetermined code can be compensated by the subsequent code word.

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According to a first aspect of the present invention, there is provided a method of receiving and processing predetermined signals by means of a battery saving circuit in a paging receiver, comprising the steps of:

detecting a first predetermined code of a preamble signal;

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detecting a second predetermined code in a batch subsequent to said first predetermined code and counting a number of third predetermined codes in said batch;

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decoding a second predetermined code of a succeeding batch and checking if an error occurred in said second predetermined code of said succeeding batch;

if an error occurred in said second predetermined code, decoding a third predetermined code of said succeeding batch and checking if an error occurred in said third predetermined code of said succeeding batch;

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if an error did not occur in said third predetermined code, counting a number of the third predetermined codes in said succeeding batch;

if an error occurred in said third predetermined code, checking if a recurrence value of the error is less than a given number; and

counting the number of the third predetermined codes in said succeeding batch if said recurrence value is less than said given number.

5 The method may comprise returning to the first predetermined code detection step if said third predetermined code in said succeeding batch is checked as a continuous logic high or low data in case of said recurrence value being less than a given number, and if not, counting the number of the third predetermined codes in said succeeding batch.

10 Preferably, said second predetermined code is a word synchronization codeword and said third predetermined codes are codewords in a plurality of frames.

15 Preferably, each of said plurality of frames comprises an address and a message codeword.

Preferably, said second and third predetermined codes are decoded by a Bose-Chaudhuri-Hocquenghem (BCH) decoding method.

20 Preferably, said given number is three.

25 According to another aspect of the present invention, there is provided a method of receiving and processing data transmitted in batches wherein each batch comprises a synchronising byte followed by a plurality of codewords, the method comprising the steps of:

- (i) detecting said synchronising byte of a first batch;

- (ii) detecting and counting said codewords of said first batch;
 - (iii) detecting said synchronising byte of a succeeding batch; and
 - 5 (iv) detecting and counting said codewords of said succeeding batch such that, if said synchronising byte thereof is not received without error, synchronisation and processing of the received data proceeds with reference to said codewords.
- 10 The method extends to apparatus for receiving data (e.g. a paging receiver), arranged to operate in accordance with a method according to any of the preceding aspects of the invention.

15 For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to Figures 1, 2, 4 and 5 of the accompanying diagrammatic drawings, in which:

20 Figure 1 is a block diagram of one example of a paging receiver embodying the present invention;

Figure 2 is a diagram of a POCSAG code format for use in embodiments of the present invention;

Figures 4A to 4C make up a flow chart for showing one example of a calling procedure of a paging receiver embodying the present invention; and

Figures 5A and 5B are timing charts illustrating respective calling procedures of the prior art and an embodiment of the present invention.

Referring to Figure 1, an antenna 100 picks up a modulated RF signal for supplying the modulated signal to a receiver 110. The receiver 110 demodulates the signal received from the antenna 100 to produce logic level data, and a decoder 130, receiving the logic level data output from the receiver 110, processes the data. A code memory 190 stores self-address code therein and is read by the decoder 130. The decoder 130 checks an address code in a CAP (Customer Administration Panel) code ROM used as the code memory 190 and the signal output from the receiver 110. If they are judged as a proper calling signal, the decoder 130 displays the received messages on the LCD (Liquid Crystal Display) 120, and stores them in a message memory of the decoder 130. In this case, the message memory is included in an MPU (Micro Processor Unit) 132, since a one-chip processor of 4 bits is used in this embodiment of the invention. The decoder 130 drives an alert circuit 170 or a vibrator 180 through a driver 140 in response to the received calling information. A call indicator 150 is driven in response to an on/off period of an alert signal and a lamp 160 is for back-lighting the LCD 120. The decoder 130 has also a memory/normal mode selection switch 240 and a read key switch 230 outside thereof.

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The memory mode is a silent mode which drives the vibrator 180 rather than the alert 170 if a calling signal is detected. The read key switch 230 is to recall received messages stored in the memory within the decoder

130 and, when the alert 170 or the vibrator 180 is driven, this is forcibly stopped. A DC-DC converter 220 generates a power source for use in the decoder 130 by using a battery 200 having a limited power capacity and a switch 210 is for power on/off of the battery 200. Numeral 111 indicates a
5 reception data line for supplying data output from the receiver 110 to the decoder 130, and a numeral 112 indicates a battery saving signal line for supplying a signal output from the decoder 130 to the receiver 110.

Referring to Figure 2, a preamble signal 250 detects a received signal
10 and is used for synchronizing a clock bit with the received signal. The preamble signal 250 is called a "first predetermined code" in this embodiment of the invention. A word synchronization code word 260 is used to adjust the word synchronization of a code word which consists of an address, a message and an idle code word signal, and is called a "second predetermined code" in
15 this embodiment of the invention. The first predetermined code is an inverted signal of 101010 and is required to comprise a transmission of at least 576 bits according to the POCSAG standard (CCIR 584), so as to enable operation of a battery saving circuit. This is to enable detection of the first predetermined code in the decoder 130, even if the receiver 110 is turned on
20 or off in response to supplying the battery saving signal (for example, 64 bits turning on and 512 bits turning off) to the receiver 110.

A POCSAG code is constructed as a batch structure which consists of a word synchronization code word (a second predetermined code) of 32 bits
25 followed by 8 frames. Each individual frame consists of two code words, that is, an address code word of 32 bits and a message code word of 32 bits. It will be appreciated that the batch structure is thus composed of 17 code words of 32 bit unit. Each one code word for the word synchronization, address,

message and idle code words, consists of an information bit of 21 bits, a BCH parity bit of 10 bits occurring by BCH-decoding the above data of 21 bits, and an even parity bit of 1 bit for the above data of 31 bits (21 + 10). Therefore, one code word becomes 32 bits.

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An aforementioned BCH encoding algorithm is processed by the generation of [31.21 BCH + parity] code word specified on the POCSAG code. A brief description is given of the processing method of this expression.

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Each code word of respective 32 bits has an information bit of 21 bits which is connected to a polynomial coefficient X^{31} through X^{11} . A syndrome table is made by dividing the polynomial coefficient by a predetermined syndrome generating polynomial ($X^{10} + X^9 + X^8 + X^6 + X^5 + X^3 + 1$)

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by means of a modulo-2 method. A calculated syndrome table corresponding to the respective information bit of 21 bits is as shown in Table 1.

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The syndrome value corresponding to the respective information bit can generate 10 bits from maximum X^9 to minimum X^0 because of dividing the polynomial by the polynomial ($X^{10} + X^9 + X^8 + X^6 + X^5 + X^3 + 1$) by means of the modulo-2. Thus, the respective syndrome table is composed of the data of 10 bits.

TABLE - 1		
	BIT NO.	SYNDROME VALUE
5	X^{31}	1110110100
	X^{30}	0111011010
	X^{29}	0011101101
	X^{28}	1111000010
	X^{27}	0111100001
10	X^{26}	1101000100
	X^{25}	0110100010
	X^{24}	0011010001
	X^{23}	1111011100
	X^{22}	0111101110
15	X^{21}	0011110111
	X^{20}	1111001111
	X^{19}	1001010011
	X^{18}	1010011101
	X^{17}	1011111010
20	X^{16}	0101111101
	X^{15}	1100001010
	X^{14}	0110000101
	X^{13}	1101110110
	X^{12}	0110111011
25	X^{11}	1101101001

In the transmitter, the information bit of 21 bits to be transmitted is added to the BCH parity bit of 10 bits being generated after BCH-encoding the information bit of 21 bits using the syndrome table of the Table-1. Thus, the data of 31 bits is made, and the even parity bit of 1 bit is added by using this data of 31 bits. Therefore, the code word of 32 bit unit is transmitted as the batch structure. While in the paging receiver, the BCH parity is again made by BCH-decoding the received code word using the syndrome table of Table-1. Then, the presence/absence of error and need for correction thereof are judged on the basis of the BCH parity bit and the received parity bit.

The BCH decoding method performed in the paging receiver is divided into two main classes. One is a decoding by software and the other is a decoding by hardware. In accordance with the present embodiment of the invention, since the one-chip microprocessor HD40L4808H 131 of 4 bits is used in the decoder 130, a decoding method by software is applied. Further, the error of various bits can be corrected by the combination of Table-1, though, in this embodiment of the invention, an error up to 2 bits (including random and burst) is corrected.

In the preferred embodiment of the present invention so far described, the batch data is checked by using the BCH decoding algorithm. Since the word synchronization, address, message and idle code words of the POCSAG code are all constructed with the BCH [31, 21 + parity] structure, rather than search for the second predetermined code (the word synchronization code word) as shown in Figure 3, the presence/absence of error is checked by the BCH decoding algorithm as shown in Figure 4.

Referring to Figures 4A to 4C, a BCH error counter X3 is added for checking the number of BCH errors. Moreover, it should be appreciated that the battery saving function according to this embodiment of the present invention is to use a POCSAG code, and the POCSAG code is originally
5 constructed to enable a battery saving function to be performed.

The flow chart portion of Figure 4A is generally similar to that of Figure 3, with some additions. Thus, referring to Figure 4A, under the operation of battery saving function, a first predetermined code is searched for
10 in a step 21, and whether the first predetermined code is detected or not is monitored in a step 22. If the first predetermined code is not detected, the procedure loops in the step 22 until the first predetermined code is detected and if it is detected, the operation advances to a step 23. In the step 23, a
15 second predetermined code check counter X1 is initialized to search for the second predetermined code during only a preparation time for checking a second predetermined code, and the battery saving function becomes disabled, that is, the receiver is continuously turned on. This is followed by a step 24
where whether or not the second predetermined code is detected is determined by checking the data being received. If the second predetermined code is not
20 detected in the step 24, the program goes to a step 29 to increase the second predetermined code check counter X1. In a following step 30, whether an increased value of the second predetermined code check counter X1 in the step 29 exceeds a predetermined time or not is monitored. If the increased
value exceeds the predetermined time value, the operation is returned to the
25 step 21 and if it does not exceed the predetermined time value, the operation is returned to the step 24.

In step 24, if the second predetermined code is detected, the operation advances to a step 25 to initialize a code word counter X2 for checking the number of the received code words in one batch. Next, whether one code word of 32 bit unit has been received or not is checked in a step 26. If one
5 code word has been received, the program goes to a step 27 to search a self-address code (a third predetermined code) among the predetermined self-frame data and increase a code word counter X2. This is followed by a step 28 where whether a point of time to receive the second predetermined code being received next or not is checked with the increased value of the code word
10 counter X2. In this step, whether the value of the code word counter X2 is 16 or not is checked since the number of the code words except the second predetermined code in the batch is 16. If it is a point of time to receive the second predetermined code of the next batch, that is, if the value of the code word counter X2 is 16, the procedure is returned to a step 31 of Figure 4B.
15 Otherwise, the procedure is returned to the step 26 of Figure 4A.

In prior systems, if it is the point of time to receive the second predetermined code of the next batch, the step 28 is followed by the step 23 to search for the second predetermined code. However, in the present
20 embodiment of the invention, it is followed by the step 31 to overcome the deficiencies of the prior systems. From the step 31, processes searching for a dummy synchronization code are performed by using the above-mentioned BCH decoding algorithm.

25 In the step 31, the BCH error counter X3, which is increased by one whenever an unknown error (i.e. an error which cannot be corrected) occurs after BCH-decoding one code word, is initialized ($X3 = 0$), and a non-error flag NEFLG which shows the reception of a non-error code word data is

cleared (NEFLG = 0). This is followed by a step 32 of Figure 4B where whether one code word of 32 bits has been received or not is monitored. If the data of 32 bits has been received, the procedure advances to a step 33 of Figure 4B, to BCH-decode the code word of 32 bits and if they are not
5 received, the procedure is returned to the step 32. Next, in a step 34 of Figure 4B, whether an error which cannot be corrected occurs or not is checked as a result of BCH decoding in the step 33. If an error does not occur or an error which can be corrected occurs, the program goes to a step 42 to set the non-error flag NEFLG (NEFLG = 1) and then goes to a step 35
10 of Figure 4B. If the error which cannot be corrected occurs in the step 34, the procedure is transferred directly to the step 35 without the step 42.

From the step 35, processes similar to the prior systems checking self-frame data in the batch data are performed. In the step 35, the code word
15 counter X2 for counting the number of the received code words in the batch data is initialized (X2 = 0). Then, whether or not one code word of 32 bit unit has been received is determined in a step 36 of Figure 4C. If the code word of 32 bits is received, the procedure advances to a step 37 of Figure 4C to BCH-decode the code word of 32 bits. In a step 38 of Figure 4C, whether
20 an error which cannot be corrected occurs or not is checked. If an error which cannot be corrected occurs, the procedure goes to a step 43 of Figure 4C, to check the non-error flag NEFLG, which shows the reception of non-error data or an error code word capable of being corrected. If non-error data or an error code word capable of being corrected has been received, the procedure
25 goes to a step 40 of Figure 4C. Otherwise, the procedure goes to a step 44 of Figure 4C to increase the BCH error counter X3 by one. Then, in a step 45 of Figure 4C, whether the increased value of the BCH error counter X3 is more than 3, that is, the code word which cannot be corrected is

continuously received more than three times or not is checked. If the code word which cannot be corrected is continuously received more than three times, the operation is returned to the step 23 of Figure 4A to search for the second predetermined code and otherwise, the operation goes to a step 46 of Figure 4C to check if the received data of 32 bits is continuous logic "high" or "low". If all the data are judged as logic "high" or "low", the program is returned to the step 21 of Figure 4A to search for the first predetermined code since it is judged that there are no data to be received any more. Otherwise, the program then advances to the step 40.

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In the step 38, if a non-error or an error capable of being corrected occurs, the operation advances to a step 39 of Figure 4C to set the non-error flag NEFLG - in this case, it is confirmed that the data which do not have an error have been received. In the step 40, the self-address code (the third predetermined code) among the predetermined self-frame data is searched for and the code word counter X2 is increased. This is followed by a step 41 of Figure 4C to see if it is a point of time to receive the second predetermined code being received next with the increased value of the code word counter X2. In this step, whether or not the value of the code word counter X2 is 16 is checked since the number of code words except the second predetermined code in the batch is 16. If it is the time to receive the next batch, the procedure is returned to the step 31 of Figure 4B. Otherwise, the procedure is returned to the step 36 to receive the next code word.

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In the step 18 of the prior systems as shown in Figure 3, if it is the time to receive the second predetermined code of the next batch, the operation is returned to the step 13 to search for only the second predetermined code. Thus, if the second predetermined code is not detected, the step 15 is not

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performed. However, according to the embodiment of the present invention as shown in Figure 4, in the step 28, if it is time to receive the second predetermined code of the next batch, the operation advances to the step 31 to initialize the BCH error counter X3 and clear non-error flag NEFLG. Then, rather than search for the predetermined code as in the prior art, the synchronization of a dummy frame is checked by checking an error by BCH decoding. Therefore, if data which cannot be decoded is received, caused by fading phenomenon in the second predetermined code of a signal being transmitted, the procedure goes to the step 35 of Figure 4B to check the code word in the batch data. Thus, if at least one among three code words in the batch data is received without an error as shown in the step 45 of Figure 4C, the procedure recognizes that the frame synchronization is to be adjusted. Therefore, even if the second predetermined code is missed, the problem of also missing the batch data can be overcome.

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Referring to Figures 5A and 5B, there are shown timing charts for showing a difference in receiving data in an embodiment of the present invention and the prior art. Figures 5A and 5B have the same transmitted data format and show a difference when a code which cannot be corrected is present in a second batch data as received. Figure 5A shows a timing chart of a calling procedure according to a prior art example. In Figure 5A, preamble data is received, while performing a battery saving function with a predetermined period, before data is received. If a first predetermined code is checked at time slot 510, a second predetermined code is searched for and the second predetermined code is checked (detected) at time slot 511. Then, self-frame data in the batch data is received at time slot 512. Thereafter, the last frame data, that is 16th code word, is checked and the second predetermined code of the next batch is searched for at time slot 513. In this

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case, since the unknown code is forcibly transmitted, the second predetermined code is not detected and the detection of the second predetermined code is continuously tried out for a predetermined time. Then, at time slot 514, the procedure proceeds again to check the first predetermined code. Therefore,
5 self-calling address transmitted on self-frame in the second batch cannot be received.

In Figure 5B, in an embodiment of the present invention, processes up to the end of the first batch data are the same as that of Figure 5A. After
10 checking the last frame data of the first batch, however, the second predetermined code is not searched for at the starting point of the second batch data, but the error state is checked by BCH decoding. Then, since an unknown error occurs at the word synchronization code of the second batch and there is no error as a result of BCH decoding with a code word of the
15 second batch, the processing of the predetermined batch data is performed at time slot 524. Therefore, the transmitted self-address code can be received.

As described above, in the case that the second predetermined code is suddenly missed by a fading phenomenon, etc., self-data can be received and
20 calling signal reception efficiency can be improved.

While a preferred embodiment of the invention has been particularly shown and described, it should be appreciated by those skilled in the art that the foregoing and other changes in form and details may be made without
25 departing from the scope of the present invention.

CLAIMS:

1. A method of receiving and processing predetermined signals by means of a battery saving circuit in a paging receiver, comprising the steps of:

5 detecting a first predetermined code of a preamble signal;

detecting a second predetermined code in a batch subsequent to said first predetermined code and counting a number of third predetermined codes in said batch;

10 decoding a second predetermined code of a succeeding batch and checking if an error occurred in said second predetermined code of said succeeding batch;

if an error occurred in said second predetermined code, decoding a third predetermined code of said succeeding batch and checking if an error occurred in said third predetermined code of said succeeding batch;

15 if an error did not occur in said third predetermined code, counting a number of the third predetermined codes in said succeeding batch;

if an error occurred in said third predetermined code, checking if a recurrence value of the error is less than a given number; and

20 counting the number of the third predetermined codes in said succeeding batch if said recurrence value is less than said given number.

2. A method as claimed in claim 1, comprising returning to the first predetermined code detection step if said third predetermined code in said succeeding batch is checked as a continuous logic high or low data in case of said recurrence value being less than a given number, and if not, counting the
25 number of the third predetermined codes in said succeeding batch.



3. A method as claimed in claim 1 or 2, wherein said second predetermined code is a word synchronization codeword and said third predetermined codes are codewords in a plurality of frames.

5 4. A method as claimed in claim 3, wherein each of said plurality of frames comprises an address and a message codeword.

10 5. A method as claimed in claim 1, 2, 3 or 4, wherein said second and third predetermined codes are decoded by a Bose-Chaudhuri-Hocquenghem (BCH) decoding method.

6. A method as claimed in any of claims 1 to 5, wherein said given number is three.

15 7. A method of receiving and processing data transmitted in batches wherein each batch comprises a synchronising byte followed by a plurality of codewords, the method comprising the steps of:

20 (i) detecting said synchronising byte of a first batch;

(ii) detecting and counting said codewords of said first batch;

(iii) detecting said synchronising byte of a succeeding batch; and

25 (iv) detecting and counting said codewords of said succeeding batch such that, if said synchronising byte thereof is not received without error, synchronisation and processing of the received data proceeds with reference to said codewords.



8. A method of receiving and processing data transmitted in batches, the method being substantially as hereinbefore described with reference to Figures 1, 2, 4 and 5 of the accompanying drawings.
- 5 9. Apparatus for receiving data, arranged to operate in accordance with a method according to any of the preceding claims.
10. Apparatus according to claim 9, being a paging receiver.

