WHAT IS CLAIMED IS:

1. A semiconductor package, comprising:

a first base plate, having a first surface, wherein the first surface comprises a first signal transmission region and a second signal transmission region, the first signal transmission region and the second signal transmission region are not connected to each other;

a first semiconductor structure, located on the first surface of the first base plate and electrically connected to the first signal transmission region;

a second base plate, located on the first base plate and comprising a base and a first interconnection surface located on the base, wherein the first interconnection surface of the second base plate is away from the first surface of the first base plate, the first interconnection surface has a first interconnection region and a second interconnection region that communicate with each other, and the first interconnection region is electrically connected to the second signal transmission region;

a filling layer, sealing the first semiconductor structure, the second base plate and the first surface of the first base plate, wherein the first interconnection region is not sealed by the filling layer, the second interconnection region is sealed by the filling layer, and there is a preset height between a top surface of the filling layer on the second interconnection region and the first interconnection region; and

the first surface of the first base plate further comprises a third signal transmission region located between the first signal transmission region and the second signal transmission region, the third signal transmission region comprises a first signal sub-region and a second signal sub-region; the first signal sub-region is connected to the first signal transmission region and located in a close region of the first signal transmission region; and the second signal sub-region is connected to the second signal transmission region and located in a close region of the second signal transmission region, wherein the first signal sub-region and the second signal sub-region are not connected to each other and an electromagnetic shielding structure is between the first signal sub-region of the first base plate and the second signal

sub-region.

2. The semiconductor package of claim 1, wherein the first semiconductor structure is located on the third signal transmission region.

3. The semiconductor package of claim 1, wherein the first interconnection region is electrically connected to the second signal transmission region by means of the second interconnection region.

4. The semiconductor package of claim 1, wherein the first signal transmission region and the second signal transmission region are located at two opposite sides of the first base plate; the first semiconductor structure has a first connection end; the first connection end and the first signal transmission region are located at a same side and connected to each other by using a lead wire; and the second interconnection region and the second signal transmission region are located at a same side and connected to each other by using a lead wire.

5. The semiconductor package of claim 1, wherein the first semiconductor structure is connected to the first signal transmission region in a direction perpendicular to the first base plate.

6. The semiconductor package of claim 1, wherein the second base plate further comprises a second interconnection surface located on an other surface of the base; the base has a channel that connects the first interconnection region and the second interconnection surface; and the first interconnection region is connected to the second signal transmission region by means of the channel in a direction perpendicular to the first base plate.

7. The semiconductor package of claim 1, wherein the base of the second base plate has an electromagnetic shielding layer.

8. The semiconductor package of claim 1, wherein the first base plate has a second surface facing away from the first surface; there is a circuit channel between the first surface and the second surface; the second surface of the first base plate has a plurality of first connection pads; and

wherein the first interconnection region of the second base plate has a plurality of second connection pads; and an area of a second connection pad is greater than or equal to an area of a first connection pad.

9. The semiconductor package of claim 8, wherein the second interconnection region of the second base plate has a plurality of third connection pads; and an area of a third connection pad is less than the area of the second connection pad.

10. The semiconductor package of claim 8, wherein the first signal transmission region of the first base plate has a plurality of fourth connection pads; and an area of a fourth connection pad is less than or equal to the area of the first connection pad.

11. The semiconductor package of claim 9, wherein a number of the third connection pads is greater than a number of the second connection pads.

12. The semiconductor package of claim 1, wherein in a direction perpendicular to the first base plate, the first base plate has a first thickness; in a direction perpendicular to the second base plate, the second base plate has a second thickness; and the first thickness is less than the second thickness.

13. The semiconductor package of claim 1, further comprising a second package, wherein the second package has a contact surface; and the second package is connected to the first interconnection region by means of the contact surface.

14. The semiconductor package of claim 13, wherein the contact surface of the second package has a first contact structure; the first contact structure has, in a direction perpendicular to the contact surface, a first height protruding from the contact surface; and the first height is greater than the preset height.

15. The semiconductor package of claim 14, wherein a first connection pad of the first base plate has a second contact structure protruding from the first base plate; the second contact structure has, in a direction perpendicular to the first base plate, a second height protruding from the first base plate; and the second height is less than or equal to the first height.

16. The semiconductor package of claim 13, wherein the second package comprises a second semiconductor structure; and a type of the second semiconductor structure is same as or different from a type of the first semiconductor structure.

17. The semiconductor package of claim 1, wherein an area of a distribution region of the first signal transmission region on the first base plate is less than an area of a distribution region of the third signal transmission region on the first base plate.