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REDUCED MASK PROCESS FOR MANUFACTURE
OF MOS GATED DEVICES

ABSTRACT OF THE DISCLOSURE

A process for forming a MOS gated device in which an oxide layer is patterned to have adjacent thick and thin oxide layers atop a silicon surface. Polysilicon is then patterned atop the oxide layer with a critical alignment step to the thin oxide layers in the process. Boron is implanted through both the thick and thin regions of the oxide which are exposed by the polysilicon mask to form P type base regions and P type guard rings in the silicon. Arsenic is thereafter implanted at an energy at which arsenic atoms penetrate only the thin oxide exposed by the polysilicon to form self-aligned source regions in the base regions previously formed. A contact opening mask which is critically aligned to the polysilicon mask forms openings for making contact to the silicon. The device is completed using non-critical alignment masking steps.

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