UV-BLOCKING LAYER FOR REDUCING UV-INDUCED CHARGING OF SONOS DUAL-BIT FLASH MEMORY DEVICES IN BEOL PROCESSING

TECHNICAL FIELD

The present invention relates to a process for preparation of a SONOS flash memory device including an ultraviolet (UV) radiation blocking layer for reducing UV-induced charging of device in back-end-of-line (BEOL) processing.

BACKGROUND ART

Non-volatile memory devices are currently in widespread use in electronic components that require the retention of information when electrical power is terminated. Non-volatile memory devices include read-only-memory (ROM), programmable-read-only memory (PROM), erasable-programmable-read-only memory (EPROM), and electrically-erasable-programmable-read-only-memory (EEPROM) devices. EEPROM devices differ from other non-volatile memory devices in that they can be electrically programmed and erased. Flash EEPROM devices are similar to EEPROM devices in that memory cells can be programmed and erased electrically. However, flash EEPROM devices enable the erasing of all memory cells in the device using a single electrical current pulse.

Product development efforts in EEPROM device technology have focused on increasing the programming speed, lowering programming and reading voltages, increasing data retention time, reducing cell erasure times and reducing cell dimensions. One important dielectric material for the fabrication of the EEPROM is an oxide-nitride-oxide (ONO) structure. One EEPROM device that utilizes the ONO structure is a silicon-oxide-nitride-oxide-silicon (SONOS) type cell. A second EEPROM device that utilizes the ONO structure is a floating gate FLASH memory device, in which the ONO structure is formed over the floating gate, typically a polysilicon floating gate.

In SONOS devices, during programming, electrical charge is transferred from the substrate to the silicon nitride layer in the ONO structure. Voltages are applied to the gate and drain creating vertical and lateral electric fields, which accelerate the electrons along the length of the channel. As the electrons move along the channel, some of them gain sufficient energy to jump over the potential barrier of the bottom silicon dioxide layer and become trapped in the silicon nitride layer. Electrons are trapped near the drain region because the electric fields are the strongest near the drain. Reversing the potentials applied to the source and drain will cause electrons to travel along the channel in the opposite direction and be injected into the silicon nitride layer near the source region. Because silicon nitride is not electrically conductive, the charge introduced into the silicon nitride layer tends to remain localized. Accordingly, depending upon the application of voltage potentials, electrical charge can be stored in discrete regions within a single continuous silicon nitride layer.

Non-volatile memory designers have taken advantage of the localized nature of electron storage within a silicon nitride layer and have designed memory circuits that utilize two regions of stored charge within an ONO layer. This type of non-volatile memory device is known as a dual-bit EEPROM, which is available under the trademark MIRRORBITJ from Advanced Micro Devices, Inc., Sunnyvale, California. The MIRRORBITJ dual-bit EEPROM is capable of storing twice as much information as a conventional EEPROM in a memory array of equal size. A left and right bit is stored in physically different areas of the silicon nitride layer, near left and right regions of each memory cell. Programming methods are then used that enable two bits to be programmed and read

simultaneously. The two bits of the memory cell can be individually erased by applying suitable erase voltages to the gate and to either the source or drain regions.

A key concept associated with the SONOS flash memory device is that for the device to operate properly, both bits must be able to be written and read separately. If one of the bits is programmed, a reverse read on the programmed bit must sense a high V_t, i.e., a "0", and a reverse read on the non-programmed bit must sense a low V_t, i.e., a "1". Thus, a reverse read on the non-programmed bit, which is equivalent to a forward read on the programmed bit, must punch through the region of trapped charge in order to generate a high enough read current. If this does not happen, the non-programmed bit will not be able to be read as a "1", i.e., a conductive bit.

One problem which has been encountered with SONOS flash memory devices including a dielectric charge storage layer is the buildup of charge in the charge storage layer, and subsequent increases in V_t, as a result of exposure to ultraviolet radiation during fabrication, and particularly in BEOL process steps, i.e., following formation of the flash memory cell. Processes which include high levels of UV radiation cause such charge buildup and concomitant increase in V_t. This increase in V_t would make all the bits appear to be high, i.e., "0". In addition, if the charge buildup is sufficiently large, it cannot be easily erased by the available voltages. As a result, the SONOS device would be rendered useless as a charge storage device.

UV exposure is not a problem for floating gate flash devices which have a polysilicon or other conductive material for a charge storage element. In such devices, the floating gate may be purposely exposed to UV radiation, in order to neutralize any electronic charge which builds up on the floating gate memory cell during processing. For example, U.S. Patent No. 6,350,651 uses UV radiation in this manner.

Such processing is not an option for SONOS flash memory devices, since the charge storage layer can be irreversibly damaged by exposure to UV radiation which builds up a large charge, and the charge cannot be neutralized by further exposure to UV radiation.

Therefore, a need exists for a method which will provide, and a device which includes provision for, protection of the charge storage layer in SONOS devices from exposure to UV radiation during BEOL processing. Accordingly, advances in such fabrication technology are needed to insure that charge buildup and increase in V_t in SONOS structures does not occur, particularly during BEOL processing.

DISCLOSURE OF INVENTION

The present invention, in one embodiment, relates to a SONOS flash memory device, including a SONOS flash memory cell; and at least one UV-protective layer, in which the UV-protective layer comprises a substantially UV-opaque material.

In one embodiment, the present invention relates to a SONOS flash memory device, including a SONOS flash memory cell; a UV-protective contact cap layer disposed over the SONOS flash memory cell, the UV-protective contact cap layer comprising a substantially UV-opaque material; and at least one additional UV-protective layer, the at least one additional UV-protective layer comprising at least a sub-layer of a UV-opaque material in which each UV-opaque material comprises one or more of silicon-rich silicon dioxide, silicon-rich silicon nitride, silicon-rich silicon carbide or silicon-rich SiCN, and in which the UV-protective layers protect the SONOS flash memory cell from damage resulting from UV exposure during BEOL processing in fabrication of the SONOS flash memory device.

In another embodiment, the present invention relates to a method of protecting a SONOS flash memory cell from UV-induced charging, including fabricating a SONOS flash memory cell in a semiconductor device; and depositing over the SONOS flash memory cell at least one UV-protective layer, wherein the UV-protective layer comprises a substantially UV-opaque material.

In one embodiment, the UV-protective layer protects the SONOS flash memory cell from damage resulting from UV exposure during BEOL processing in fabrication of the SONOS flash memory device.

Thus, the present invention, by providing a UV-protective layer, overcomes the problem of UV-induced charging of SONOS flash memory cells, particularly during BEOL processing. The present invention provides advantages such as (1) formation of a UV-protective layer which protects the device from BEOL UV radiation; (2) protection of the SONOS flash memory cell from UV-induced charging; (3) provision of a process modification which can be easily accommodated in presently employed fabrication processes; and (4) formation of one or more of a contact cap layer, interlevel dielectric layers, and a top oxide with this additional function in addition to standard dielectric functions. Thus, the present invention provides an advance in ONO fabrication technology, and insures proper charge isolation in ONO structures in SONOS flash memory devices, while at the same time providing distinct process and economic advantages. Although described in terms of, and particularly applicable to, SONOS flash memory devices, the present invention is broadly applicable to fabrication of any semiconductor device that includes a charge storage layer subject to unwanted UV charging.

BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 schematically illustrates, in cross-section, a portion of a semiconductor substrate containing a Dual-Bit EEPROM transistor which incorporates a substantially UV-opaque contact cap layer, and which further includes a further UV-protective layer having a substantially UV-opaque sub-layer, fabricated in accordance with an embodiment of the present invention.

Fig. 2 schematically illustrates, in cross-section, a portion of a semiconductor substrate containing a pair of Dual-Bit EEPROM transistors which incorporates a substantially UV-opaque sub-layer in a UV-protective layer, fabricated in accordance with an embodiment of the present invention.

Fig. 3 schematically illustrates, in cross-section, a portion of a semiconductor substrate which incorporates two UV-protective layers each of which includes a substantially UV-opaque sub-layer, fabricated in accordance with an embodiment of the present invention.

Figs. 4-5 illustrate, in cross-section, process steps for the fabrication of the UV-protective layers of the present invention on a semiconductor device, in a process in accordance with an embodiment of the present invention.

Fig. 6 schematically illustrates, in cross-section, a portion of a semiconductor substrate similar to that of Fig. 1, which incorporates a contact cap layer, three interlayer dielectric layers and a top oxide layer, fabricated in accordance with an embodiment of the present invention.

Fig. 7 is a schematic flow diagram showing the steps of an embodiment of the present invention.

It should be appreciated that for simplicity and clarity of illustration, elements shown in the Figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements are exaggerated relative to each other for clarity. Further, where considered appropriate, reference numerals have been repeated among the Figures to indicate corresponding elements.

Furthermore, it should be appreciated that the process steps and structures described below do not form a complete process flow for manufacturing integrated circuits. The present invention can be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as are necessary for an understanding of the present invention.

MODES FOR CARRYING OUT THE INVENTION

Referring first to Fig. 1, there is schematically shown in cross-section a transistor 10, which in one embodiment is a SONOS flash memory cell, suitable for use in a dual-bit EEPROM device, such as the MIRRORBITJ. The transistor 10 includes source/drain regions 12 and 14 located in a semiconductor substrate 16 and separated by a channel region 18. The substrate 16 may be, for example, a single crystal silicon wafer. The substrate 16 may also be gallium arsenide, a silicon-on-insulator layer, an epitaxial layer, a silicon-germanium layer, a germanium-on-insulator layer, or other known semiconductor substrate. A stack gate 24 overlies the channel region 18. The stack gate 24 includes a control gate electrode 26, and an ONO structure including a bottom or tunnel oxide layer 28, a charge storage layer 30 and a top oxide layer 32, as shown in Fig. 1. In one embodiment, the charge storage layer 30 is a nitride charge storage layer. In one embodiment, the charge storage layer 30 comprises silicon nitride. In other embodiments, the charge storage layer 30 comprises other known dielectric charge storage materials such as, for example, a high-K dielectric material. Suitable high-K dielectric charge storage materials are disclosed in copending, commonly assigned application assigned U.S. Serial No. 10/036,757, entitled USE OF HIGH-K DIELECTRIC MATERIALS IN MODIFIED ONO STRUCTURE FOR SEMICONDUCTOR DEVICES. The stack gate 24 further includes sidewall liners 34. As shown in Fig. 1, charges 36a and 36b may be stored in the charge storage layer 30, which acts as a charge or electron storage layer in the SONOS or Dual-Bit EEPROM device.

Referring still to Fig. 1, the stack gate 24 is covered and surrounded by a first interlevel dielectric (ILD) layer 20, which also may be referred to as IDL0 ("ILD zero") layer 20. In one embodiment, the ILD0 layer 20 is silicon dioxide. In other embodiments, the ILD0 layer 20 may comprise other materials, such as boron phosphosilicate glass (BPSG) or other known materials for such layer. In the embodiment shown in Fig. 1, the ILD0 layer 20 is thicker than the height of the stack gate 24.

In the operation of the exemplary Dual-Bit EEPROM transistor 10, voltages are applied to the gate electrode 24 and as appropriate to the source/drain regions 12 and 14. The applied voltages cause electrical charge from the source/drain regions 12 and 14 to propagate across the channel region 18. During programming, once the charge encounters a sufficiently strong vertical field, the charge either is injected or tunnels from the channel region 18 through the bottom oxide layer 28 into the silicon nitride charge storage layer 30. The charge storage layer may also be referred to as an electron storage layer. For example, depending upon the particular voltage levels applied to the control-gate electrode 26 and to the source/drain regions 12 and 14, the electrical charges 36a, 36b are transferred into the charge storage layer 30 and are localized to regions in proximity to either the source/drain region 12, or the source/drain region 14.

Those skilled in the art will recognize that for proper functioning of a dual-bit EEPROM device, the electrical charges 36a, 36b should remain isolated in the regions of the charge storage layer 30 to which they are initially introduced and, no charge should be present prior to programming of the charge storage layer 30. The proper maintenance of the condition, either programmed or not programmed, of the charge storage layer 30 is needed for the proper performance of a dual-bit EEPROM device. In particular, the charge storage layer 30 should be protected from incident UV radiation which can create a charge in the charge storage layer 30. As described above, such spuriously created charges can introduce errors into stored data and even damage the charge storage layer 30.

In accordance with the invention, unwanted charge buildup in the charge storage layer 30 from incident UV radiation is minimized by forming a UV-protective layer as described herein. The protection from spurious charges in and the improved performance of Dual-Bit EEPROM devices obtained by the present invention can be better understood following a description of a fabrication process for the structures described above in accordance with the invention.

In the embodiment shown in Fig. 1, the first ILD layer 20 is covered by a contact cap layer 38. The contact cap layer 38 may also be referred to as a "C1" layer. In one embodiment, the contact cap layer 38 comprises a silicon-rich material which absorbs UV radiation. In one embodiment, the contact cap layer 38 comprises a substantially UV-opaque material such as a silicon-rich nitride, silicon-rich oxide, silicon-rich carbide or silicon-rich carbide-nitride. In one embodiment, the contact cap layer 38 comprises one or more of silicon-rich silicon dioxide, silicon-rich silicon nitride, silicon-rich silicon carbide or silicon-rich silicon carbide-nitride. The contact cap layer 38 may be deposited by a variety of process techniques, e.g., CVD, LPCVD, APCVD, etc. In one illustrative embodiment, the contact cap layer 38 is comprised of a layer of silicon-rich silicon nitride that is formed by a CVD process. In one embodiment, the substantially UV-opaque contact cap layer 38 provides protection to the transistor 10 from UV radiation which may impinge upon the transistor 10 during processing subsequent to the formation of the stack gate 24 of the transistor 10. In one embodiment, the contact cap layer 38 is sufficiently UV opaque to block at least about 95% of incident UV radiation. In another embodiment, the contact cap layer 38 is sufficiently UV opaque to block at least about 98% of incident UV radiation. And in another embodiment, the contact cap layer 38 is sufficiently UV opaque to block at least about 99% of incident UV radiation. The silicon-rich materials of which the contact cap layer 38 is comprised are described in more detail below.

In one embodiment (not shown), the contact cap layer 38 comprises a first, substantially UV opaque sub-layer, and a second sub-layer which comprises a material which is not UV opaque. The embodiment of the contact cap layer 38 having the first, substantially UV opaque sub-layer and the second sub-layer is substantially similar to the layers described below with respect to the UV-protective layer 46, except that the total thickness of the layers may be less. In one embodiment, the first, substantially UV opaque sub-layer of the contact cap layer 38 may be substantially thicker than the second sub-layer. In one embodiment, due to the relatively small total thickness of the contact cap layer 38, a second sub-layer is not present. In one embodiment, the contact cap layer 38 comprises only a single, substantially UV-opaque layer.

Referring still to Fig. 1, the transistor 10 further includes conductive connecting plugs 40, which may be, for example, tungsten plugs. The conductive plugs 40 are formed in apertures 42 in the ILD0 layer 20. The apertures 42 penetrate through the ILD0 layer 20, providing a path or via to the source 12 and/or drain 14 of the transistor 10. The transistor 10 further comprises metal electrodes 44. The metal electrodes 44 may be, for example, connecting elements (e.g., bit lines, etc.) of the transistor 10 to power sources and adjacent transistors. The conductive plugs 40 in Fig. 1 provide electrical connection between the metal electrodes 44 and the source 12 and/or drain 14. In one embodiment, as shown in Fig. 2, the conductive plugs 40 provide electrical connection both to the source 12 of one transistor 10, and to the drain 14 of an adjacent transistor.

In the embodiment shown in Fig. 1, the transistor 10 is covered by a UV-protective layer 46. In one embodiment, the UV-protective layer 46 is a second interlevel dielectric layer, designated ILD1. The UV-protective layer 46 includes a first, substantially UV opaque liner or sub-layer 46a and a second sub-layer 46b. In one embodiment, the second sub-layer 46b is substantially thicker than the first sub-layer 46a, thus the first sub-layer 46a may also be referred to as a liner. In one embodiment, the first, substantially UV opaque sub-layer 46a provides protection to the transistor 10 from UV radiation which may impinge upon the transistor 10 during processing subsequent to the formation of the stack gate 24 of the transistor 10. In one embodiment, the first sub-layer 46a is sufficiently UV opaque to block at least about 95% of incident UV radiation. In another embodiment, the first sub-layer 46a is sufficiently UV opaque to block at least about 98% of incident UV radiation. And in another embodiment, the first sub-layer 46a is sufficiently UV opaque to block at least about 99% of incident UV radiation.

As used herein, the term "substantially UV opaque" means that the layer so described blocks at least about 90% of the incident UV light. As used herein, the term "substantially not UV opaque" means that the layer so described passes a major amount of the incident UV radiation without absorption thereof. As used herein, the term "substantially UV transparent" means that the layer so described passes at least about 75% of the incident UV radiation without absorption thereof. Such terms do not mean that the material has no effect on the UV radiation, such as shifts in phase, wavelength or other properties.

The first sub-layer 46a comprises a silicon-rich material which absorbs UV radiation. In one embodiment, the silicon-rich material is substantially UV-opaque as defined herein. In one embodiment, the first sub-layer 46a comprises one or more of silicon-rich silicon dioxide, silicon-rich silicon nitride, silicon-rich silicon carbide, or silicon-rich SiCN.

In one embodiment, the first sub-layer 46a comprises silicon-rich silicon dioxide. As is known in the art, pure or stoichiometric silicon dioxide is substantially transparent to UV radiation, including UV radiation in the range from near-UV radiation having a wavelength of about 400 nm, to UV radiation having a wavelength of about 200 nm. However, increasing the silicon content of silicon dioxide above a stoichiometric ratio increases the refractive index and the UV absorbency of the material. Thus, a silicon-rich silicon dioxide provides enhanced UV blocking capability. As the silicon content is increased, the UV blocking or opacity increases. Thus, in one embodiment, the first sub-layer 46a comprises silicon-rich silicon dioxide, in which the amount of silicon is sufficient to render the first sub-layer 46a substantially UV opaque. In one embodiment, the silicon-rich silicon dioxide has a formula SiO_x, wherein $x < 2$. In one embodiment, the silicon-rich silicon dioxide has a formula SiO_x, wherein $1.8 \leq x \leq 1.99$. In one embodiment, the silicon-rich silicon dioxide has a formula SiO_x, wherein $1.88 \leq x \leq 1.95$.

In general, the silicon-rich forms of the materials used in the UV-protective layers, including the contact cap layer 38, have a higher refractive index that the corresponding non-silicon-rich forms of the same materials. In general, enrichment of the silicon content of these materials correlates both with increased refractive index and with increased UV opacity in these materials.

As is well known, the refractive index of substantially stoichiometric silicon dioxide is about 1.46. As mentioned above, the refractive index of silicon-rich silicon dioxide is higher than that of silicon dioxide. In one embodiment, the first sub-layer 46a has a refractive index in the range from about 1.5 to about 1.8. In another embodiment, the refractive index of the first sub-layer 46a is about 1.55 to about 1.75. In another embodiment, the refractive index of the first sub-layer 46a is about 1.6 to about 1.7, and in one embodiment, the refractive index of the first sub-layer 46a is greater than about 1.6.

Here, and throughout the specification and claims, the limits of the ranges and ratios may be combined. Thus, for example, in the foregoing ranges of refractive index, although the range from about 1.6 to about 1.8 is not specifically recited, such range is within the scope of the disclosure.

In one embodiment, the first sub-layer 46a comprises silicon-rich silicon nitride. Silicon nitride, in its non-silicon-rich, stoichiometric form is generally assigned the empirical formula Si_3N_4. Silicon-rich silicon nitride comprises a Si-enriched form of silicon nitride. Thus, if the formula for silicon-rich silicon nitride is written as Si_xN_4, the value of x is greater than 3. In one embodiment, $3.01 \leq x \leq 4$. In one embodiment, the value of x ranges from greater than 3, i.e., from about 3.01 to about 4. In one embodiment, the value of x ranges from about 3.1 to about 3.8, and in another, from about 3.15 to about 3.6.

In one embodiment, the first sub-layer 46a comprises silicon-rich silicon carbide, SiC. Silicon carbide is generally assigned the empirical, stoichiometric formula SiC. Silicon-rich SiC comprises a Si-enriched SiC relative to stoichiometric SiC. Thus, if silicon carbide is represented as Si_aC_b, in silicon-rich SiC, $a > b$, and $a + b = 2$, whereas in stoichiometric SiC, a is substantially equal to b, i.e., $a \approx b$, and $a + b = 2$. In one embodiment, in silicon-rich SiC, a ranges from 1.01 to about 1.2, and $a + b = 2$. In one embodiment, in silicon-rich SiC, a ranges from 1.02 to about 1.1, and $a + b = 2$. Thus, in non-silicon-rich SiC, a ranges from greater than 0.99 to less than 1.01 and $b = 2 - a$.

In one embodiment, the first sub-layer 46a comprises silicon-rich SiCN. SiCN has been referred to under various names, such as silicon carbon nitride, silicon carbonitride and silicon cyanide. The empirical formula of SiCN varies depending on the formation conditions, but is generally considered to be analogous to Si_3N_4 and C_3N_4, in which the Si and C components are interchanged. The formula of the "interchanged" Si and C has been sometimes referred to as $(Si;C)_3N_4$. Herein, this material will be referred to simply as SiCN. Silicon-rich SiCN contains a major proportion of Si and a minor proportion of C, and non-silicon-rich SiCN contains a minor proportion of SI and a major proportion of C. Thus, SiCN may be considered to have a general formula $Si_xC_yN_4$. Using this formula, in silicon-rich SiCN, $x > 1.5$ and $y < 1.5$, and non-silicon-rich SiCN, $x \leq 1.5$ and $y \geq 1.5$. In one embodiment, in silicon-rich SiCN, x ranges from greater than 1.5 to about 2.5, and y ranges from about 0.5 to less than 1.5. In one embodiment, in silicon-rich SiCN, x ranges from about 1.55 to about 2.25, and y ranges from about 0.75 to about 1.45.

In one embodiment, silicon-rich SiCN comprises a super-stoichiometric quantity of Si, relative to the C and N. The SiCN with the super-stoichiometric quantity of Si has a total amount of Si and C which exceeds the quantity of Si and C needed to be stoichiometrically equivalent to the quantity of N. The increase is obtained by providing Si enrichment of the SiCN. In this embodiment, for example, if $y = 1.5$, $x > 1.5$. Thus, based on the amount of C and N in the SiCN, the content of Si is enriched. In other words, once the content of C relative to N is determined, rather than the stoichiometric quantity of Si being included, in this embodiment, in silicon-rich SiCN, the content of Si is higher than the stoichiometric quantity needed, thus it has a super-stoichiometric Si content.

In one embodiment, the silicon-rich material in the first sub-layer 46a absorbs UV radiation in the UV range from about 450 nm to about 190 nm. In one embodiment, the silicon-rich material in the first sub-layer 46a absorbs UV radiation in the UV range from about 400 nm to about 200 nm. In one embodiment, the silicon-rich material in the first sub-layer 46a absorbs UV radiation in the UV range from about 390 nm to about 210 nm.

In one embodiment, UV absorption or percent transmittance (%T) is measured in a Hewlett-Packard UV spectrophotometer at a wavelength of 254 nm. Measurement of UV radiation at this wavelength provides a good estimate of the absorption of UV radiation generally.

In one embodiment, the second sub-layer 46b comprises a non-silicon-rich form of the material of the first sub-layer. Thus, for example, in an embodiment in which the first sub-layer 46a comprises silicon-rich silicon dioxide, the second sub-layer 46b comprises non-silicon-rich, or substantially stoichiometric, silicon dioxide. Similarly, in an embodiment in which the first sub-layer 46a comprises silicon-rich silicon nitride, the second sub-layer 46b comprises non-silicon-rich, or substantially stoichiometric, silicon nitride. Likewise, in an embodiment in which the first sub-layer 46a comprises silicon-rich silicon carbide, the second sub-layer 46b comprises non-silicon-rich, or substantially stoichiometric, silicon carbide. And similarly, in an embodiment in which the first sub-layer 46a comprises silicon-rich SiCN, the second sub-layer 46b comprises non-silicon-rich, or substantially stoichiometric, SiCN.

In one embodiment, the second sub-layer 46b is not UV-opaque. In one embodiment, the second sub-layer 46b is substantially UV transparent, down to a wavelength of about 200 nm. In one embodiment, the second sub-layer 46b absorbs at least some high energy UV radiation, that is, UV radiation having a wavelength in the range from about 254 nanometers (nm) down to about 200 nm, or to about 190 nm.

In one embodiment, the second sub-layer 46b is silicon dioxide. In one embodiment, the second sub-layer 46b is silicon dioxide having a general formula SiO_x, wherein $x \leq 2$. In one embodiment, the second sub-layer 46b is silicon dioxide having a general formula SiO_2, i.e., a substantially stoichiometric silicon dioxide. In another embodiment, the second sub-layer 46b is non-silicon-rich silicon nitride, Si_3N_4, i.e., a substantially stoichiometric silicon nitride. In another embodiment, the second sub-layer 46b is non-silicon-rich silicon carbide, SiC, as defined above. In another embodiment, the second sub-layer 46a is non-silicon-rich SiCN, as defined above.

Fig. 2 shows a second schematic view of a pair of adjacent transistors 10a and 10b. As in the embodiment shown in Fig. 1, the embodiment shown in Fig. 2 includes a semiconductor substrate 16, upon which have been formed two adjacent transistors 10a and 10b. Each transistor 10a, 10b includes, a source 12, a drain 14 and a channel region 18. Formed above the channel region 18 of each respective transistor 10a, 10b is a stack gate 24a, 24b, such as that described in more detail with respect to the transistor 10 of Fig. 1. As in Fig. 1, each transistor 10a, 10b in Fig. 2 includes a first interlevel dielectric layer 20, designated ILD0 layer 20, which covers and surrounds

each of the stack gates 24a, 24b. As in Fig. 1, the ILD0 layer 20 is covered by a contact cap layer 38. In one embodiment, the contact cap layer 38 is a UV-blocking layer.

Fig. 2 illustrates a first conductive plug 40a, a metal conductor 44 and a second conductive plug 40b. In the embodiment of Fig. 2, the conductive plug 40a provides an electrical connection between the metal conductor 44 and adjacent drain 14 and source 12 of two adjacent transistors 10a, 10b. Fig. 2 illustrates a second conductive plug 40b, which provides an electrical connection from an external source (not shown) to the metal conductor 44.

As shown in Fig. 2, the contact cap layer 38 is covered by a UV-protective layer 46. In one embodiment, the UV-protective layer 46 shown in Fig. 2 is a second interlevel dielectric layer, designated ILD1. The UV-protective layer 46 comprises a first substantially UV-opaque sub-layer 46a, and a second sub-layer 46b. In one embodiment, as described above with respect to Fig. 1, the second sub-layer 46b is substantially UV transparent, and in one embodiment, the second sub-layer 46b is substantially not UV opaque. The description provided above with respect to the UV-protective layer 46 embodiment shown in Fig. 1 is fully applicable in all respects to the embodiment of Fig. 2, so is not repeated here.

Fig. 3 schematically illustrates another embodiment of the present invention. Fig. 3 shows a portion of a semiconductor device 50, which may include, for example, a transistor such as those described with respect to Figs. 1 and 2. The structure shown in Fig. 3 depicts layers applied during BEOL processing. The device 50 includes a first interlevel dielectric layer 20 (ILD0 layer 20), which may be disposed in a layer covering a stack gate (not shown) or other structure of a semiconductor device. The ILD0 layer 20 of Fig. 3 is substantially the same as that described above with respect to the embodiments shown in Figs. 1 and 2. The device 50 further includes a contact cap layer 38, which is substantially the same as that described above with respect to the embodiments shown in Figs. 1 and 2. The device 50 shown in Fig. 3 includes a first conductive plug 40a and a second conductive plug 40b. The device 50 shown in Fig. 3 also includes a first conductive metal 44a and a second conductive metal 44b. The first conductive plug 40a provides electrical connection between the first conductive metal 44a and the second conductive metal 44b. The second conductive plug 40b provides electrical connection between the second conductive metal 44b and an external power source or other device (not shown).

The semiconductor device 50 shown in Fig. 3 includes two UV-protective layers. The device 50 includes a first UV-protective ILD layer 46, and a second UV-protective layer 48. In one embodiment, both the first UV-protective ILD layer 46 and the second UV-protective layer 48 are substantially the same as the UV-protective layer 46 described above with respect to Figs. 1 and 2, with respect to materials, thicknesses, functions, etc.

In one embodiment, the first UV-protective ILD layer 46 shown in Fig. 3 is a second interlevel dielectric layer, designated ILD1. The first UV-protective ILD layer 46 shown in Fig. 3 includes a first substantially UV-opaque sub-layer 46a, and a second sub-layer 46b. In one embodiment, the second sub-layer 46b is substantially UV transparent, and in another embodiment, the second sub-layer 46b is substantially not UV opaque.

In one embodiment, the second UV-protective layer 48 shown in Fig. 3 is a third interlevel dielectric layer, designated ILD2. The second UV-protective layer 48 shown in Fig. 3 includes a second substantially UV-opaque sub-layer 48a, and a second sub-layer 48b. In one embodiment, the second sub-layer 48b is substantially UV transparent, and in another embodiment, the second sub-layer 48b is substantially not UV opaque.

The thickness of the UV-protective layer is, of course, the sum of the thicknesses of the respective sub-layers from which it is formed. In one embodiment, the first sub-layer has a thickness in the range from about 300 angstroms to about 1000 angstroms, and the UV-protective layer has a total thickness of about 4000 angstroms to about 10,000 angstroms. In another embodiment, the first sub-layer has a thickness in the range from about 400 angstroms to about 800 angstroms, and the UV-protective layer has a total thickness of about 5000 angstroms to about 8000 angstroms. In another embodiment, the first sub-layer has a thickness in the range from about 500 angstroms to about 700 angstroms, and the UV-protective layer has a total thickness of about 6000 angstroms to about 7000 angstroms. In another embodiment, the thickness of the first sub-layer 46a is sufficient to absorb incident UV radiation resulting from BEOL processes, including, for example, PECVD, which may be used in depositing subsequent materials on the semiconductor device. In an embodiment in which the UV-protective layer constitutes a single layer, such as in the contact cap layer 38, or in a top oxide layer, the thickness of the UV-protective layer has a thickness in the range from about 300 angstroms to about 1000 angstroms.

Although the foregoing embodiments of the present invention have been described in detail, as would be understood by persons of ordinary skill in the art, further embodiments of the present invention may include additional UV-protective layers. In some such embodiments, the UV-protective layer may constitute a further interlevel dielectric layer, or ILD, for example an ILD3 layer. In the case of the ILD0 layer, the sub-layer which is substantially UV-opaque is the contact cap layer 38, which in effect is the top or upper layer, rather than the bottom or lower layer, as in the embodiments of the ILD1 and ILD2 layers shown in Figs. 1-3. In other embodiments, the UV protective layer is a layer other than an interlevel dielectric layer. For example, the UV protective layer may be a top oxide layer. The top oxide layer covers the entire semiconductor device. In one embodiment, both the contact cap layer 38 and a top oxide layer comprise a UV protective layer as described above. In one embodiment, these layers include a UV opaque first sub-layer and a non-UV opaque second sub-layer, as each sub-layer has been described above. In another embodiment, the contact cap layer, and in yet another embodiment, the top oxide layer, respectively comprise a single, UV opaque layer, as opposed to a UV-protective comprising two sub-layers.

Although not shown, the embodiments shown in Figs. 1-3 may include additional UV-protective layers such as described herein. For example, these embodiments may comprise a UV-protective ILD2 layer, a UV-protective ILD3 layer, and/or a UV-protective top oxide layer, in addition to the UV-protective contact cap layer 38 and/or the UV-protective ILD1 layer 46. Similarly, in one embodiment, the ILD1 layer 46 is not a UV-protective layer, but a subsequent layer, such as an ILD2, ILD3 or top oxide layer, is a UV-protective layer. Fig. 6 shows an embodiment including additional layers, some or all of which may comprise UV-protective layers and/or substantially UV-opaque layers.

Processes for Fabrication of the Device

The following description of the process of the present invention is described in the context of a UV-protective layer suitable for use in a Dual-Bit EEPROM device, such as the MIRRORBITJ device. It is to be understood that, while the present invention is discussed herein in that context, that this is merely exemplary and is not intended to limit the scope of the present invention. The UV-protective layer fabricated by the presently disclosed method is applicable to any semiconductor device in which a flash memory cell is included and which may be susceptible to UV-induced charging or other damage.

The following description of the present invention follows with reference to Figs. 4-6. Figs. 4-5 illustrate, in cross-section, embodiments of the semiconductor device after certain process steps in the fabrication of a UV protective layer in accordance with an embodiment of the invention. Fig. 7 is a schematic flow diagram showing the steps of an embodiment of a process in accordance with the present invention.

In the first step of a process in accordance with the present invention, shown schematically in Fig. 7 as step 701, a semiconductor substrate with a SONOS flash memory cell fabricated thereon is provided, as shown in Fig. 4. The SONOS flash memory cell may be fabricated by any appropriate method known in the art. Since the fabrication of such semiconductor devices is well known, for the sake of brevity such is not disclosed in detail herein. An example of such a device 10 is shown in Fig. 4. The component parts of the device 10 shown in Fig. 4 are substantially the same as described above with respect to Fig. 1, and include the source/drain regions 12 and 14 located in the semiconductor substrate 16 and separated by the channel region 18. A stack gate 24 overlies the channel region 18. The device 10 shown in Fig. 4 further includes the first interlevel dielectric layer 20, the contact cap layer 38, the conductive plugs 40, and the metal conductors 44.

In the second step of the process in accordance with the present invention, shown schematically in Fig. 7 as step 702, a first layer or sub-layer of the UV-protective layer is deposited over the SONOS flash memory cell. In one embodiment, the first layer or sub-layer is substantially UV opaque, as defined above. In one embodiment, the first layer or sub-layer is the contact cap layer 38. In one embodiment, the first layer or sub-layer is the sub-layer 46a. In one embodiment, the contact cap layer 38 is the first layer deposited and this is followed by deposition of the first sub-layer 46a, both of which comprise substantially UV-opaque materials.

In one embodiment, the first sub-layer comprises silicon-rich silicon dioxide. As described above, silicon-rich silicon dioxide has a formula SiO_x, in which $x < 2$. (Alternatively, the formula could be expressed as Si_yO_2, in which $y > 1$.) As described above, in other embodiments, $1.8 \leq x \leq 1.99$, and another embodiment, $1.88 \leq x \leq 1.95$.

The contact cap layer 38 and/or the first sub-layer 46a, comprising a silicon-rich material which absorbs UV radiation, is typically blanket-deposited over the entire wafer. In one embodiment, the method for depositing the first sub-layer is a method which does not use or generate UV radiation. In another embodiment, the method is one which would not expose the SONOS memory cell to UV radiation.

In an embodiment in which the contact cap layer 38 and/or the first sub-layer 46a comprises silicon-rich silicon dioxide, silicon-rich silicon nitride, or silicon-rich silicon carbide, various methods are commonly known in the art for forming and depositing such materials, and are not discussed in detail herein.

In an embodiment in which the contact cap layer 38 and/or the first sub-layer 46a comprises silicon-rich SiCN, and in which the second-sublayer 46b comprises non-silicon-rich SiCN, various methods are known for forming and depositing such materials. Due to the variable stoichiometry which can be obtained in SiCN, the formation of silicon-rich, or non-silicon-rich, SiCN is obtained by changing the amount of silicon-containing feed to the process.

In general, in the silicon-rich materials, the higher the refractive index, the higher the UV absorption capability of the material. Increasing the refractive index generally results in an increase in UV opacity of the material.

For example, in an embodiment in which the first sub-layer 46a is silicon-rich silicon dioxide, the silicon-rich silicon dioxide may be differentiated from pure or stoichiometric silicon dioxide on the basis of its refractive index. For stoichiometric silicon dioxide, the refractive index is about 1.46 to 1.5. In order to obtain sufficient UV-protection, that is, for the first sub-layer to be substantially UV opaque, the refractive index needs to be greater than 1.5, in one embodiment, the refractive index is greater than about 1.6 and, as noted above, in other embodiments the refractive index may be substantially higher than 1.6. The increase in refractive index of the silicon dioxide is achieved by incorporating more silicon in the silicon dioxide, i.e., by forming silicon-rich silicon dioxide as described above. The determination of whether sufficient silicon is present is easily made by measurement of the refractive index of the layer during processing.

Similar considerations apply to silicon-rich silicon nitride, silicon-rich SiCN and silicon-rich silicon carbide.

As shown in Fig. 7 as step 703, the third step in the present invention comprises deposition of a second sub-layer 46b of the UV-protective layer 46. When a sufficient, selected thickness of the first sub-layer 46a has been deposited, the second sub-layer 46b is deposited thereover.

As shown in Fig. 7, some embodiments bypass the step 703, proceeding directly to the step 704 and thence optionally returning to step 702 to deposit another layer of substantially UV-opaque material. The bypass of step 703 is schematically illustrated in Fig. 7 by the alternate path (a). Return from step 704 to step 702 is schematically illustrated in Fig. 7 by the alternate path (b).

In one embodiment, as noted above, the material of the second sub-layer comprises a non-silicon-rich form of the material of the first sub-layer. In one such embodiment, the transition from deposition of a silicon-rich to deposition of a non-silicon-rich layer is accomplished simply by changing the deposition conditions. In one embodiment, the transition is accomplished by changing the post-deposition heat treatment conditions, as described above with respect to SiCN.

For example, in one embodiment in which the silicon-rich material is silicon-rich silicon dioxide, the transition from depositing the first sub-layer to depositing the second sub-layer is accomplished simply by changing the quantity of silicon-containing precursor provided to the deposition apparatus from a first quantity which results in deposition of a silicon-rich silicon dioxide, to a second quantity, which results in deposition of a substantially stoichiometric silicon dioxide. In one embodiment, both steps are carried out in the same apparatus, on a substantially continuous basis. In one embodiment, any discontinuity results from any delay or pause in deposition resulting from the change in quantity of silicon-containing precursor being provided to the deposition apparatus. Thus, in one embodiment, the steps 702 and 703 are part of a substantially continuous deposition step, which may be regarded as a combination of steps 702 and 703. This embodiment is illustrated schematically in Fig. 7 by the alternate pathway (b), leading from step 704 back to step 702.

Other methods of depositing the non-silicon-rich material can be suitably selected by those of skill in the art.

An exemplary structure resulting from step 703, deposition of the second sub-layer 46b, on the first sub-layer 46a shown in Fig. 5 is the structure shown in Fig. 1.

In one embodiment, a second UV-protective ILD layer 48 is deposited over the first UV-protective ILD layer 46, as is shown, for example in Fig. 3. In this embodiment, the steps 702 and 703 are repeated. In one embodiment, one layer, in another embodiment two or more layers, and in yet another embodiment, no layers of another material are formed between the first UV-protective ILD layer and the second UV-protective ILD layer. In one embodiment, the additional layer(s) include metal conductive layers, similar to the layers 44a, 44b shown in Fig. 3. Thus, while in one embodiment, a full layer is formed, the layer intervening the first UV-protective ILD layer and the second UV-protective ILD layer may be etched or otherwise partially removed in forming, e.g., a conductive pattern or other "wiring". Then, the second UV-protective ILD layer may be deposited to provide insulation and protection to the intervening layer or material. In one embodiment, the second UV-protective layer replaces a conventional interlayer dielectric layer, such as an ILD2 layer, a contact cap layer or a top oxide layer, as described above.

In another embodiment, shown in Fig. 6, a third UV-protective layer 52 is deposited over the second UV-protective ILD layer 48. Fig. 6 schematically illustrates, in cross-section, a portion of a semiconductor substrate similar to that of Fig. 1, which incorporates a contact cap layer 38, three interlayer dielectric layers 20, 46 and 48 (of which either or both of layers 46 and 48 may be UV-protective layers), and a UV-protective top oxide layer 52, fabricated in accordance with an embodiment of the present invention. The third UV-protective layer, or top oxide layer 52 would be substantially similar to the first and second UV-protective layers, comprising, in one embodiment, a first, substantially UV opaque sub-layer and a second sub-layer, which comprises a non-UV-opaque material, and in another embodiment, comprises a single, substantially UV-opaque layer.

In one embodiment, the third UV-protective layer replaces a conventional interlayer dielectric layer, such as an ILD3 layer.

These embodiments are illustrated in Fig. 7 as step 704, and by the alternate pathway (b), which leads from step 704 back to step 702. According to step 704, step 702 and step 703, or step 702 only, may be repeated as needed to deposit additional UV-protective layers, or substantially UV-opaque layers via alternate pathways (a) and/or (b). As also indicated in Fig. 7, step 704 includes an optional return to step 702, or the process may proceed to the final step shown in Fig. 7, which is to continue fabrication of the semiconductor device.

As indicated in the final step of Fig. 7, following formation of the UV-protective layer or layers in accordance with the present invention, the semiconductor device and the SONOS flash memory cell are further processed in BEOL processes, to complete the fabrication of the device, as appropriate. As a result of the present invention, in one embodiment, it is not necessary to protect the device and the SONOS flash memory cell from exposure to UV radiation. In other embodiments, it may be desirable to protect the device and the SONOS flash memory cell from such exposure, since it may not be possible to fully protect the device from all harmful effects of UV radiation by means of the present invention.

In one embodiment, the semiconductor device and the SONOS flash memory cell are protected from exposure to UV radiation during the processing steps subsequent to formation of the stack gate. In another embodiment, the semiconductor device and the SONOS flash memory cell are protected from exposure to UV radiation during the processing steps subsequent to formation of the ONO portions of the stack gate. In one embodiment, the semiconductor device and the SONOS flash memory cell are protected from exposure to UV radiation during the processing steps subsequent to formation of the charge storage layer. In one embodiment, the protection from UV

radiation at and beyond these points in the fabrication process comprises the herein described formation of one or more UV protective layers. In another embodiment, the protection from UV radiation further comprises shielding or otherwise avoiding exposure to UV radiation. In another embodiment, the protection from UV radiation further comprises selection and use of non-UV processes, as described above.

INDUSTRIAL APPLICABILITY

The present invention, the present invention, by providing a UV-protective layer, overcomes the problem of UV-induced charging of SONOS flash memory cells, particularly during BEOL processing. The present invention provides advantages such as (1) formation of a UV-protective layer which protects the device from BEOL UV radiation; (2) protection of the SONOS flash memory cell from UV-induced charging; (3) provision of a process modification which can be easily accommodated in presently employed fabrication processes; and (4) formation of one or more of a contact cap layer, interlevel dielectric layers, and a top oxide with this additional function in addition to standard dielectric functions. Thus, the present invention provides an advance in ONO fabrication technology, and insures proper charge isolation in ONO structures in SONOS flash memory devices, while at the same time providing distinct process and economic advantages. Although described in terms of, and particularly applicable to, SONOS flash memory devices, the present invention is broadly applicable to fabrication of any semiconductor device that includes a charge storage layer subject to unwanted UV charging.

Although the invention has been described and illustrated with reference to specific illustrative embodiments thereof, it is not intended that the invention be limited to those illustrative embodiments. Those skilled in the art will recognize that variations and modifications can be made without departing from the spirit of the invention. For example, the thicknesses of the individual layers making up the ONO structure can be varied from that described herein. It is therefore intended to include within the invention all such variations and modifications that fall within the scope of the appended claims and equivalents thereof.

Claims

What is claimed is:

1. A SONOS flash memory device (10,50), comprising:
a SONOS flash memory cell (24); and
at least one UV-protective layer (38, 46, 48 and/or 52), wherein the UV-protective layer comprises a substantially UV-opaque material.

2. The device of claim 1, wherein the UV-protective layer is a contact cap layer (38) disposed over the SONOS flash memory cell.

3. The device of claim 1, wherein the UV-protective layer (38, 46, 48 and/or 52) protects the SONOS flash memory cell from damage resulting from UV exposure during BEOL processing in fabrication of the SONOS flash memory device.

4. The device of claim 1, wherein the UV-opaque material comprises one or more of silicon-rich silicon dioxide, silicon-rich silicon nitride, silicon-rich silicon carbide or silicon-rich SiCN.

5. The device of claim 1, further comprising at least one additional UV-protective layer, the at least one additional UV-protective layer comprising at least a sub-layer of a UV-opaque material.

6. The device of claim 5, wherein the at least one additional UV-protective layer is a component of one or more of an interlayer dielectric layer 1 (46), interlayer dielectric layer 2 (48), or a top oxide layer (52).

7. The device of claim 1, wherein the UV-opaque material comprises a refractive index greater than about 1.5.

8. A method of protecting a SONOS flash memory cell from UV-induced charging, comprising:
fabricating a SONOS flash memory cell in a semiconductor device; and
depositing over the SONOS flash memory cell at least one UV-protective layer, wherein the UV-protective layer comprises a substantially UV-opaque material.

9. The method of claim 8, wherein the UV-opaque material comprises one or more of silicon-rich silicon dioxide, silicon-rich silicon nitride, silicon-rich silicon carbide or silicon-rich SiCN and/or comprises a refractive index greater than about 1.5.

10. The method of claim 8, further comprising depositing at least one additional UV-protective layer, the at least one UV-protective layer comprising at least a sub-layer of a UV-opaque material.