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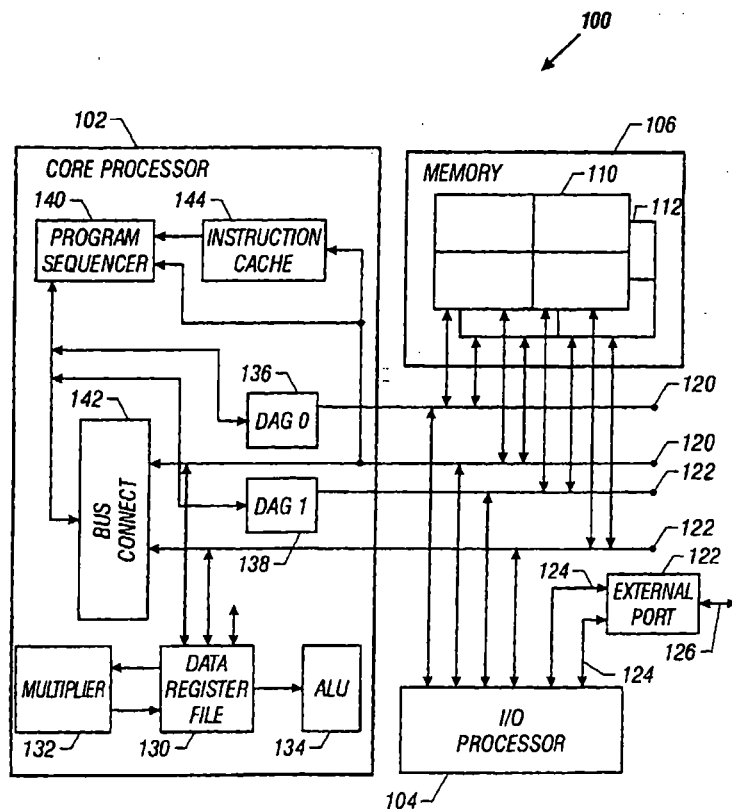
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(54) Title: **MULTI-TIERED MEMORY BANK HAVING DIFFERENT DATA BUFFER SIZES WITH A PROGRAMMABLE BANK SELECT**

(57) Abstract: An apparatus having a core processor and a plurality of cache memory banks is disclosed. The cache memory banks are connected to the core processor in such a way as to provide substantially simultaneous data accesses for said core processor

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