FIG. 1

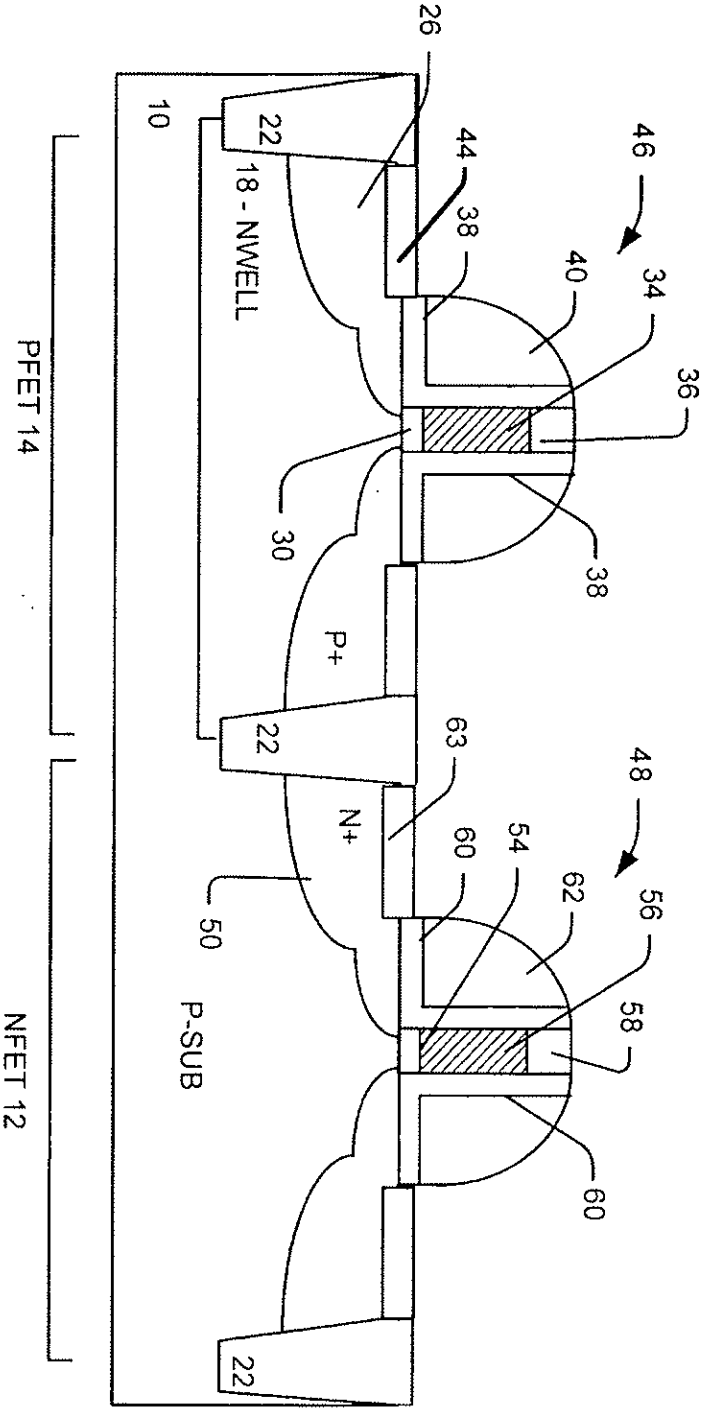

26
22
18 - NWELL
10
44
38
46
34
40
36
30
38
P+
22
63
48
N+
60
54
62
56
58
50
P-SUB
60
22
PFET 14
NFET 12

FIG. 2

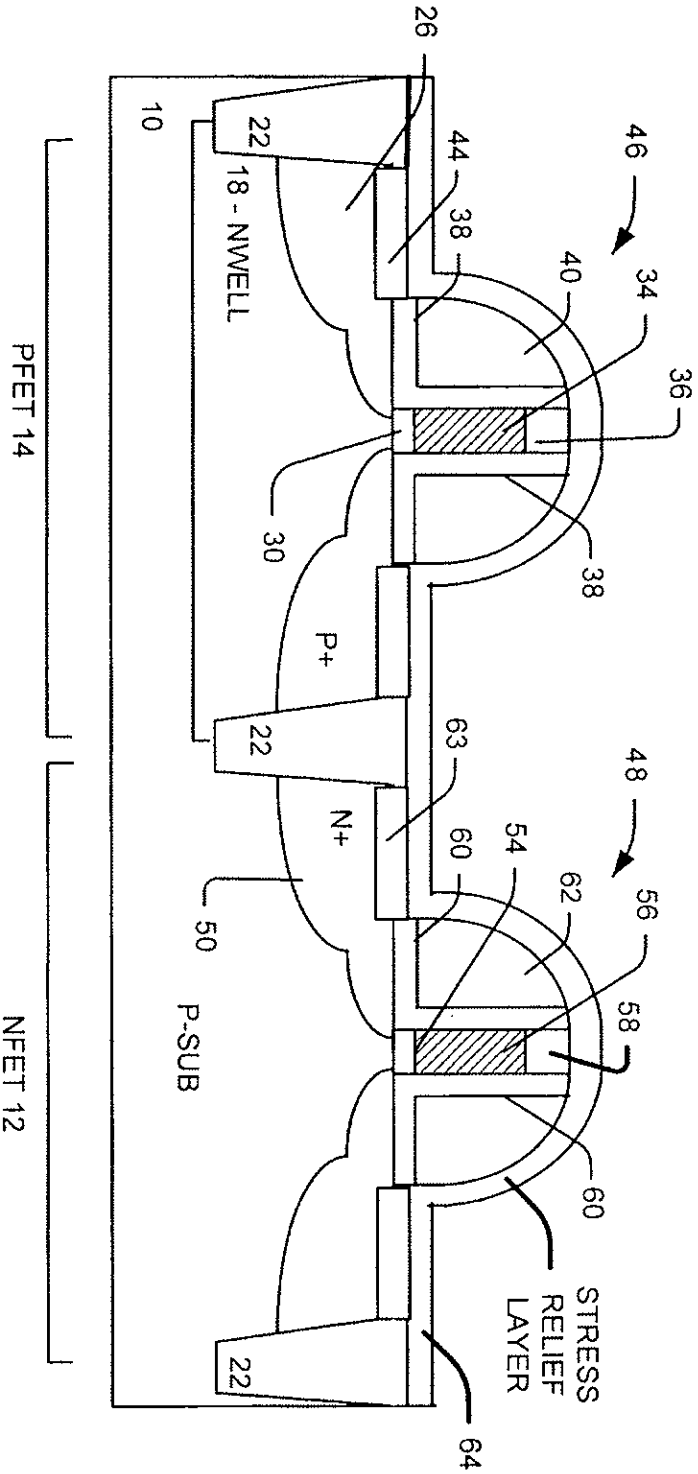

26
46
44
38
40
34
36
22
18 - NWELL
10
30
38
P+
63
48
22
N+
60
54
62
56
58
50
P-SUB
60
STRESS
RELIEF
LAYER
22
64
PFET 14
NFET 12

FIG. 3

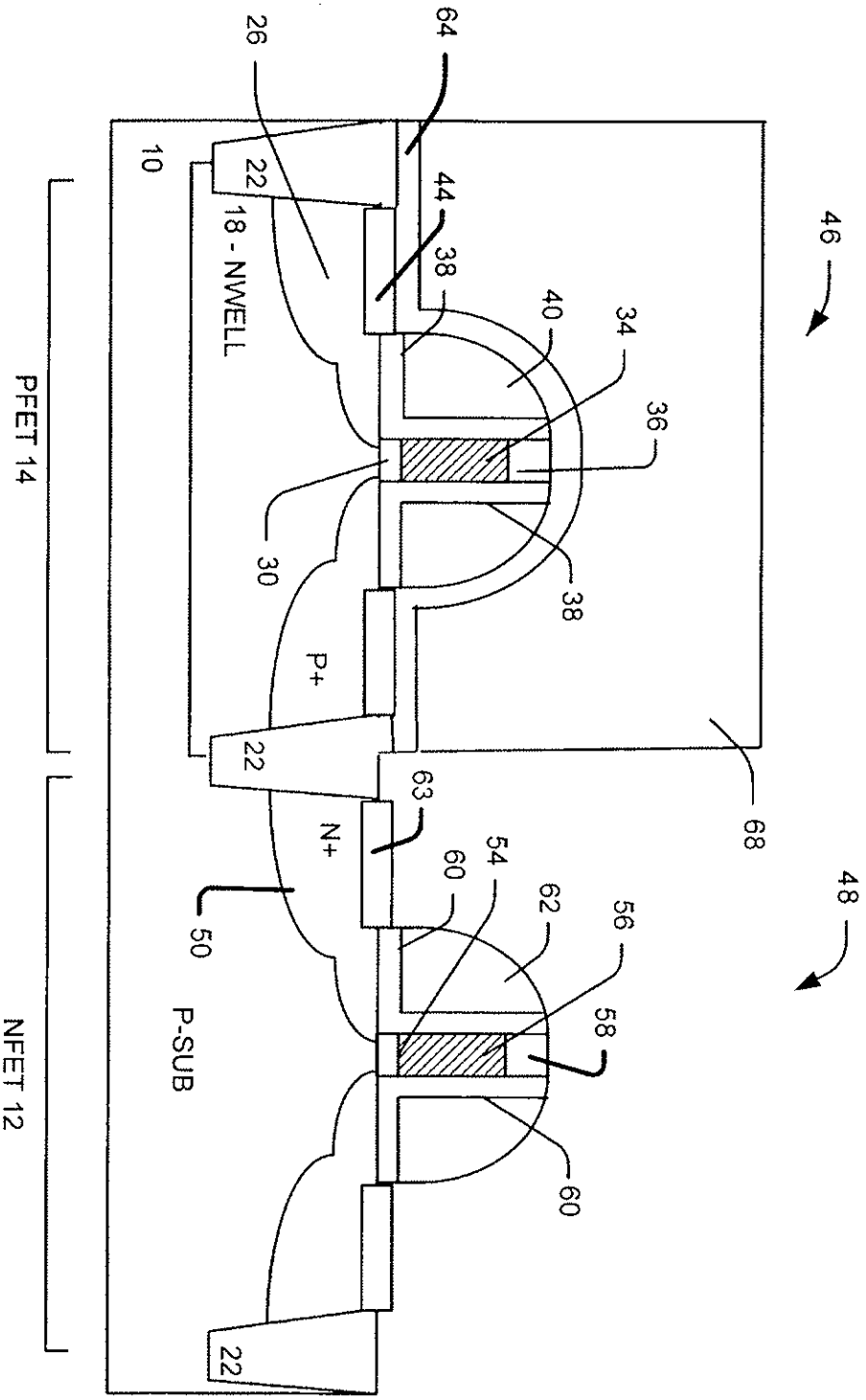
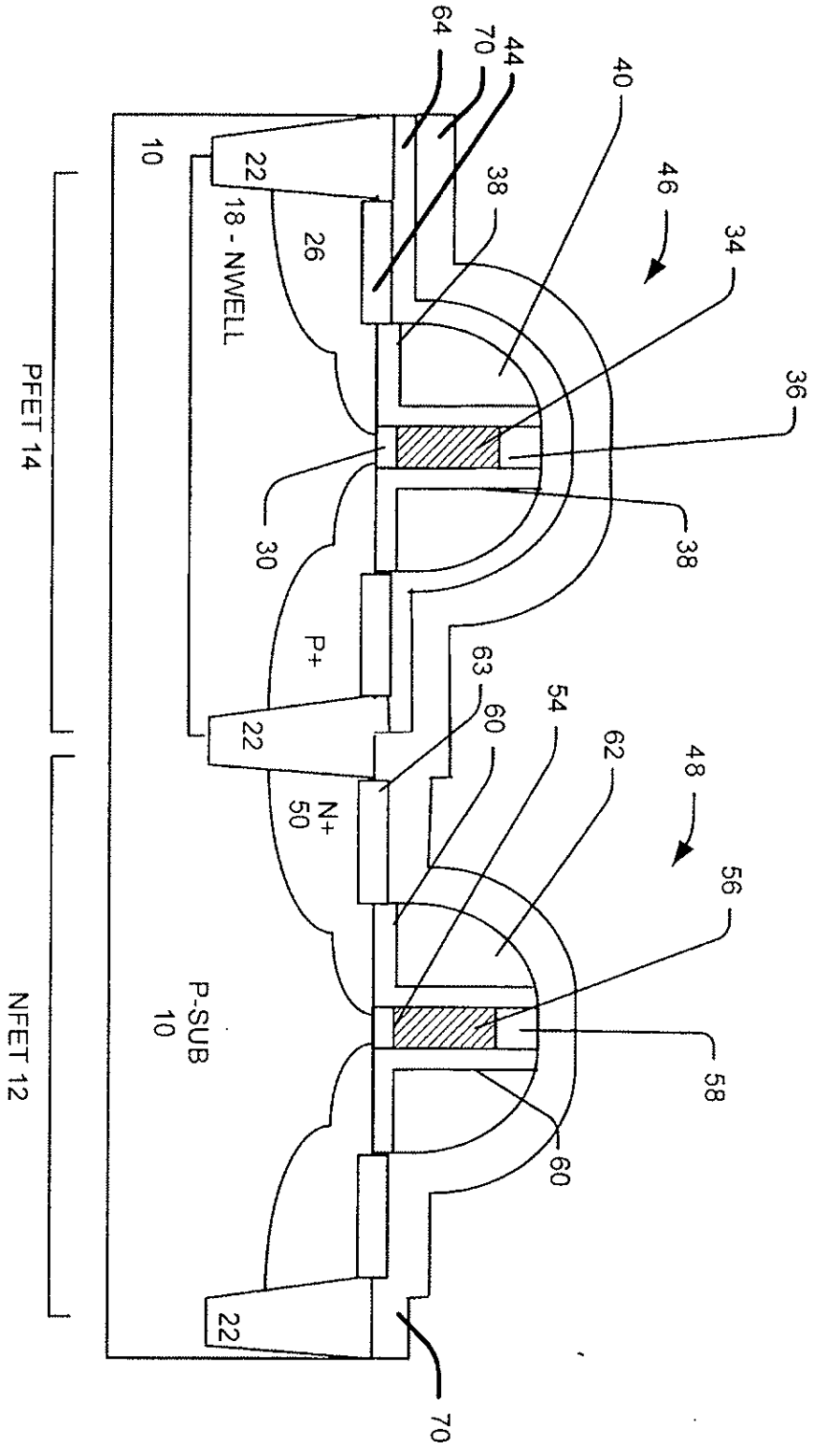

64
26
22
10
18 - NWELL
44
38
40
34
36
30
38
P+
22
63
N+
54
60
62
56
58
60
50
P-SUB
22
68
46
48
PFET 14
NFET 12

FIG. 4


64
70
44
40
46
34
36
38
22
18 - NWELL
26
10
30
38
P+
63
60
54
62
48
22
N+
50
56
58
60
P-SUB
10
PFET 14
NFET 12
22
70

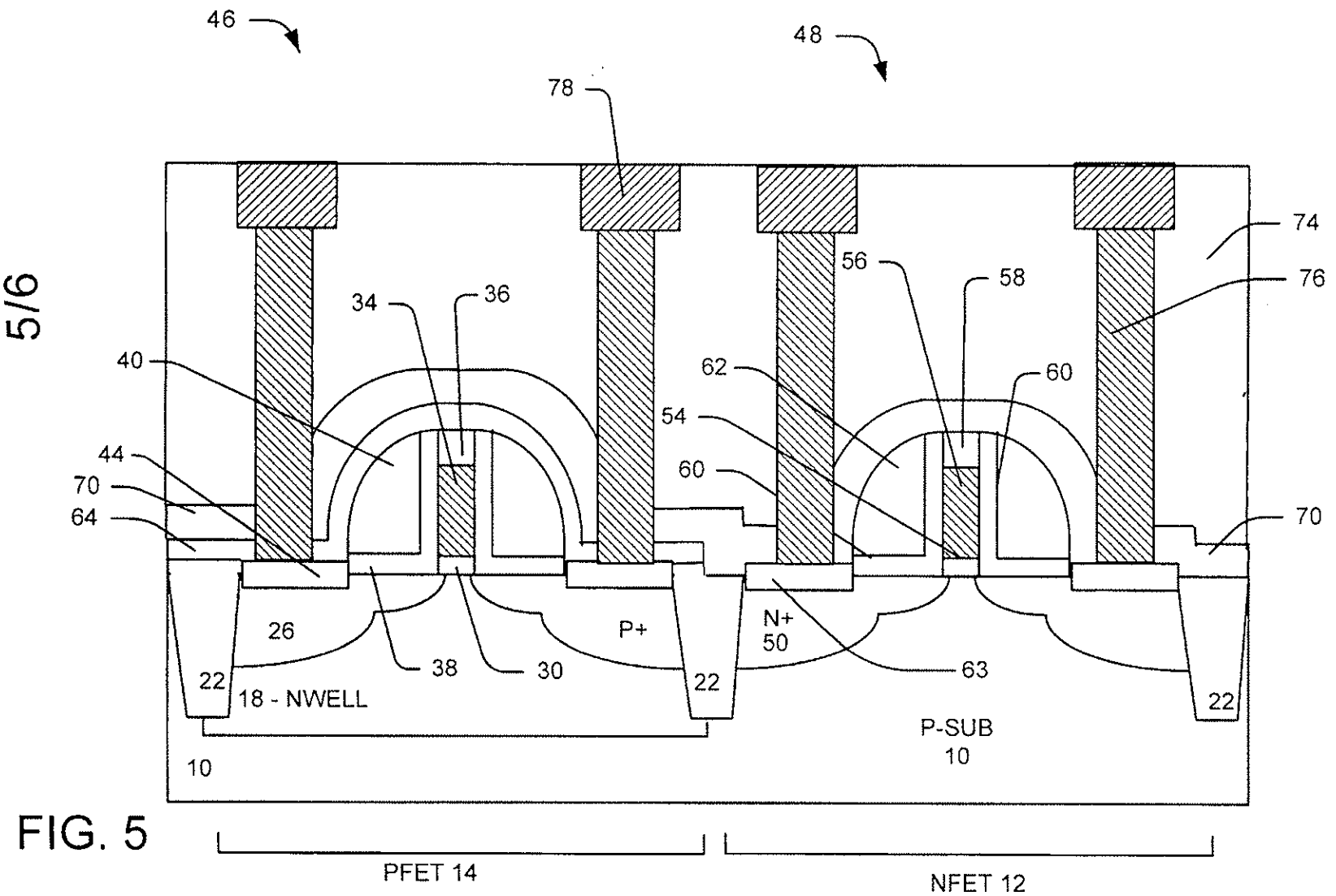

46
48
78
74
56
58
76
34
36
40
62
60
54
44
60
70
64
70
26
P+
N+
50
38
30
63
22
22
22
18 - NWELL
P-SUB
10
10
PFET 14
NFET 12

FIG. 5

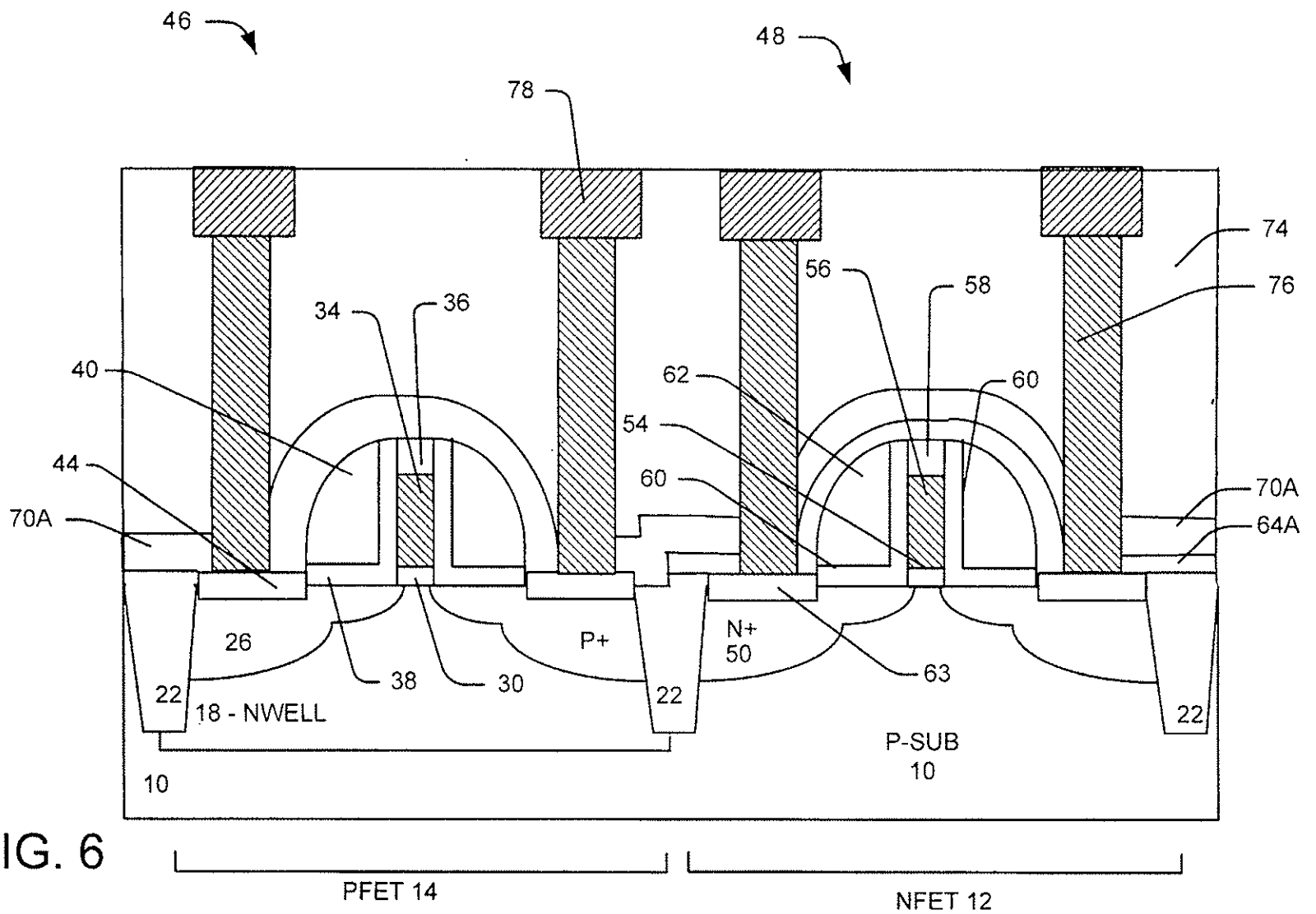

46
48
78
74
56
58
76
34
36
40
62
60
54
44
60
70A
70A
64A
26
P+
N+
50
38
30
63
22
18 - NWELL
22
22
P-SUB
10
10
PFET 14
NFET 12

FIG. 6