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METHOD FOR DEPOSITING A DIFFUSION BARRIER

Field of the Invention

The present invention relates generally to the processing of semiconductor devices, and more specifically to providing a diffusion barrier onto a semiconductor device.

Background of the Invention

Modern semiconductor devices are requiring speeds in excess of 200 megahertz. In order to form future generations of semiconductor devices, copper (Cu) will essentially be required for interconnects. One problem with the use of copper is that copper cannot directly contact silicon dioxide because copper diffuses too easily through the silicon dioxide layer. Therefore, in the prior art the copper is typically surrounded by a diffusion barrier on all sides.

Diffusion barriers for copper include a number of materials, such as silicon nitride and various refractory metal nitrides (TiN, TaN, WN, MoN) and refractory silicon nitrides (TiSiN, TaSiN, WSiN), or refractory metal-semiconductor-nitride layers. Of all of these barriers, the two showing promise for barriers include tantalum nitride (TaN) and tantalum silicon nitride (TaSiN). These materials are usually deposited by sputtering. However, sputtering generally has poor sidewall step coverage, where step coverage is defined to be the percentage of a layer being deposited on a specific surface divided by the thickness of a layer being deposited on the uppermost surface of a semiconductor device. In the case of sputtered tantalum nitride (TaN) and tantalum silicon nitride (TaSiN), and the step coverage for a 0.35 μm via can be in the range of 5% to 20% for an aspect ratio of 3:1. Such low step coverage increases the risk that the barrier material will not be thick enough to be an effective diffusion barrier along the sides and bottom of a deep opening. In an attempt to get enough of the material along the walls of openings, a much thicker layer at the uppermost surface is deposited, however, this is undesirable because it increases the resistance of the interconnect.

Chemical vapor deposition (CVD) has been used to form tantalum nitride. The precursors for TaN includes tantalum halides, such as Tantalum Pentachloride ($TaCl_5$). The problem with tantalum halides is that the halides react with the copper causing interconnect corrosion. Another precursor includes penta[dimethylamido]tantalum ($Ta(NMe_2)_5$). When this precursor is used to deposit tantalum nitride (TaN), the compound that is actually forms is an insulating layer of Ta_3N_5. An insulator cannot be used in contact openings or via openings because the insulator prevents electrical contact between the upper interconnect layer and the lower interconnect layer.

Still another known precursor includes terbutylimido-tris-diethyl amino tantalum [(TBTDET), $Ta{=}NBu(NEt_2)_3$]. This compound can be used to form TaN. However, there are problems associated with this precursor. Specifically, deposition temperatures higher than 600°C is needed to deposit reasonably low resistivity films. Such high temperatures for back-end metallization are incompatible for low-k dielectrics and also induces high stresses due to thermal mismatch between the back-end materials. Another problem with the TBTDET precursor is that too much carbon (C) is incorporated within the layer. This compound generally has approximately 25 atomic percent carbon. The relatively high carbon content makes the layer highly resistive, and results in films that are less dense, lowering the diffusion barrier effectiveness for a comparable thickness of other materials. The resistivity of TaN when deposited using TBTDET at temperatures lower than 600°C is approximately 12,000 μohm-cm. Films with such a high resistivity (desired is less than approximately 1000 μohm-cm) cannot be used for making effective interconnect structures.

CVD of titanium silicon nitride (TiSiN) has been demonstrated using titanium tetrachloride ($TiCl_4$). This compound is again undesirable because in forming the TiSiN, chlorine is once again present which causes corrosion of copper and other materials used for interconnect.

A need, therefore, exists to deposit a TaN or TaSiN using organo-metallic precursors that can be formed relatively conformally with a reasonable resistivity and good barrier properties at lower wafer temperatures.

Brief Description Of The Drawings

The present invention is illustrated by way of example and not limited in the accompanying figures, in which like references indicate similar elements, and in which:

FIG. 1 includes an illustration of a cross-sectional view of a portion of semiconductor device substrate after forming openings in an interlevel dielectric layer to doped regions within the substrate;

FIG. 2 includes an illustration of a cross-sectional view of FIG. 1 after forming materials needed to form interconnects in accordance with one embodiment of the present invention;

FIG. 3 includes an illustration of a substrate of FIG. 2 after forming inlaid interconnects to doped regions within the substrate;

FIG. 4 includes an illustration of a top view of the substrate of FIG. 3. after forming an interlevel dielectric layer and an opening within that layer;

FIG. 5 includes an illustration of a cross-sectional view of the substrate of FIG. 4 illustrating the opening to the lower interconnect;

FIG. 6 includes an illustration of a cross-sectional view of the substrate of FIG. 5 after forming an interconnect to a lower interconnect level; and

FIG. 7 includes in illustration of a cross-sectional view of the substrate of FIG. 6 after forming a substantially completed device.

Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity, and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures are exaggerated relative to other elements to help to improve understanding of embodiment(s) of the present invention.

Detailed Description Of The Drawings

A refractory Metal Nitride and a refractory metal Silicon Nitride layer are formed using metal organic chemical deposition. More specifically, tantalum nitride (TaN) can be formed by a Chemical Vapor Deposition (CVD) using Ethyltrikis (Diethylamido) Tantalum [(ETDET), $(Et_2N)_3Ta{=}NEt$] and ammonia (NH_3). By the inclusion of a semiconductor source such as silane (SiH_4), a tantalum silicon nitride (TaSiN) layer can also be formed. Both of these layers can be formed at

wafer temperatures lower than 500° Celsius with relatively small amounts of carbon (C) within the film. Therefore, the embodiments of the present invention can be used to form tantalum nitride (TaN) or tantalum silicon nitride (TaSiN) layer that is relatively conformal and has reasonably good diffusion barrier properties.

As used in this specification, chemical vapor deposition is one type of deposition method that is to be distinguished from sputter deposition. Sputter deposition is essentially a physical type of deposition in which a layer is being deposited onto a wafer by the action of a plasma directed toward a target. The material evolves from the target and is deposited in a substantially vertically orientation to the wafer. Chemical vapor deposition on the other hand is a chemical reaction that occurs at or near the surface of the substrate to form a layer along the exposed surfaces of the wafer.

Tantalum nitride (TaN) and tantalum silicon nitride (TaSiN) are formed using ETDET/NH_3, and ETDET/NH_3/SiH_4 respectively. For TaN, the deposition generally takes place in a CVD reactor at a pressure in the range of 5-15 Torr. The monitored deposition temperature varies depending upon where the temperature is being monitored. If the heater block temperature is being monitored, the temperature is generally in a range of approximately 400-480° Celsius. If the wafer temperature is measured, the temperature is typically in a range of approximately 350-400° C.

The ETDET is introduced using Helium (He) as a carrier gas that is bubbled through the ampoule. The flow rate of the Helium (He) is in the range of 200-800 sccm. The heater box temperature for the ampoule is maintained at approximately 80° Celsius. In general, the heater box temperature can be maintained within a range of approximately 50-90° Celsius. The temperature of the ETDET within the ampoule is approximately about 10° Celsius lower than the heater box temperature. Ammonia (NH_3) is introduced at a rate ranging from 200-500 sccm which generally gives a deposition rate of approximately 150-200 Å/minute The deposition rate will also depend on the reactor configuration. Using these parameters TaN film can be deposited that has less than 15% carbon (C) and is generally no more than 1%. When used as a barrier layer, the layer TaN is usually deposited to a thickness in a range of approximately 200-300 Å along an exposed surface of the substrate, and generally has step

coverage of greater than 50 % at the bottom surface of an opening having an aspect ratios of 3:1.

The flow of ammonia has been observed to enhance the deposition across all temperature ranges. Without ammonia limited or no deposition is observed even at high wafer temperatures. This is in contrast to the precursor (TBTDET) used to deposit TaN as reported in literature, which reported deposition without ammonia (NH_3).

In CVD systems, there is typically more difficulty depositing the layer at the bottom of the opening, and therefore, the step coverage at the bottom is a good indicator of the thinnest portion of the film. The TaN also has been found to have reasonably good adhesion to the surfaces of both metals and oxides. This is important for integrating the layer into an interconnect process. Should the layer be used to make contact (electrical or physical) to a Silicon containing layer such as a gate electrode or doped regions within a semiconductor substrate, titanium may be deposited between the TaN and Silicon (Si) to form a good ohmic contact. Without the titanium, a relatively high contact resistance between TaN and p+ Silicon may be formed because of large differences in the work functions between p+ silicon and tantalum nitride.

The deposition parameters for TaSiN are the same except as noted below. The pressure is typically in a range of approximately 0.1 to 1 Torr. The flow rates are slightly changed in that: the Helium (He) flows at a rate of approximately 50-150 sccm at the same conditions for the ampoule as described earlier for TaN; ammonia (NH_3) is introduced at a rate of approximately 150-300 sccm; and silane (SiH_4) is introduced at approximately 1-10 sccm. These parameters give a deposition rate of approximately 150-250 Å/minute with approximately the same carbon incorporation and adhesion characteristics as the TaN.

Different source gases may be used for the Silicon source and the TaN precursor. Specifically, it is possible that Disilane (Si_2H_6) or some other Silicon gas could be used. In addition, it is believed that source gasses containing other semiconductor souces, such as germanium will work as well. However, care should be exercised, in assuring that gas phase reaction is not present. Also, the wafer temperature of the deposition should not exceed 500° Celsius, and be typically less than 400 ° Celsius, because of the issues noted previously. The TaN precursor has similar concerns. In general, the ethyl group attached to the doubly bonded nitrogen can comprise either an ethyl [$(Et_2N)_3Ta{=}NEt$] or a

methyl [$(Et_2N)_3Ta{=}NMe$] group. The carrier gas for the ampoule includes helium (He), argon (Ar), nitrogen (N_2) or hydrogen (H_2).

Following deposition of a TaN films by CVD, the films can be exposed to an in-situ plasma treatment which allow a reduction in resistivity of the deposited films. Different gases, including argon, hydrogen, nitrogen, silane, and ammonia, individually or in combination can be used for plasma treatment. For example, the use of argon generally allows a reduction in resistivity of the films by a factor of 2 or more. Other gases generally work best in combination with argon although this is not necessary. Use of silane will allow incorporation of Si in the films, thus forming TaSiN in the matrix. This method allows control over the Si to N ratio in the film. The flow rate for the gases can range from 100-1000 sccm; pressure ranging from 100 mTorr- 15 Torr; and plasma power ranging from 100- 2000 Watts. The plasma treatment can also be done intermittently, that is, deposition/plasma/deposition steps. Further, thermal annealing of films by SiH4 can also be done instead of using plasma in order to incorporate Si in the films. The process involves flowing SiH4 flow over the heated wafers after deposition step. Anneal conditions similar to plasma can be used except that there would be no plasma.

Embodiments of the present invention are better understood with the example that follows in which two levels of interconnects are formed using the chemically vapor deposited material. FIG. 1 includes an illustration of a cross-sectional view of a portion of a semiconductor device substrate 10 before interconnects are formed. The semiconductor device substrate 10 is a monocrystalline semiconductor wafer, a semiconductor-on-insulating wafer, or any other substrate used to form semiconductor devices. Field isolation regions 12 are formed over the semiconductor device substrate 10. Doped regions 14 are source/drain regions for a transistor and lie within the substrate 10 adjacent to the field isolation regions 12. A gate dielectric layer 22 and gate electrode 24 overlie the substrate 10 and portions of the doped regions 14. An interlevel dielectric layer 26 is deposited over the semiconductor device substrate 10. The interlevel dielectric layer 26 can include an undoped, a doped, or combination of doped and undoped silicon dioxide films. In one particular embodiment, an undoped silicon dioxide film is covered by a borophosphosilicate glass (BPSG) layer. After planarization of layer 26,, openings 28 are formed through the interlevel dielectric layer 26 and extend to the doped regions

14. As illustrated in FIG. 1, the openings 28 include a contact portion which is relatively narrow that contacts the doped regions 14, and a relatively wider interconnect trench, which is where the interconnect is formed. In one example of FIG. 1, the contact portion has an aspect ratio is 3:1 as compared to the trench. This is an example of a dual damascene process for forming inlaid interconnects which are generally known within the prior art.

The materials used to form the contacts and interconnects are then deposited over the interlevel dielectric layer 26 and within the openings 28. As illustrated in FIG. 3, which illustrates a partially completed device, layer 32 of titanium or other refractory material is formed, and is in contact with the doped regions 14. This layer generally has a thickness in a range of approximately 100-400 Å. Next, a TaN or TaSiN layer 34 is formed over layer 32. The tantalum nitride layer 34 or TaSiN layer 34 is formed using the previously described deposition parameters. The thickness of the layer is in the range of approximately 200 to 300 Å. A conductive layer 36 is formed within the remaining portions of the openings and overlying 34. The conductive layer 36 typically includes copper (Cu), aluminum (Al), tungsten (W) or the like. In this particular embodiment, the conductive layer 36 is copper. The partially completed device is then polished to remove the portions of layers 32, 34 and 36 that overlie the interlevel dielectric layer 26. This forms contact portions and interconnect portions for the interconnects 44 and 42 as illustrated in FIG. 3.

A second interlevel dielectric layer 56 is deposited and patterned over the interconnects 42 and 44 and the first interlevel dielectric layer 26. FIGS. 4 and 5 illustrate top and cross-sectional views, respectively, of the second interlevel dielectric layer after patterning. The second interlevel dielectric layer 56 includes a doped or undoped oxide. The patterning forms a via opening 52 and an interconnect trench 54. Other via openings and interconnect trenches are formed but are not shown in Figs. 4 and 5.

As illustrated in FIG. 6, TaN or TaSiN layer 64 is then deposited using one of the previously described deposition techniques. Layer 64 contacts the lower interconnect 42. Layer 64 has a thickness in a range of approximately 200 to 300 Å and is covered by a second conductive layer 66 using a material similar to layer 36. The portions of the layers 64 and 66 overlying the second interlevel dielectric layer outside of the interconnect trench are then removed by polishing to give the structure as

illustrated in FIG. 6. The combination of layers 64 and 66 forms a bit line 62 for the semiconductor device. A substantially completed device 70 is formed after depositing a passivation layer 72 overlying the second level interconnects, as illustrated in FIG. 7. In other embodiments, other insulating layers and interconnects levels can be formed but are not shown in the figures.

Many benefits exist for embodiments of the present invention. The CVD reaction that forms TaN or TaSiN is performed at wafer temperatures lower than approximately 500° Celsius, and typically less than 400° Celsius. Therefore, the process is compatible with low-k dielectrics and does not induce high stresses in the films. The amount of carbon incorporation is less than 15 atomic percent, and typically 1 atomic% or less. Therefore, the film does not have porous qualities and is a better diffusion barrier compared to using TBTDET as a precursor. The reduced carbon results in a resistivity of the CVD TaN films that are at least an order of magnitude lower compared to the prior art use of the TBTDET. Still, other advantages with the embodiments is the relative ease of integration into an existing process flow.

Thus it is apparent that there has been provided, in accordance with the invention, a process for depositing a diffusion barrier to fabricate a semiconductor device, which fully meets the advantages set forth above. Although the invention has been described and illustrated with reference to specific illustrative embodiments thereof, it is not intended that the invention be limited to those illustrative embodiments. Those skilled in the art will recognize that variations and modifications can be made without departing from the spirit of the invention. It is therefore intended to include within the invention all such variations and modifications as fall within the scope of the appended claims and equivalents thereof.

CLAIMS

We claim:

1. A method of forming a semiconductor device comprising the steps of:
placing a semiconductor substrate into a chemical vapor deposition (CVD) reactor;
introducing a metal organic precursor into the (CVD) reactor;
introducing a semiconductor source into the (CVD) reactor; and
reacting the metal organic precursor, and the semiconductor source to form a refractory metal-semiconductor-nitride layer.

2. The method of claim 1, wherein:
the step of introducing metal organic precursor further comprises the metal organic precursor comprising tantalum;
the step of introducing a semiconductor source further comprises the semiconductor source comprising silicon; and
the step of reacting further includes reacting the metal organic precursor, and the semiconductor source to form a tantalum-silicon-nitride layer.

3. The method of claim 1, including an additional step of:
introducing ammonia into the CVD reactor; wherein
the step of reacting includes reacting the ammonia, the metal organic precursor, and the semiconductor source to form a refractory metal semiconductor-nitride layer; and wherein
the step of introducing the semiconductor source includes the semiconductor source being silane.

4. The method of claim 1 wherein the step of introducing a metal organic precursor includes the metal organic precursor being $[(R^1)_2N)]_3$-Ta=NR^2, where R^1 comprises an ethyl, and R^2 comprises one of an ethyl and a methyl.

5. A method of forming a semiconductor device comprising the steps of:
forming an insulation layer over a semiconductor device substrate, wherein the insulation layer has an opening;
depositing a refractory metal-semiconductor-nitride layer using chemical vapor deposition; and
forming a conductive layer after the refractory metal-semiconductor-nitride layer, wherein the conductive layer comprises aluminum or copper.

6. The method of claim 5, wherein the step of forming the conductive layer includes forming the conductive layer to comprise copper, and wherein the combination of the conductive layer and the refractory metal-semiconductor-nitride layer form an interconnect.

7. The method of claim 1 or 5, wherein refractory metal-semiconductor-nitride layer has a carbon content of less than approximately 15 atomic percent.

8. The method of claim 1 or 5, wherein the refractory metal-semiconductor-nitride layer is formed at a wafer temperature of less than approximately 500° Celsius.

9. The method of claim 1 or 5, wherein the refractory metal-semiconductor-nitride layer has a step coverage of greater than approximately 50%.

10. The method of claim 9, wherein the step coverage of greater than approximately 50% occurring in a feature having an aspect ratio of approximately 3:1 or greater.