CLAIMS:

1. A processor comprising:

a general purpose processor core;

a three-dimensional (3D) integrated circuit stack including multiple graphics processor cores, the 3D integrated circuit stack coupled to the general purpose processor core; and

interconnect logic having at least one data channel, to interconnect the graphics processor cores of the 3D integrated circuit stack and couple the graphics processor cores with a shared resource, the interconnect logic further to enable data distribution between the graphics processor cores and the shared resource over a virtual channel including multiple programmatically pre-assigned traffic classifications.

2. The processor of claim 1, wherein the at least one data channel is a shared bus.

3. The processor of claim 1, wherein the interconnect logic includes multiple data channels.

4. The processor of claim 3, wherein each of the multiple data channels is a separately clock gated bus, and wherein each bus is to use early indications to signal incoming activity.

5. The processor of claim 1, wherein the shared resource is a shared memory resource.

6. The processor of claim 5 wherein the shared memory resource is a shared cache.

7. The processor of claim 1, wherein the interconnect logic is to enable the data distribution over multiple virtual channels, the multiple virtual channels including the virtual channel and one or more additional channels.

8. The processor of claim 7, wherein the multiple virtual channels are to be arbitrated based on a programmable priority system.

9. The processor of claim 8, wherein each of the multiple virtual channels is to be assigned multiple traffic classifications.

10. The processor of claim 9, wherein each of the multiple traffic classifications includes a programmable priority.

11. The processor of claim 10, wherein the programmable priority is relative to traffic classifications within a same virtual channel of the multiple virtual channels.

12. The processor of claim 1, wherein the interconnect logic operates at a higher frequency than the graphics processor cores.

13. The processor of claim 1, additionally including a set of interconnect nodes to couple the graphics processor cores with the interconnect logic, wherein the interconnect logic includes multiple data channels and the set of interconnect nodes is configured to switch data between the multiple data channels when transiting one of the graphics processor cores.

14. A system comprising:

a processor including a three-dimensional (3D) circuit stack including a plurality of cores, at least one of the plurality of cores including an instruction set for processing graphics instructions, the at least one core to be coupled with a shared resource on the processor via interconnect logic having at least one clock gated physical data channel and a set of virtual channels including one or more virtual channels, the one or more virtual channels having multiple programmatically pre-assigned traffic classifications; and

memory coupled to the at least one core and the interconnect logic, the memory to store data for the at least one core before transmission via the interconnect logic.

15. The system as in claim 14 wherein the shared resource on the processor is a shared memory resource.

16. The system as in claim 15, wherein the shared memory resource includes a shared cache memory.

17. The system of claim 14, wherein the set of virtual channels includes multiple virtual channels, wherein the multiple virtual channels in the set of virtual channels are to be arbitrated based on a programmable priority system.

18. The system of claim 17, wherein each of the multiple programmable traffic classifications is prioritized relative to other traffic classes assigned to the same virtual channel of the multiple virtual channels.

19. The system of claim 14, wherein the system is a system on a chip integrated circuit.

20. A non-transitory machine-readable medium having stored thereon data, which if performed by at least one machine, causes the machine to fabricate a system on a chip integrated circuit including a three-dimensional (3D) circuit stack of multiple graphics processor cores to perform a method comprising:

determining a channel access status on a multiple node shared bus for a message from a source node to a target node, wherein at least one node of the multiple node shared bus couples with a graphics processor core of integrated circuit and at least one node of the multiple node shared bus couples with a shared resource on the integrated circuit;

transmitting a message from the source node to the target node over a first data channel, wherein the message is associated with a first traffic classification having a first priority;

receiving the message at a first data bus connector coupled with the graphics processor core; and

based on at least the source node and the target node, switching the message from the first data channel to a second data channel.

21. The non-transitory machine-readable medium of claim 20, additionally including determining that the message is associated with the first traffic classification and switching the message from the first data channel to the second data channel based at least on the first traffic classification.

22. The non-transitory machine-readable medium of claim 20, wherein determining the channel access status comprises:

determining, using a channel access protocol, if a third data channel is available to transmit the message from the source node to the target node; and

after determining that transmission over the third data channel is blocked, transmitting the message over the first data channel.

23. The non-transitory machine-readable medium of claim 22, wherein the first, second, and third data channel are virtual data channels.

24. The non-transitory machine-readable medium of claim 22, wherein the channel access protocol is a time division multiple access protocol.

25. The non-transitory machine-readable medium of claim 22, wherein the channel access protocol is a carrier sense multiple access protocol.