

MOSFET Protection Circuit

This invention relates to circuits employing metal-oxide-semiconductor field effect transistors (MOSFETs).

Such circuits are commonly found, for example, in electrically programmable read only memory (EPROM), electrically erasable programmable read only memory (EEPROM) and display drivers. Usually such circuits are fabricated in integrated form and in order to minimise power consumption use CMOS components. A CMOS integrated circuit can support voltages up to certain physical limits which depend on process characteristics. In the case of an EEPROM circuit, a voltage as high as possible must be applied to a memory cell in order to program data into the cell. The upper bound for this programming voltage depends on certain limiting parasitic effects and is typically in the range of 20 to 30 volts. An important parasitic limiting effect is a gate-aided breakdown effect known as 'BVDSS' breakdown, which occurs at the high voltage drain end of a turned off transistor at voltages lower than the junction breakdown voltage.

A known mechanism for protecting a MOSFET transistor in an EEPROM against BVDSS breakdown utilises an additional MOSFET transistor connected with its current electrodes in series between the drain of the transistor to be protected and a node which would otherwise be directly connected to the drain. The gate electrode of the additional protection transistor is connected to a source of voltage intermediate the high level (programming) and low level (normal) voltages supplied to the EEPROM. This intermediate voltage should be as high as possible so as to avoid gate-aided breakdown at the protection transistor's own drain, but not so high as to allow the protection transistor's source to rise above the BVDSS value of the transistor to be protected.

One circuit employing such protection for a MOSFET transistor by utilising an additional protection transistor requires a voltage divider to generate the protection

5 voltage for gating the protection transistor. The voltage divider is fed from a high voltage and usually draws a DC current, which is clearly not desirable.

10 Another circuit employing such protection for a MOSFET transistor by utilising an additional protection transistor requires a voltage multiplier to generate, from the normal (non-programming) voltage applied to the circuit, the protection voltage for gating the protection transistor. However, this arrangement has the disadvantage that BVDSS breakdown protection is not provided if the high (programming) voltage is present without the normal supply.

15 It is an object of the present invention to provide a circuit employing BVDSS breakdown protection of a MOSFET transistor wherein the above disadvantages may be overcome, or at least alleviated.

In accordance with the invention a MOSFET transistor protection circuit comprising:

20 a first MOSFET transistor having drain and source electrodes coupled between a first node for receiving a supply voltage of predetermined first and second values and a second node for receiving a datum voltage; and

25 a second MOSFET transistor of the same channel type as the first transistor having drain and source electrodes connected in series between the first node and the drain and source electrodes of the first transistor and having its gate electrode coupled to a third node for receiving a protection voltage;

30 and means for generating the protection voltage at a level between the predetermined first and second values such that the first transistor is protected against BVDSS breakdown,

characterized in that the protection voltage generating means is coupled to the first node and comprises:

35 a third MOSFET transistor arranged to receive the protection voltage at its gate electrode; and

means for monitoring current produced in the third transistor due to BVDSS breakdown and for varying the protection voltage accordingly so as to reduce the monitored current.

Two circuits in accordance with the invention will now be described, way of example only, with reference to the accompanying drawings, in which:

Figure 1 shows a circuit diagram of a first circuit
5 employing BVDSS breakdown protection for an N-channel MOSFET transistor; and

Figure 2 shows a circuit diagram of a second circuit employing BVDSS breakdown protection for N-channel and P-channel MOSFET transistors.

10 Referring firstly to Figure 1, in an integrated circuit EEPROM memory an N-channel MOSFET transistor 2 has its source and gate electrodes connected to ground. The drain electrode of the transistor 2 is connected to the source electrode of a transistor 4. The drain electrode of
15 transistor 4 is connected to a node 5 to which is applied a supply voltage which can be of high (programming) value V_{pp} or low (normal) value V_{dd} . The gate electrode of the transistor 4 is connected to receive a protection voltage V_{prot} whose generation will be described hereafter. As
20 described above, the transistor 4 serves to protect the transistor 2 against BVDSS breakdown at its drain in conventional manner by ensuring that the voltage at the drain of the transistor 2 is below the BVDSS value of the transistor: the source of transistor 4 will not rise above a
25 level equal to the protection voltage V_{prot} minus the threshold voltage V_{th} of the transistor 4.

The protection voltage V_{prot} is generated by a circuit comprising three MOSFETs 6, 8, 10. Transistors 6, 8 are P-channel transistors each having their drain electrodes
30 connected to the node 5 which is connected to the supply line. The source electrode of transistor 8 is connected to the gate electrodes of transistors 6, 8 and to the drain electrode of transistor 10 which is an N-channel transistor. The source electrode of transistor 10 is open
35 circuited, and the gate electrode of transistor 10 is connected both to the source electrode of transistor 6 and to a node 14 for connection to the gate electrode of transistor 4.

In use of the circuit of Figure 1, the N-channel transistor 10 will have a BVDSS current when its gate is at a low voltage and the supply line voltage at node 14 is high (V_{pp}). This current is mirrored by the two P-channel transistors 6, 8 which cause the protection voltage V_{prot} at the source of transistor 6 to rise until BVDSS current ceases, i.e. until BVDSS breakdown stops. It will be understood that the protection voltage V_{prot} generated at the node 14 can also be used for all other N-channel protection MOSFETs (not shown) in the same integrated circuit.

It will be understood that in order to protect a P-channel MOSFET in a similar way using a P-channel MOSFET protection transistor, a similar circuit structure to that of the protection voltage generating components 6, 8, 10 can be used, each of the transistors 6, 8, 10 being replaced by a transistor of opposite channel type. In this case BVDSS breakdown would occur when the gate voltage comes close to the high supply voltage V_{pp} . Such a voltage protection generating arrangement is shown in Figure 2 in transistors 38, 40, 42.

Referring now to Figure 2, in an integrated circuit EEPROM memory incorporating both N-channel and P-channel MOSFET transistors 22, 24 (e.g. a CMOS memory), the transistors are protected in conventional manner respectively by MOSFET transistors 26, 28 of similar conductivity type to their respective transistors 22, 24. Both the transistors 26, 28 are gated by the same protection voltage V_{prot} which is intermediate the high supply voltage V_{pp} and ground.

As in the circuit of Figure 1, the protection voltage is generated from the high supply voltage V_{pp} and a transistor arrangement 30, 32, 34 (corresponding in channel type and connections to the transistor arrangement 6, 8, 10 in Figure 1) is used to prevent the protection voltage V_{prot} from causing BVDSS breakdown in N-channel transistors such as transistor 28 to which it is applied. In order to prevent BVDSS breakdown in P-channel transistors such as

transistor 26 to which the protection voltage is applied, node 36 from which the output from arrangement 30, 32, 34 is taken is also connected to the drain electrode of an N-channel MOSFET transistor 38. The source electrode of transistor 38 is connected to ground. An N-channel MOSFET transistor 40 has its source electrode connected to ground and has its drain electrode connected to the gate electrodes of transistors 38, 40 and to the source electrode of a P-channel transistor 42. Transistor 42 has its drain electrode open circuited and has its gate electrode connected to the node 36. It will be appreciated that transistor arrangement 38, 40, 42 forms the symmetrical complement to the already described transistor arrangement 30, 32, 34 and functions in an symmetrically complementary manner to prevent BVDSS breakdown in P-channel MOSFETs such as transistor 22. Thus the protection voltage V_{prot} generated in the circuit of Figure 2 can vary within a limited range: the lowest value of V_{prot} is above that gate voltage which avoids BVDSS breakdown of an N-channel transistor and the highest value of V_{prot} is below that gate voltage which avoids BVDSS breakdown of a P-channel transistor.

It will be appreciated that in the above described circuits the protection voltage V_{prot} is generated by simple circuitry, is self adjusting and has no DC consumption.

It will also be appreciated that although the invention has been described in relation to CMOS EEPROM devices, the invention may be of use in a wide range of other applications where MOSFETs are used with high voltages such as, for example, display drivers.

It will also be appreciated that the invention may be used in integrated circuits in which high voltages are applied only from externally (e.g. EPROMs), since the invention does not require an on-chip charge pump.

CLAIMS

- 5 1. A MOSFET transistor protection circuit comprising:
a first MOSFET transistor having drain and source
electrodes coupled between a first node for receiving a supply
voltage of predetermined first and second values and a second
node for receiving a datum voltage; and
10 a second MOSFET transistor of the same channel type as the
first transistor having drain and source electrodes connected in
series between the first node and the drain and source electrodes
of the first transistor and having its gate electrode coupled to a
third node for receiving a protection voltage;
15 and means for generating the protection voltage at a level
between the predetermined first and second values such that the
first transistor is protected against BVDSS breakdown,
characterized in that the protection voltage generating
means is coupled to the first node and comprises:
20 a third MOSFET transistor arranged to receive the
protection voltage at its gate electrode; and
means for monitoring current produced in the third
transistor due to BVDSS breakdown and for varying the protection
voltage accordingly so as to reduce the monitored current.
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2. A circuit according to claim 1 wherein the monitoring
means comprises fourth and fifth MOSFET transistors constituting
a current mirror.
- 30 3. A circuit according to claim 2 wherein the third transistor
is of the same channel type as the first and second transistors and
the fourth and fifth transistors are of opposite channel type to the
first, second and third transistors.



4. A circuit according to claim 1, 2 or 3 wherein the third transistor is an N-channel transistor and the means for monitoring increases the protection voltage so as to reduce the current monitored in the third transistor, and
5 the protection voltage generating means further comprises: a sixth MOSFET transistor having a P-channel and arranged to receive the protection voltage; and means for monitoring current produced in the sixth transistor due to BVDSS
10 accordingly so as to reduce the monitored current.

5. An integrated circuit EEPROM incorporating a MOSFET protection circuit according to any preceding claim.

15 6. A MOSFET protection circuit substantially as hereinbefore described with reference to Figure 1 or Figure 2 of the accompanying drawings.

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