

**METHOD OF LAYERING CACHE AND ARCHITECTURAL SPECIFIC
FUNCTIONS TO PERMIT GENERIC INTERFACE DEFINITION**

ABSTRACT

Cache and architectural functions within a cache controller (212) are layered and provided with generic interfaces (220-230). Layering cache and architectural operations allows the definition of generic interfaces (220-230) between controller logic and bus interface units (204-208) within the controller (212). The generic interfaces (220-230) are defined by extracting the essence of supported operations into a generic protocol. The interfaces (220-230) themselves may be pulsed or held interfaces, depending on the character of the operation. Because the controller (212) logic is isolated from the specific protocols required by a processor (102) or bus architecture, the design may be directly transferred to new controllers for different protocols or processors by modifying the bus interface units (204 and 208) appropriately.

Fig. 2

This Sheet Has Been Replaced

