

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
2 June 2005 (02.06.2005)

PCT

(10) International Publication Number
WO 2005/050977 A1

(51) International Patent Classification⁷: **H04N 3/15**
(21) International Application Number:
PCT/US2004/037729

(22) International Filing Date:
12 November 2004 (12.11.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/705,843 13 November 2003 (13.11.2003) US

(71) Applicant (for all designated States except US): **MICRON TECHNOLOGY, INC.** [US/US]; 8000 S. Federal Way, Boise, ID 83707-0006 (US).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **KRYMSKI, Alexander** [RU/CA]; 2960 Mountain Pine Drive, La Crescenta, CA 91214 (US).

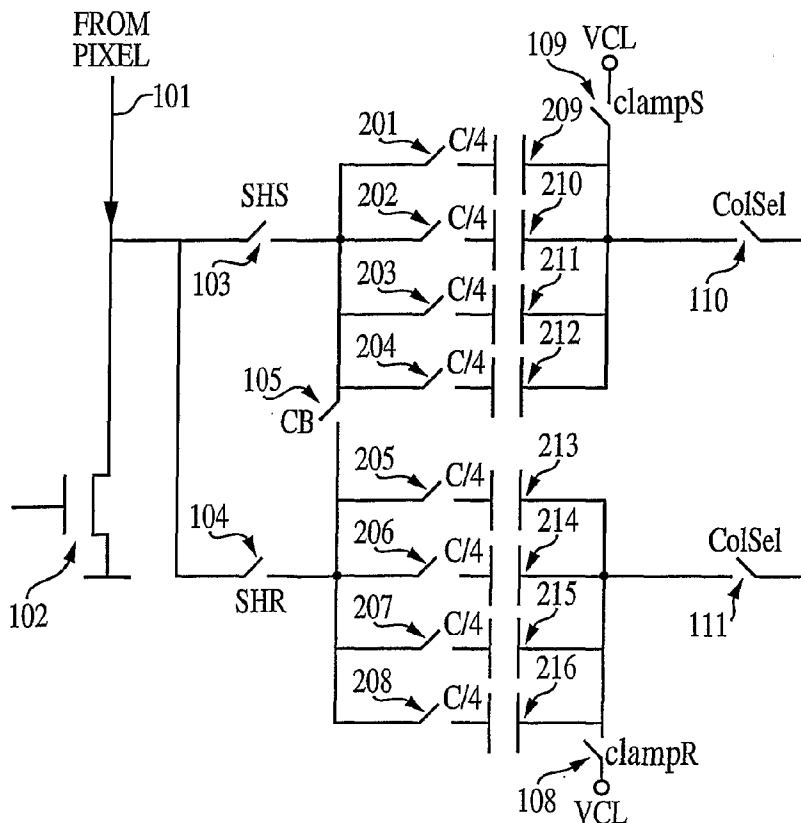
(74) Agent: **D'AMICO, Thomas, J.**; Dickstein Shapiro Morin & Oshinsky LLP, 2101 L Street, NW, Washington, DC 20037-1526 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LU, MC, NL, PL, PT, RO, SE,

[Continued on next page]

(54) Title: **PIXEL SIGNAL BINNING AND INTERPOLATION IN COLUMN CIRCUITS OF A SENSOR CIRCUIT**



(57) Abstract: A binning circuit and related method, wherein pixel signals from column circuits in a sensor circuit are sampled and interpolated. The binning circuit samples analog pixel and reset signals from different sensor circuit column lines. Once a predetermined number of column lines are sampled in the binning circuit, the sampled pixel signals are averaged together in one operation, while the reset signals are averaged together in another operation.

WO 2005/050977 A1



SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Published:

— *with international search report*