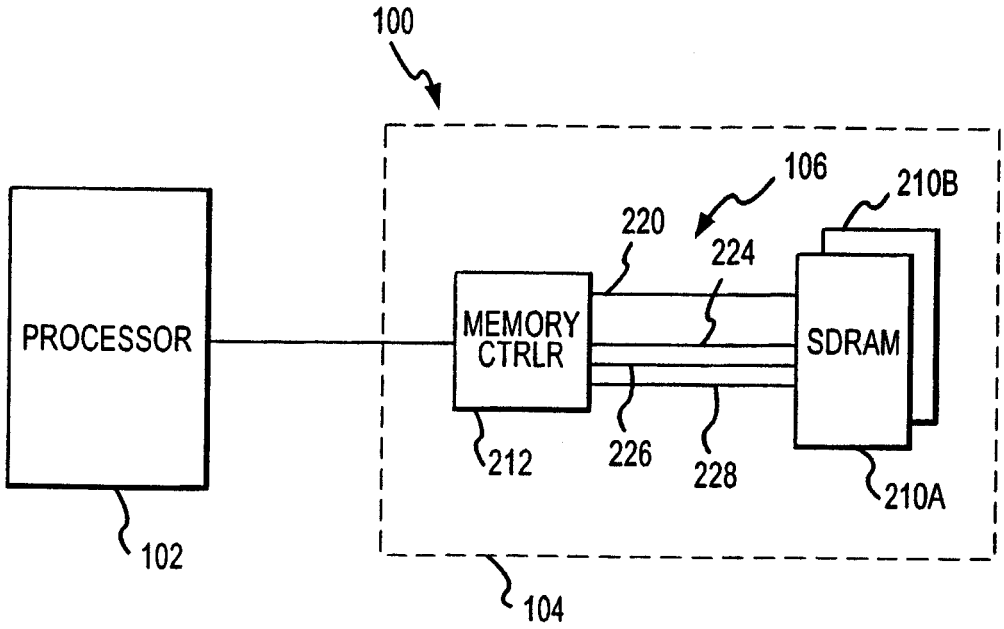

100
106
210B
220
224
PROCESSOR
MEMORY CTRLR
SDRAM
212
226
228
210A
102
104

FIG.1

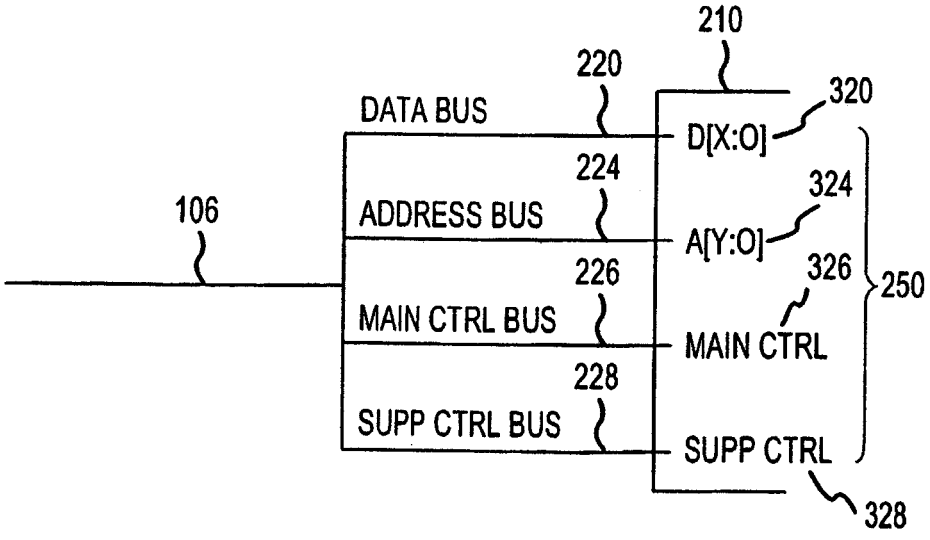

210
220
320
DATA BUS
D[X:O]
224
324
106
ADDRESS BUS
A[Y:O]
226
326
250
MAIN CTRL BUS
MAIN CTRL
228
SUPP CTRL BUS
SUPP CTRL
328

FIG.2

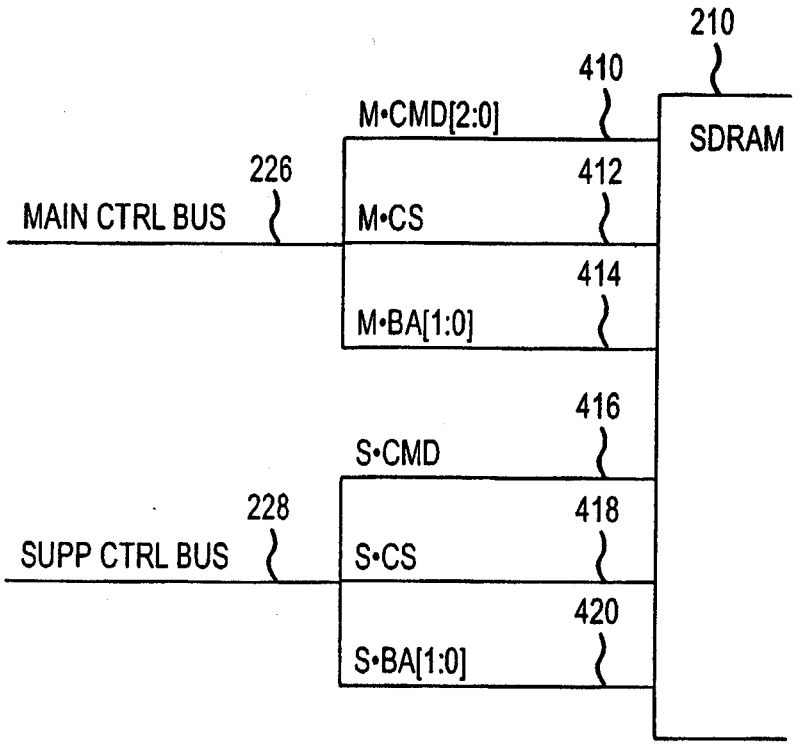

210
410
M•CMD[2:0]
SDRAM
226
412
MAIN CTRL BUS
M•CS
414
M•BA[1:0]
416
S•CMD
228
418
SUPP CTRL BUS
S•CS
420
S•BA[1:0]

FIG.3

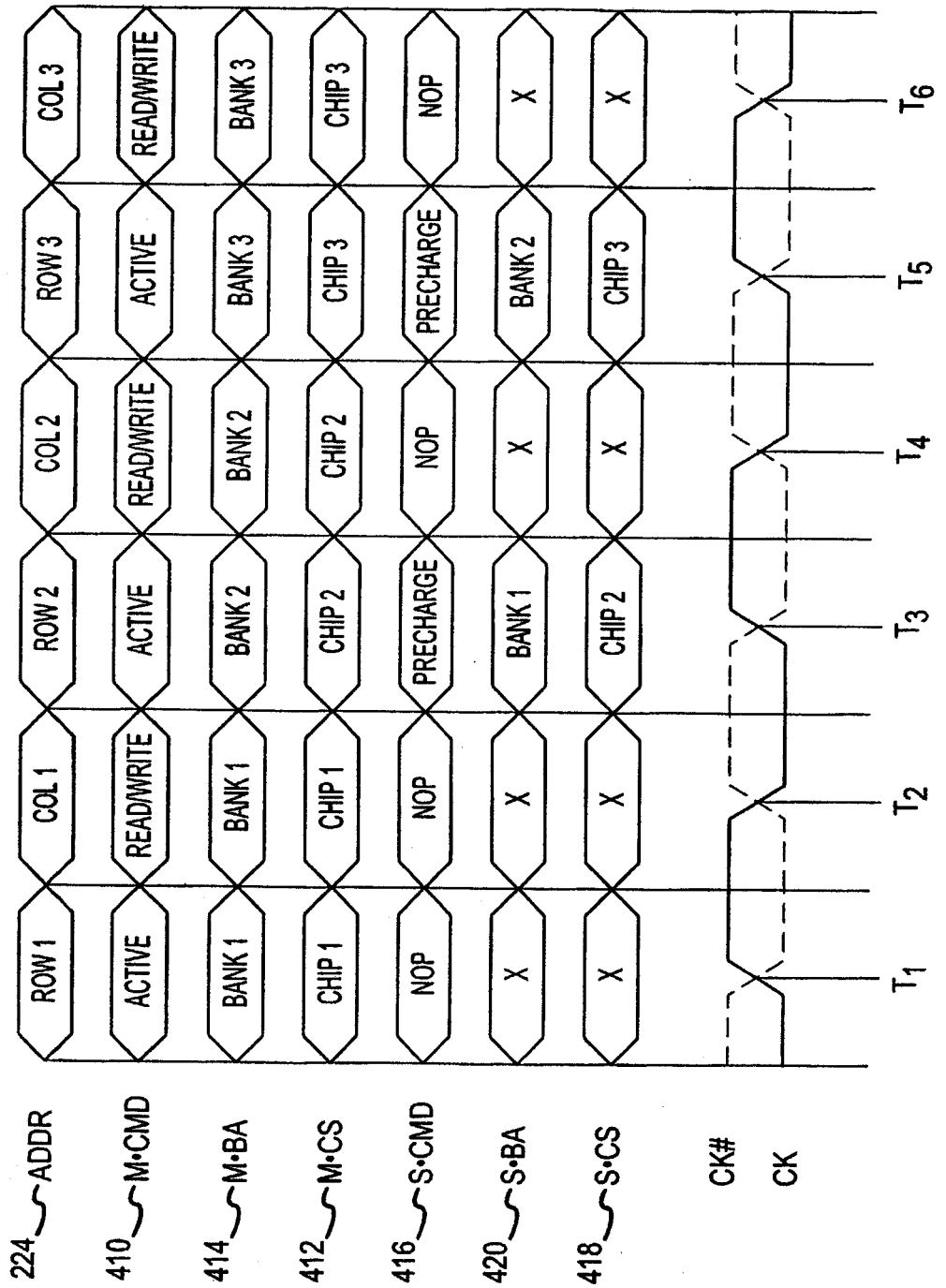

224 ADDR
410 M•CMD
414 M•BA
412 M•CS
416 S•CMD
420 S•BA
418 S•CS
CK#
CK
ROW 1
COL 1
ROW 2
COL 2
ROW 3
COL 3
ACTIVE
READ/WRITE
ACTIVE
READ/WRITE
ACTIVE
READ/WRITE
BANK 1
BANK 1
BANK 2
BANK 2
BANK 3
BANK 3
CHIP 1
CHIP 1
CHIP 2
CHIP 2
CHIP 3
CHIP 3
NOP
NOP
PRECHARGE
NOP
PRECHARGE
NOP
X
X
X
X
BANK 1
X
BANK 2
X
X
X
CHIP 2
X
CHIP 3
X
T1
T2
T3
T4
T5
T6
X=DON'T CARE

FIG.4

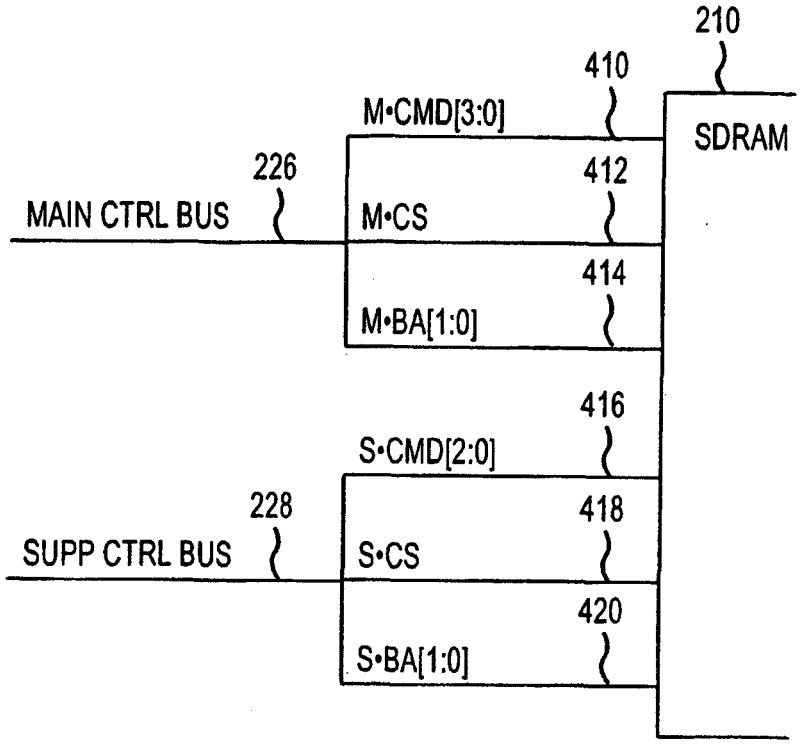

210
410
M•CMD[3:0]
SDRAM
226
412
MAIN CTRL BUS
M•CS
414
M•BA[1:0]
416
S•CMD[2:0]
228
418
SUPP CTRL BUS
S•CS
420
S•BA[1:0]

FIG.5

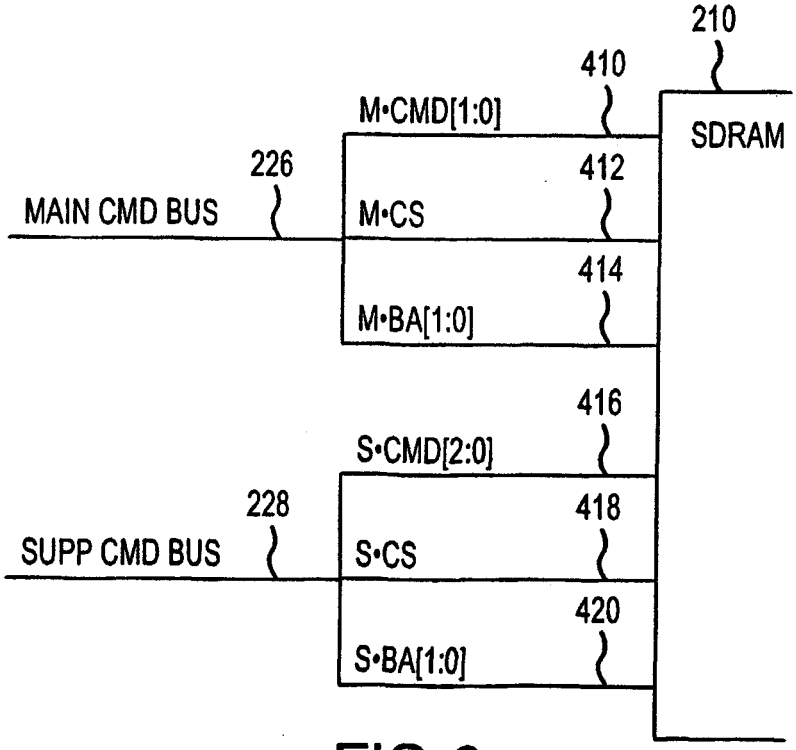

210
410
M•CMD[1:0]
SDRAM
226
412
MAIN CMD BUS
M•CS
414
M•BA[1:0]
416
S•CMD[2:0]
228
418
SUPP CMD BUS
S•CS
420
S•BA[1:0]

FIG.6

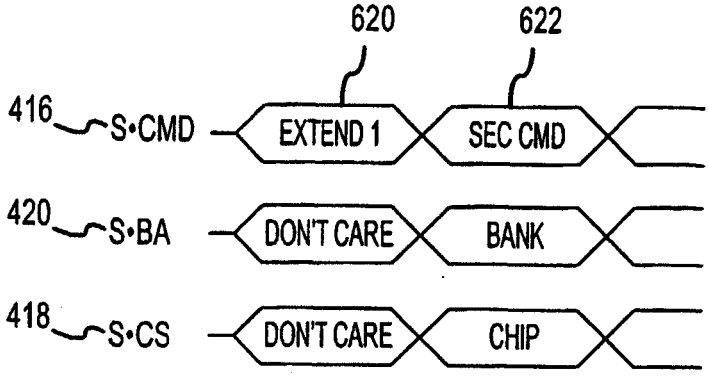

620
622
416
S•CMD
EXTEND 1
SEC CMD
420
S•BA
DON'T CARE
BANK
418
S•CS
DON'T CARE
CHIP

FIG.7

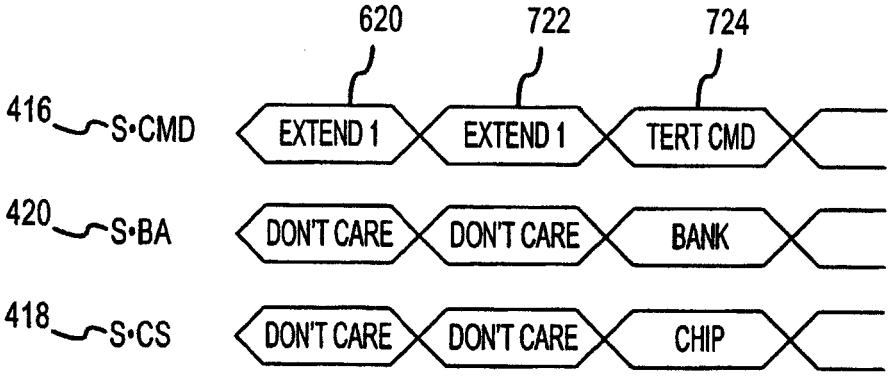
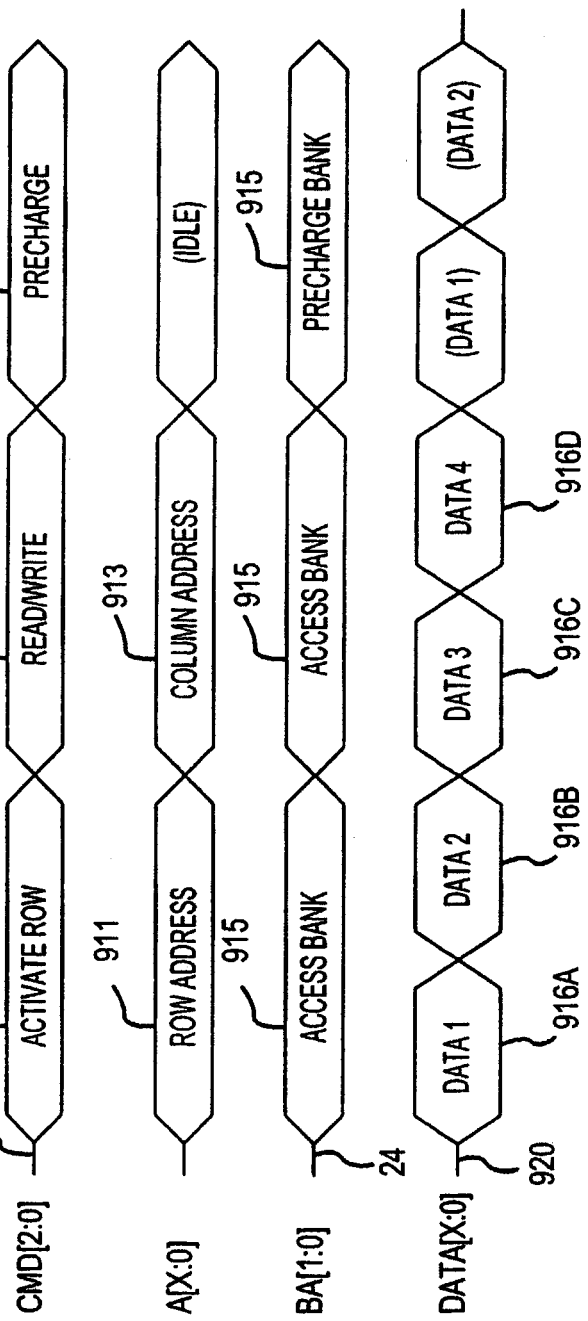

620
722
724
416
S•CMD
EXTEND 1
EXTEND 1
TERT CMD
420
S•BA
DON'T CARE
DON'T CARE
BANK
418
S•CS
DON'T CARE
DON'T CARE
CHIP

FIG.8



(PRIOR ART)

FIG.9