

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

The diagram illustrates a multi-stage processor architecture:

- Main Memory** and **Instruction Cache** are connected to the top of the system.
- Fetch Stage Instructions** (210) receives instructions from Main Memory and the Instruction Cache. It includes a **START ADDRESS** (280).
- An **MNU** (Memory Nucleus Unit) is connected to the Fetch Stage and provides address information (267) to the **TBR** (Trap Base Register).
- The **TBR** outputs **TRAP TYPE** signals (295, 296) which are fed into the **Decode Stage**.
- The **Fetch Stage** also outputs instruction addresses (28A-28D, 220) to the **INSTRUCTION FIFO** (234).
- The **INSTRUCTION FIFO** outputs instruction words (221A-221D, 230) to the **Decode Stage**.
- The **Decode Stage** contains several functional units:
 - SUPV** (Supervisor) unit (281) receiving signals 232 and 233.
 - EF** (Effective Address) unit (282) receiving signal 231.
 - CWP** (Control Word Processor) unit (283) receiving signal 3.
 - NN** (Next Node) unit (284) receiving signal 8.
- A **32 ACCESS BITS** bus (212) connects the Instruction FIFO to the Decode Stage.
- The output of the Decode Stage feeds into the **EXECUTION STAGE**, which produces the final **OUT** result.
- An **UPDATE BUS** (251) is shown at the bottom left, likely for cache coherence or state updates.