What is claimed is:

Claim 1: A method consisting essentially of:

a) providing a semiconductor comprising a front side, a back side, and a pn-junction, the front side comprises a pattern of conductive tracks and a bus bar, the conductive tracks and the bus bar comprise an underlayer and the back side includes metal contacts;

b) contacting the semiconductor with a low internal stress copper plating composition;

c) plating a low internal stress copper layer adjacent the underlayer of the conductive tracks and bus bar; and

d) attaching an interconnecting ribbon to the busbar at temperatures of 200° C or less after plating the low internal stress copper layer adjacent the underlayer to the conductive tracks and the bus bar.

Claim 2: The method of claim 1, wherein the low internal stress copper is plated by electrolytic plating or light induced plating.

Claim 3: The method of claim 1, wherein the underlayer is chosen from nickel and cobalt.

Claim 4: The method of claim 1, wherein the temperature is 150° C to 200° C.

Claim 5: The method of claim 1, wherein the underlayer is 20nm to 2µm thick.

Claim 6: The method of claim 1, wherein the low stress copper layer is 1µm to 50µm thick.

Claim 7: The method of claim 1, further consisting essentially of depositing a metal flash layer or organic solderability preservative on the low stress copper layer.

What is claimed is:

1: A method consisting essentially of:

a) providing a semiconductor comprising a front side, a back side, and a pn-junction, the front side comprises a pattern of conductive tracks and a bus bar, the conductive tracks and the bus bar comprise an underlayer and the back side includes metal contacts;

b) contacting the semiconductor with a low internal stress copper plating composition;

c) plating a low internal stress copper layer adjacent the underlayer of the conductive tracks and bus bar, wherein the low internal stress copper layer has a low internal stress of 700 psi or less; and

d) attaching an interconnecting ribbon to the busbar at temperatures of 200° C or less after plating the low internal stress copper layer adjacent the underlayer to the conductive tracks and the bus bar, wherein the method is free of any sintering.

2: The method of claim 1, wherein the low internal stress copper is plated by electrolytic plating or light induced plating.

3: The method of claim 1, wherein the underlayer is chosen from nickel and cobalt.

4: The method of claim 1, wherein the temperature is 150° C to 200° C.

5: The method of claim 1, wherein the underlayer is 20nm to 2μm thick.

6: The method of claim 1, wherein the low stress copper layer is 1μm to 50μm thick.