

PATENT SPECIFICATION

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(54) DELTA MODULATOR HAVING INCREASED DYNAMIC RANGE

(71) We, MOTOROLA, INC., a corporation of the State of Delaware, United States of America, of 5725 East River Road, Chicago, Illinois 60631, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

10 This invention relates to a delta modulator having an increased dynamic range.

Various attempts have been made to increase the effective dynamic range of delta modulation systems. One system which has been used applies a gain control to the amplifier for the modulation signal, ahead of the delta modulator, to compress the range of modulation signal. This action is compensated for by a complementary gain controlled amplifier which follows the demodulator to expand the received signal back to the full range of dynamic expression. This system, rather than increasing the dynamic range of the delta modulator, actually reduces the dynamic range of modulation signal so that it can be handled by the delta modulator. This system has the disadvantage that it has time constants, and as it does not operate instantaneously it permits overshoot of the modulation signal. Similar systems have been used which do not include time constants and therefore do not cause delay. However, these systems require critical matching of the nonlinearities.

35 In systems with low clock rates, quantizing noise appears between the complementary nonlinearities and causes intermodulation with the signal to produce additional modulation noise.

40 Systems of adaptive delta modulation have been used which adjust the quantizing step size in accordance with signal level to achieve the effect of compression in the delta modulator and expansion in the demodulator. These systems are quite com-

plex and have not been suitable for use with low clock rates. It has also been proposed to add noise to the input signal so that the noise is sufficient to break up the idle pattern of the delta modulator, and thus provide a modulation output. Although any signal, however small, will then influence the output of the delta modulator, the presence of the additional noise is objectionable.

It is an object of the invention to provide a delta modulator having a nonlinear element in the feedback path which decreases the feedback factor for low amplitude signals with respect to high amplitude signals to thereby increase the dynamic range of the delta modulator.

According to one aspect of the present invention, there is provided a delta modulator for developing a digital signal in response to a modulating signal, including comparator means having two inputs and an output, said comparator means producing a signal at said output representing the difference between signals applied at said inputs, means applying a modulating signal to one of said inputs of said comparator means, a digital signal generation means coupled to said output of said comparator means and responsive to the signal therefrom for producing a digital signal, and feedback means coupled between said digital signal generation means and the other of the inputs of said comparator means and including a filter means and nonlinear translating means, said filter means producing a signal varying with the average amplitude of said digital signal, said nonlinear translating means being coupled to said filter means and producing a modified feedback signal having reduced amplitude in response to a signal from said filter means which is below a predetermined value.

According to a further aspect of the invention there is provided a delta demodu-

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lator for use with the delta modulator described above.

The invention will now be described by way of example only, with particular reference to the accompanying drawings wherein:

Figure 1 is a block diagram of a delta modulator in accordance with the invention;

Figure 2 is a circuit diagram of the non-linear element used in the modulator of Figure 1;

Fig. 3 is a block diagram of a delta demodulator which may be used in a system with the delta modulator of Fig. 1;

Fig. 4 illustrates the transfer characteristics of the nonlinear element of Fig. 2; and

Fig. 5 shows the extension of dynamic range of the delta modulator of the invention.

Fig. 1 shows in block diagram form a delta modulator in accordance with the invention. The modulating signal, which may be an analog audio signal, is applied at input terminal 10. This signal is applied to a first input 12 of comparator 15. The comparator controls a flip-flop circuit 16 to which clock pulses are applied from terminal 18. The flip-flop 16 produces an output having one of two levels when a clock pulse is applied thereto, with the output level being determined by the polarity of the input from the comparator 15. When the input to the flip-flop 16 is of one polarity the lower level output is produced, and when the input is of the opposite polarity the higher level output is produced. The output of the flip-flop is a train of digital pulses occurring at a regular rate, with the adjacent pulses being at the higher level when a signal of one polarity is continuously applied thereto and at the lower level when the signal polarity is reversed.

The pulse train from the flip-flop 16 is applied to output terminal 20. The pulse output of flip-flop 16 is also applied to filter 22, which may include an integrator to provide an output which varies with the average amplitude of the pulse wave applied thereto. This may be a filter having a special integration characteristic as described in patent application No. 28843/74 (Serial No. 1 455 041). The output of filter 22 is applied to the nonlinear translating circuit 24 which applies a signal to the second inverting input 14 of the comparator 15. The difference between the input signal voltage appearing at comparator input 12 and the feedback signal appearing at comparator input 14 forms an error signal which determines the polarity of the output of the comparator 15.

Considering the operation of the delta modulator, when the instantaneous voltage

of the input analog signal applied to input 12 of the comparator is more positive than the signal which is fed back and applied to the second comparator input 14, the comparator output will cause the flip-flop 16 to produce a high level output pulse when triggered by the clock. If the instantaneous voltage of the input signal continues to rise at a faster rate than the signal which is fed back, the signal at input 12 will remain more positive than the signal fed back so that the output of the flip-flop 16 will remain high. When the instantaneous voltage of the input signal at terminal 12 remains constant or drops, this will fall below the signal fed back, and the output of the comparator applied to the flip-flop 16 will produce the low level output. If the comparator is essentially balanced when no input analog signal is applied, the high and low level outputs will alternate to produce an idle pattern which has a frequency of 6 kHz for a clock rate of 12 kHz. This condition is maintained so long as the signal fed back to comparator input 14 is alternately more positive and more negative than comparator input 12.

The nonlinear element 24 translates the signal applied thereto in a generally linear manner until the signal reaches a particular amplitude. This may be selected to be at or near the normal threshold of the delta modulator. Above this particular amplitude the signal is translated in a linear manner, but at a higher gain. The idle pattern at the input to the nonlinear element 24, occurring when there is no signal present, is of low level due to the frequency response characteristic of the filter 22. This idle pattern falls into the low gain region of non-linear element 24 so that the magnitude of the idle pattern fed to comparator input 14 is less than would otherwise exist. Thus less signal strength is required at comparator input 12 to seize control and effect modulation. The digital output at terminal 20 is demodulated by filter 22 and nonlinear element 24 to provide an approximation to the input signal.

Fig. 2 shows a circuit which may be used as the non-linear element 24 in the delta modulator system of Fig. 1. The output from the filter 22 is applied to input terminal 30. This signal is applied through capacitor 31 and resistor 32 to the base of transistor 34. Transistor 34 is biased from a supply potential 35 by resistor 36 connected to the collector electrode, and by resistor 37 connected in series with resistor 36 to the base electrode. The output from the collector electrode is applied through resistor 38 and capacitor 40 to the output terminal 42. Resistor 44 provides a path for signals from the input terminal 30 through capacitor 31, which path is com-

pleted through capacitor 40 to the output terminal 42. The output terminal 42 is connected to the inverting input 14 of the comparator 15 in the system of Fig. 1.

5 In the circuit of Fig. 2, when the input signal at terminal 30 is small, the transistor 34 will operate to provide an output signal which is the inversion of the input signal. This acts to partially cancel the signal from the filter applied through capacitor 31, resistor 44 and capacitor 40 to the output terminal 42. Accordingly, only a small signal will be applied to input 14 of comparator 15. When the input signal exceeds a predetermined value, which as stated above can be the level of the idle pattern from filter 22 of the delta modulator, the signal developed at the collector electrode of transistor 34 and applied through capacitor 46 to the oppositely connected diodes 47 and 48 will be sufficient to render the diodes conducting. This will limit the voltage at the collector electrode of the transistor 34 so that this voltage remains substantially constant. Accordingly, as the signal level applied to the input terminal 30 increases, the signal at the collector electrode which is applied through resistor 38 to the output terminal 42 will not increase. 30 This signal will cancel only a part of the larger signal applied through resistor 44 to the output terminal 42. As the signal level increases, the transistor output will cancel a progressively smaller portion of the signal applied through resistor 44 from the filter 22; so that the output of element 24 applied at the inverting input terminal 14 of the comparator 15 will increase.

Fig. 3 shows in block diagram form a 40 delta demodulator circuit which can be used in a communication system with the delta modulator of Fig. 1. The digital signal produced by the delta modulator of Fig. 1 can be transmitted from output terminal 20 thereof to input terminal 50 of the delta demodulator by any suitable transmission means. The digital signal is applied from terminal 50 to flip-flop 52 to which a clock input is applied at terminal 54. The clock 50 used for the flip-flop 52 of the demodulator must operate at the same rate as the clock applied to the flip-flop in the modulator and be properly phased with respect to the incoming digital signal so that it serves to reconstruct a proper digital waveform from the received signal which may have undergone various distortions during transmission. The output of the flip-flop 52 is applied to filter 56 which preferably has the same characteristics as the filter 22 of the modulator in Fig. 1. The output of the filter 56 is applied to nonlinear element 58 which may have the same characteristics as the element 24 in the modulator of Fig. 1. It 65 may be desired to provide an element hav-

ing different characteristics from that of element 24 to take care of special circumstances. The output of the nonlinear element produces the analog modulating signal or audio signal or audio signal at output terminal 60.

Fig. 4 shows the transfer characteristic of the non-linear circuit shown in Fig. 2. Curve A shows the transfer characteristic, which has a very small slope for small input 75 signals and a large slope for larger input signals. The knees or corners B of the curve are approximately at the original threshold of the delta modulator, and form junctions between the low gain center portion and the high gain outer portions. The output pulse wave of the delta demodulator when no signal is applied, commonly referred to as the idle pattern, produces an output from the filter 22 as shown by wave 85 C in Fig. 4. Such a wave when applied to the nonlinear circuit of Fig. 2, will produce an output wave as shown by curve D. The peaks of the wave of curve C may extend beyond the corners B and produce peaks in the output wave of the nonlinear element as shown by the curve D. Since the threshold of signal sensitivity of the delta modulator is proportional to the magnitude of the idle pattern voltage fed back, it is apparent that 95 the nonlinear element will reduce the idle pattern voltage to lower the signal threshold voltage.

The digital output for a large amplitude modulating signal will produce an output 100 wave from the filter 22 as shown by curve E in Fig. 4. This saturated signal input will produce an output from the nonlinear circuit as shown by curve F. As the input signal increases in either direction from 105 zero, the output will be small initially because of the small slope of the transfer characteristic between the points B. When the signal reaches these points, the output will increase to provide a high amplitude 110 output, as shown by curve F in Fig. 4.

The performance of the delta modulator as shown in Fig. 1, combination with the demodulator of Fig. 3, for a signal at 1,000 hertz and a clock rate of 12 kHz is shown 115 in Fig. 5. The dotted response curve G shows the response of the standard delta modulator wherein the filter 22 is a simple integrator and the nonlinear element 24 is not used. The dashed curve H shows the 120 response when the special loop filter of application No. 28843/74 (Serial No. 1.455 041) is used. The solid curve I shows the response of a modulator according to the invention. 125

The upper set of curve displays the level of the fundamental 1000 cps component of the output signal as a function of input signal level. The lower set of curves displays the ratio of total output signal (in- 130

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- cluding noise and distortion) to the noise and distortion contained in the output as a function of input signal level for a system which has a bandpass from 300 to 3000 Hz.
- 5 This lower set of curves is therefore an indication of the quality of the demodulated signal. The three lower curves represent the same delta modulation systems as the upper curves and are indicated in the same way.
- 10 It is apparent from Fig. 5 that the invention provides a substantial reduction of the input threshold, as compared to a typical known delta modulator. Also the noise and distortion characteristics for low level signals
- 15 is improved. The overall dynamic range of the system has been increased to provide a range of the order of 45 decibels. This represents a significant improvement over known delta modulators. The nonlinear
- 20 element used in the described embodiment of the invention is of simple and inexpensive construction and is not critical of adjustment.

WHAT WE CLAIM IS:—

- 25 1. A delta modulator for developing a digital signal in response to a modulating signal, including:
comparator means having two inputs and an output, said comparator means producing
- 30 a signal at said output representing the difference between signals applied at said inputs,
means applying a modulating signal to one of said inputs of said comparator means,
- 35 digital signal generation means coupled to said output of said comparator means and responsive to the signal therefrom for producing a digital signal, and
feedback means coupled between said
- 40 digital signal generation means and the other of said inputs of said comparator means and including a filter means and nonlinear translating means, said filter means producing a signal varying with the average
- 45 amplitude of said digital signal, said nonlinear translating means being coupled to said filter means and producing a modified feedback signal having reduced amplitude in response to a signal from said filter means
- 50 which is below a predetermined value.
2. A delta modulator as claimed in claim 1 wherein said comparator means has first and second inputs, one of which inverts the signal applied thereto, with said modulating
- 55 signal being applied to said first input

and said modified feedback signal being applied to said second input, said comparator producing an output of one polarity in response to a modulating signal which is more positive than the modified feedback 60 signal and producing an output of the opposite polarity in response to a modulating signal which is more negative than the modified feedback signal.

3. A delta modulator as claimed in claim 2 wherein said digital signal generation means includes means responsive to clock pulses for producing output signals of first and second levels, said signal generation means producing an output of said first level 70 in response to a signal from said comparator means of one polarity and producing an output signal of said second level in response to a signal from said comparator means of opposite polarity. 75

4. A delta modulator as claimed in claim 1 wherein said nonlinear translating means includes means forming first and second signal paths connected in parallel, with said first signal path including means for inverting the signal therein to cancel at least a portion of the signal in said second signal path. 80

5. A delta modulator as claimed in claim 4 wherein said nonlinear translating means includes means in said first path which inverts the signal, and limiting means for limiting the amplitude of the signal in said first path to a predetermined value, whereby at low signal levels the signal in said first path 90 substantially cancels the signal in said second path and at high signal levels the signal in said first path is limited and cancels only a portion of the signal in said second path.

6. A delta modulator as claimed in claim 5 wherein said means in said first path which inverts the signal includes a transistor. 95

7. A delta modulator substantially as hereinbefore described and as shown in Figures 1 and 2 of the accompanying drawings. 100

8. A delta demodulator for use with a delta modulator as claimed in claim 1 the demodulator being substantially as herein-described and as shown in Figure 3 of the accompanying drawings. 105

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- cluding noise and distortion) to the noise and distortion contained in the output as a function of input signal level for a system which has a bandpass from 300 to 3000 Hz.
- 5 This lower set of curves is therefore an indication of the quality of the demodulated signal. The three lower curves represent the same delta modulation systems as the upper curves and are indicated in the same way.
- 10 It is apparent from Fig. 5 that the invention provides a substantial reduction of the input threshold, as compared to a typical known delta modulator. Also the noise and distortion characteristics for low level signals
- 15 is improved. The overall dynamic range of the system has been increased to provide a range of the order of 45 decibels. This represents a significant improvement over known delta modulators. The nonlinear
- 20 element used in the described embodiment of the invention is of simple and inexpensive construction and is not critical of adjustment.
- WHAT WE CLAIM IS:—
- 25 1. A delta modulator for developing a digital signal in response to a modulating signal, including:
comparator means having two inputs and an output, said comparator means producing a signal at said output representing the difference between signals applied at said inputs,
means applying a modulating signal to one of said inputs of said comparator means,
- 35 digital signal generation means coupled to said output of said comparator means and responsive to the signal therefrom for producing a digital signal, and
feedback means coupled between said
- 40 digital signal generation means and the other of said inputs of said comparator means and including a filter means and nonlinear translating means, said filter means producing a signal varying with the average
- 45 amplitude of said digital signal, said nonlinear translating means being coupled to said filter means and producing a modified feedback signal having reduced amplitude in response to a signal from said filter means
- 50 which is below a predetermined value.
2. A delta modulator as claimed in claim 1 wherein said comparator means has first and second inputs, one of which inverts the signal applied thereto, with said modulating signal being applied to said first input
- and said modified feedback signal being applied to said second input, said comparator producing an output of one polarity in response to a modulating signal which is more positive than the modified feedback
- 60 signal and producing an output of the opposite polarity in response to a modulating signal which is more negative than the modified feedback signal.
3. A delta modulator as claimed in claim 2 wherein said digital signal generation means includes means responsive to clock pulses for producing output signals of first and second levels, said signal generation means producing an output of said first level
- 70 in response to a signal from said comparator means of one polarity and producing an output signal of said second level in response to a signal from said comparator means of opposite polarity.
- 75 4. A delta modulator as claimed in claim 1 wherein said nonlinear translating means includes means forming first and second signal paths connected in parallel, with said first signal path including means for inverting the signal therein to cancel at least a portion of the signal in said second signal path.
- 80 5. A delta modulator as claimed in claim 4 wherein said nonlinear translating means includes means in said first path which inverts the signal, and limiting means for limiting the amplitude of the signal in said first path to a predetermined value, whereby at low signal levels the signal in said first path
- 85 substantially cancels the signal in said second path and at high signal levels the signal in said first path is limited and cancels only a portion of the signal in said second path.
- 90 6. A delta modulator as claimed in claim 5 wherein said means in said first path which inverts the signal includes a transistor.
- 95 7. A delta modulator substantially as hereinbefore described and as shown in Figures 1 and 2 of the accompanying drawings.
- 100 8. A delta demodulator for use with a delta modulator as claimed in claim 1 the demodulator being substantially as herein-described and as shown in Figure 3 of the accompanying drawings.
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