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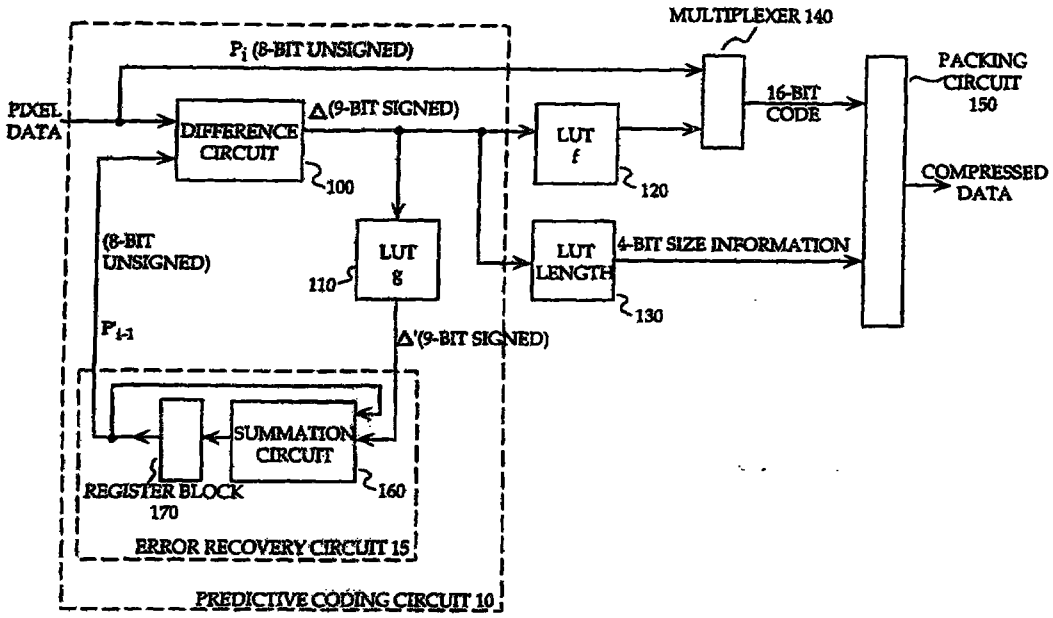
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(54) Title: A MEMORY BASED VLSI ARCHITECTURE FOR IMAGE COMPRESSION



(57) Abstract

An image compression apparatus is discussed that includes a first look-up table (120) providing a quantized code, a second look-up table (130) providing the length of that code, and a predictive coding circuit (10) which generates an address for indexed those look-up tables (120, 130).