

CLAIMS

1. Semiconductor wafer (10) comprising a monocrystalline substrate wafer (1) consisting essentially of silicon,
the monocrystalline substrate wafer (1) being structured to have tips (3) on its top surface,
each of the tips (3) being covered in the given order with a group-IIIB silicide layer (5) and a group-IIIB nitride layer (6),
the group-IIIB silicide layer (5) having a thickness of not less than 5 nm and
the group-IIIB nitride layer (6) being covered with a monocrystalline group-IIIA nitride layer (7, 8).
2. Semiconductor wafer (10) according to claim 1, wherein a contact area between the group-IIIB nitride layer (6) and the monocrystalline group-IIIA nitride layer (7, 8) is not more than 50% of the grown group-IIIA nitride layer in case of a coalesced film.
3. Semiconductor wafer (10) according to claim 1 or 2, the tips having a height between 100 nm and 50 μm , preferably at least 3 μm .
4. Semiconductor wafer (10) according to any one of the preceding claims, the tips having a bottom width between 1 nm and 10 μm .
5. Semiconductor wafer (10) according to any one of the preceding claims, the tips having a center-to-center distance between 100 nm and 10 μm , preferably at most 3 μm .
6. Semiconductor wafer (10) according to any one of the preceding claims, the group-IIIB nitride layer (6) having a (111) surface orientation and/or being either a single layer of ScN or YN, or a double layer of ScN and YN, or a multiple mixed or graded layer of $\text{Y}_{1-x}\text{Sc}_x\text{N}$ with $0 \leq x \leq 1$.

7. Semiconductor wafer (10) according to any one of the preceding claims, the group-IIIB silicide layer (5) having a (0001) surface orientation and/or being a $Y_{1-z}Sc_zSi_x$ layer with $0 \leq z \leq 1$.
8. Semiconductor wafer (10) according to any one of the preceding claims, the monocrystalline group-IIIA nitride layer (7, 8) being a coalesced film or a structured layer, especially comprising an array of rods, blocks, tips or pyramids.
9. Semiconductor wafer (10) according to any one of the preceding claims, the monocrystalline group-IIIA nitride layer (7, 8) being a monocrystalline $In_xAl_zGa_{1-(x+z)}N$ layer with $0 \leq x, z, (x+z) \leq 1$.
10. Semiconductor wafer (10) according to any one of the preceding claims, the monocrystalline group-IIIA nitride layer (7, 8) having a (0001) surface orientation.
11. Semiconductor wafer (10) according to any one of the preceding claims, the monocrystalline substrate wafer (1) being a Si(111) or Si(001) wafer.
12. Use of a semiconductor wafer (10) according to any one of the preceding claims as a substrate for producing light emitting elements, field effect transistors, or for microstructure printing.
13. Method for producing a semiconductor wafer (10) according to any one of the preceding claims, comprising the steps of:
 - providing a monocrystalline substrate wafer (1),
 - structuring the substrate wafer (1) to form tips (3) on its top surface,
 - covering the tips (3) in the given order with a group-IIIB silicide layer (5) and a group-IIIB nitride layer (6),
 - the group-IIIB silicide layer (5) having a thickness of not less than 5 nm,
 - covering the group-IIIB nitride layer (6) with a monocrystalline group-IIIA nitride layer (7, 8).

14. Method according to claim 13, the step of covering the tips (3) in the given order with a group-IIIB silicide layer (5) and a group-IIIB nitride layer (6) comprises forming the group-IIIB silicide layer (5) by a silicidation process.

15. Method according to claim 13 or 14, the step of covering the tips (3) in the given order with a group-IIIB silicide layer (5) and a group-IIIB nitride layer (6) comprises depositing group-IIIB nitride on top of group-IIIB silicide by in situ nitridation of group-IIIB silicide surface, or by MBE technique.