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VIDEO GRAPHIC DYNAMIC RAM

Background of the Invention

This invention relates, in general, to semiconductor memories, and more particularly, to a memory useful in a video graphic system.

Video graphic systems require a great deal of memory capacity. One of the most critical memory requirements for a video graphic system is the rate at which data must be read from the memory to refresh the cathode ray tube (CRT) display. Data rates of eight to fifty M bytes/sec are common. Next is the ability of the memory to have additional bandwidth to allow update of the memory without interfering with the video refresh of the CRT. The third priority is the ability to asynchronously change the data flow to another address sequence within a reasonable time. This third requirement is needed to handle smooth scrolling and multiple windows to the memory. With present memory architecture of a dynamic RAM, the data path depth must be increased to handle increased bandwidth. This increases the memory chip count and decreases the optimal size depending upon the number of display frames required. For higher density displays which require higher bandwidth, larger memory sizes are not the most efficient approach to take. In addition, it is also desirable to write into the memory at the same time that the memory is being used to refresh the CRT display.

One suggested memory had a shift register which received an entire row of data. However, since a picture frame will likely start on other than a boundary established by the first bit to be shifted out, such a memory is not considered totally satisfactory. Also this type of memory does not allow for the boundary to be changed while sequencing data for a horizontal line.

Therefore, there is a need for an architecture of a memory chip which can perform a CRT display refresh cycle by placing multiple bytes into a shift register which can then be shifted out independent of the standard access.

Accordingly, it is an object of the present invention to provide an improved memory chip.

Another object of the present invention is to provide a memory which has the capability to shift data out independently from the normal access to a standard memory.

Yet another object of the present invention is to provide a memory which can serially shift data out at a high rate of speed while providing access to odd boundaries of a CRT display associated with the memory.

Summary of the Invention

The above and other objects and advantages of the present invention are achieved by providing a latch on the same integrated circuit as a standard memory array. In addition to the latch there is also provided a temporary storage register, a multiplexer, and means for controlling the multiplexer. The latch is coupled to the standard memory and receives an entire row of data. Upon command the data is transferred from the latch to the storage register. The storage register is coupled to the multiplexer which can sequentially shift out of the storage register the data stored therein.

The subject matter which is regarded as the instant invention is set forth in the appended claims. The invention itself, however, together with further objects and advantages thereof, may be better understood by referring to the following detailed description taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

FIG. 1 is a block diagram showing a portion of the circuitry needed for controlling a CRT display;

FIG. 2 shows in block diagram form an embodiment of the present invention useful in the system of FIG. 1; and

FIG. 3 shows yet another embodiment of the present invention useful in the system of FIG. 1.

The exemplifications set out herein illustrate the preferred embodiments of the invention in one form thereof and such exemplifications are not to be construed as limiting in any manner.

Detailed Description of the Drawings

FIG. 1 illustrates in block diagram form most of the circuitry needed in a video graphic display system. The block diagram represents, in general, just one of many video graphic display systems in which the present invention would be useful. Random access memory (RAM) 10 is used as the video display memory and the block diagram representing RAM 10 is shown as having some depth to indicate that there is more than one RAM chip being used. By use of the present invention, however, the CRT that would be connected to the video, blanking, and horizontal sync output lines of output interface 16 can be controlled with as few as four 64K dynamic RAMs. Serial data can be shifted out (SOUT) of RAM 10 at a rate in the 20 to 25 megahertz range. This data is coupled by a data bus to output interface 16. RAM 10 is controlled by an advanced CRT controller 11 which also performs other control functions for the display system. Advanced CRT controller 11 has a bus interface port which is used for connecting controller 11 to a microprocessor (not shown). Controller 11 also has an address bus plus control signals going to a memory control circuit 12. The MPU (not shown) is

connected to memory control circuit 12 by a system bus. Memory control circuit 12 is also connected to memory 10 and provides required control signals for memory 10. A graphic generator 13 is connected to memory control circuit 12 as well as to the MPU by way of bus interface connections. Controller 11 provides control data to output interface 16 and is coupled to output interface 16 by two handshake lines 18 and 19. A vertical sync is provided by controller 11 for the CRT display (not shown). A serial clock logic circuit 14 receives an input from controller 11 as well as from handshake line 19. Handshake line 19 carries a signal from output interface 16 to logic circuit 14. Logic circuit 14 generates a serial clock signal which is used by RAM 10. An additional clock 17 provides the necessary timing signals for output interface 16.

FIG. 2 illustrates in block diagram form a memory chip suitable for use in memory bank 10 of FIG. 1. A memory chip 25 contains a standard memory array 26. Dotted line 27 is used to illustrate a row of data in memory array 26. The entire row of data can be transferred to a latch 28 all at once. Signal $\overline{\text{SCAS}}$ is a command used to transfer the data from row 27 to latch 28. $\overline{\text{SCAS}}$ is a serial column address strobe signal similar to $\overline{\text{CAS}}$ which is a standard well known column address strobe used in memory array 26. Memory array 26 has all of the standard interface pins necessary for a standard dynamic RAM. These pins appear as interface pins for memory chip 25. VSS and VCC provide power for memory chip 25. Pin D is a data input pin for memory array 26 while pin Q carries the data outputted by memory array 26. An R/W pin provides the read/write signal for memory array 26. Row address strobe, $\overline{\text{RAS}}$, and column address strobe, $\overline{\text{CAS}}$, are supplied to memory array 26. In addition, an eight-bit multiplexer address bus is provided to eight-bit latch 32. Eight-bit latch 32 is loaded at the same time that latch 28 is loaded by $\overline{\text{SCAS}}$.

Latch 28 is coupled to a shift register 29. All of the data from latch 28 is transferred to shift register 29 upon the serial load command $\overline{\text{SLOAD}}$ signal. $\overline{\text{SLOAD}}$ signal also allows the multiplexer address from latch 32 to be transferred to an eight-bit latch 33. The data in shift register 29 is shifted to serial output line, SOUT, through a multiplexer 31 under command of a decoder 34. Decoder 34 receives the multiplexer address from eight-bit latch 33 and decodes the address to provide the command to multiplexer 31. The data from shift register 29 is shifted out serially through multiplexer 31 and timed to serial clock, SCLK, signal. An optional line connected to shift register 29 is a serial input, SIN, line which allows serial data to be coupled into shift register 29 from a source external from memory chip 25.

By way of example, if memory array 26 is a 64K X 1 bit memory array such as MCM6664, which is made and sold by Motorola Inc., a 256 bit row of data can be transferred to a 256-bit latch 28. In such a case shift register 29 would be a 256-bit shift register and multiplexer 31 would be a 256 to one multiplexer, and decoder 34 would be an 8-to-256 decoder. The bandwidth of shift register 29 and how it gets loaded determines the boundary of the video display. It is very likely that a picture frame will start on other than this boundary and change several times while sequencing data for horizontal lines. The wider the shift register becomes the more severe the problem. Therefore, a multiplexer address is used which is decoded by decoder 34 and can commence shifting data out from shift register 29 at any bit location of the shift register. The serial clock signal, SCLK, will then continue shifting the data out serially through multiplexer 31. The data can be shifted out at a maximum rate of 40 nanoseconds per bit for a typical 150 nanosecond RAM. This memory architecture allows the CRT control circuitry to start on any bit within the 256-bit boundary. An additional advantage is the

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separation of the normal RAM cycle timing from the loading of shift register 29 which comes about with the inclusion of buffer latch 28 and separate load input signal $\overline{\text{SLOAD}}$. To keep the serial data stream going the loading of shift register 29 must be precise to twice the shift clock. With this separation the RAM cycle is independent of the loading time. Memory array 26 performs standard memory operations, such as reading and writing, through pins D and Q when there is a $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycle.

Dotted line 36 is used to illustrate, in memory chip 25, the standard memory array above line 36 and the newly-added circuit below dotted line 36.

In operation, the serial fetch of data from output SOUT is independent of the operation of memory array 26 once buffer latch 28 is loaded. After the data from latch 28 is transferred from shift register 29, memory array 26 is free to reload latch 28 at any time after the transfer but before all the data has been shifted out of shift register 29 through multiplexer 31. $\overline{\text{RAS}}$ signal is used to enable the data such as in row 27. $\overline{\text{SCAS}}$ is used to obtain output positions of the serial data in shift register 29 through control of multiplexer 31. The negative transition of $\overline{\text{SCAS}}$ latches the 8-bit multiplexer address into latch 32. The positive transition of $\overline{\text{SCAS}}$ latches the data in buffer latch 28. At this time memory array 26 is released to complete the precharge and additional cycles. When the CRT controller has shifted out old data it can load data to shift register 29 on its own timing, at which time, the 8-bit address is also transferred to decoder 34. Decoder 34 and multiplexer 31 allow the output data position within shift register 29 to be selected. Data is then shifted out at the clock rate of SCLK from the chosen position followed by those bits of higher address within shift register 29. $\overline{\text{SLOAD}}$ is a signal provided by the CRT controller and is triggered when shift register 29 is empty.

FIG. 3 illustrates another embodiment of memory chip 25 of FIG. 2. In FIG. 3, memory chip 40 contains many similar elements to the elements of FIG. 2. Such similar elements are identified by the same reference numerals and their function and operation will not be reiterated in detail. The main difference with memory chip 40 is in the manner that the serial data is selected for shifting out. A second latch 44 is coupled to latch 28 and is loaded upon command of $\overline{\text{SLOAD}}$. Latch 44 is coupled to output SOUT by a plurality of controllable buffers 43. Although only a few of controllable buffers 43 are illustrated it will be recognized that each bit stored in latch 44 requires one buffer or controllable gate to couple it to the SOUT pin. The controllable buffers 43 are controlled by outputs from decoder 42. The address that is decoded by decoder 42 is received by latch 32 and coupled to counter 41 upon the $\overline{\text{SLOAD}}$ signal. Counter 41 provides the address to be decoded to decoder 42 and at the same time receives SCLK signal which sequentially varies the output of decoder 42 so that data from latch 44 can be coupled sequentially by the proper buffer 43 to the SOUT pin. Memory chip 40 is illustrated, only by way of example, as having a 64K X 1 bit memory array, thereby providing a 256-bit row. Accordingly then latch 28 and latch 44 are each 256 bits wide. And since 256 bits can be coded into an 8-bit signal latch 32 and counter 41 are each eight bits wide. It then follows that decoder 42 is an 8-to-256 decoder. Decoder 42 and the plurality of controllable buffers 43 function as a multiplexer to couple the data from latch 44 to the single output pin SOUT.

It will be noted that the present invention is applicable to larger as well as smaller memories than 64K. The latch should be large enough to hold the number of bits in a row, i.e. 2^n bits where n is an integer. Then the number of bits handled by the decoder section should be equal to n.

Although the memory array of the present invention has been illustrated in conjunction with a CRT video system it should be recognized that such a memory chip can be used effectively in a data buffer for DMA applications wherein data is placed in a RAM through a standard mode of operation and then DMAed out using the serial mode such as a huge type of FIFO system. Another use would be prefetching of instructions from a program RAM to rapidly fill a CACHE system. Yet another application would be in disk transfers at independent speeds.

By now it should be appreciated that there has been provided an improved memory chip which is extremely useful in shifting out data at a high rate of speed while allowing the main memory array of the memory chip to function in a normal manner. When this improved memory chip is used in a video circuit it allows the CRT display to be refreshed while updating the RAM with new information. Other advantages are that the RAM bandwidth is increased and a boundary condition within the memory can be overcome. The chip is useful in video digitizing and serial data retrievals.

CLAIMS

1. A monolithic memory capable of providing output data at a high speed, comprising: a standard memory array; a latch capable of latching a plurality of data bits, the latch being coupled to the standard memory for temporarily storing data from the standard memory; a shift register capable of storing a plurality of data bits, the shift register being coupled to the latch for receiving the data temporarily stored in the latch; and a multiplexer coupled to the shift register for selecting a predetermined data bit from the shift register and sequentially coupling the data out of the shift register to an output pin of the monolithic memory commencing with the predetermined data bit.

2. The memory of claim 1 further including means for commanding the multiplexer to select the predetermined data bit.

3. The memory of claim 2 wherein the means for commanding is a decoder.

4. The memory of claim 1 wherein the latch and the shift register each handle the same number of data bits so that plurality in each case is equal to an integer n, and wherein the multiplexer is an n-to-one multiplexer.

5. The memory of claim 4 wherein n equals 256.

6. The memory of claim 1 wherein the standard memory is a dynamic random access memory (RAM).

7. A method of reading data out of a memory for use at a high rate of speed, comprising: latching a block of data in a first temporary storage, wherein the block of data contains a predetermined number of bits; loading the block of data from the first temporary storage into a second

temporary storage; and selecting a particular bit in the block of data in the second temporary storage to shift out first and continuing shifting out data from the second temporary storage in a sequential manner.

8. The method of claim 7 further including reading/writing data into or out of the memory in a normal manner while the data is being shifted out of the second temporary storage.

9. The method of claim 8 further including latching another block of data in the first temporary storage during the time that the data is being shifted out of the second temporary storage.

10. A video display system having at least a memory system, and a controller to control operation of the video display system, the memory system comprising: a latch for storing at least one row of data, the latch being loaded upon a first command from the controller; first means for temporarily storing coupled to the latch for receiving the row of data from the latch upon a second command from the controller; and second means for selecting a predetermined bit in the first means to commence serially shifting data out of the first means.

11. The video display system of claim 10 wherein the second means includes an address latch for temporarily storing an address of the predetermined bit, a decoder for decoding the temporarily stored address, and a plurality of controllable means controlled by the decoder for serially coupling the data out of the first means.

12. An architecture for a high speed memory placed on an integrated circuit chip, the integrated circuit having a standard dynamic random access memory (RAM) and further comprising: first means for temporarily storing a block of

data from the RAM; second means for temporarily storing coupled to the first means for controllably receiving the block of data from the first means; a temporary storage for temporarily storing an address for a predetermined bit of data within the block of data; a decoder coupled to the temporary storage for decoding the address of the predetermined bit; and third means coupled to the second means and to the decoder for serially outputting the data of the second means upon command of the decoder to commence with the predetermined bit while allowing the RAM to be written into and read from in a normal manner during the time the data is being outputted from the second means.

13. The architecture for a high speed memory of claim 12 further including a counter located between the temporary storage and the decoder.

14. The architecture for a high speed memory of claim 12 wherein the first and second means are latches and the third means are a plurality of controllable gates which are individually controlled by the decoder.

15. The architecture for a high speed memory of claim 12 wherein the first means is a latch, the second means is a shift register, and the third means is a multiplexer.